

FMOSCPW70N120-H

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FMOSCPW70N120-H

70A 1200V N-Channel Silicon Carbide Enhancement Mode Power MOSFET

Features

- $V_{DS}=1200V$, $I_D=70A$.
- $R_{DS(ON)} \leq 42m\Omega$, @ $V_{GS}=18V$, $I_D=30A$.
- Optimized on-resistance with rapid switching behavior.
- Compatible with standard gate drivers.
- High avalanche endurance capability.
- Optimized for high power density applications.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21).

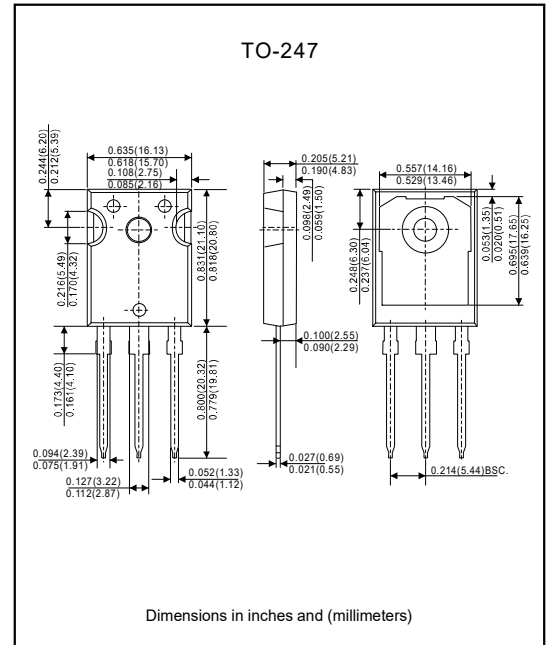
Applications

- Switching mode power supply, PFC and DC/DC converter.
- EV charging station, UPS and renewable energy.
- Power inverter and motor driver.

Mechanical data

- Epoxy : UL94-V0 rated flame retardant.
- Case : Molded plastic, TO-247.
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026.
- Weight : Approximated 6.15g.

Package outline



Maximum ratings (At $T_J=25^\circ C$ unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Minimum drain to source voltage	$V_{GS}=0V$, $I_D=100\mu A$	V_{DS}	1200			V
Operate gate to source voltage (Recommended operating values)		$V_{GS_Op.}$	-8~0		15~18	V
Transient gate to source voltage (Transient operating limit)	AC f > 1Hz, pulse width < 100ns	$V_{GS_Tran.}$	-10		22	V
Continuous drain current	$V_{GS}=18V$, $T_c=25^\circ C$	I_D			70	A
Pulsed drain current		I_{DM}			160	A
Continuous body diode current	$V_{GS}=0V$, $T_c=25^\circ C$	I_S			55	A
Power dissipation	$T_c=25^\circ C$	P_D			300	W
Thermal resistance, junction to ambient	Device on PCB, with 6cm ² of cooling area	$R_{\theta JA}$		40		$^\circ C/W$
Thermal resistance, junction to case		$R_{\theta JC}$		0.5		$^\circ C/W$
Soldering temperature		T_L			260	$^\circ C$
Junction temperature range		T_J	-55		+175	$^\circ C$
Storage temperature range		T_{STG}	-55		+175	$^\circ C$

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Electrical characteristics (At $T_J=25^\circ\text{C}$ unless otherwise specified)

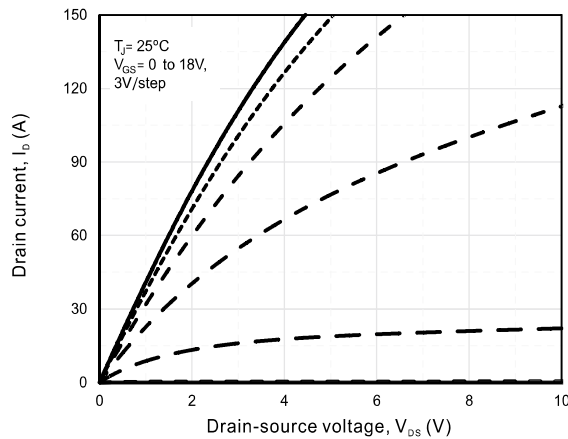
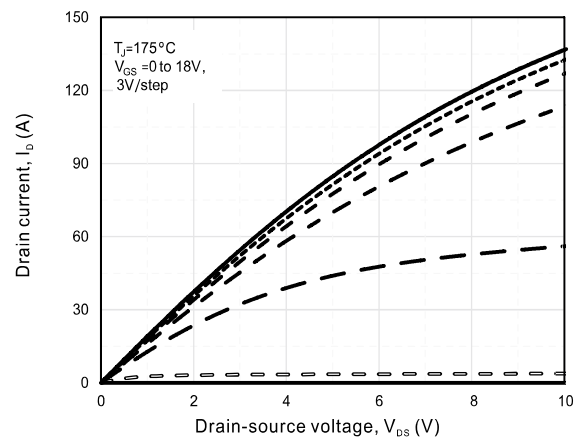
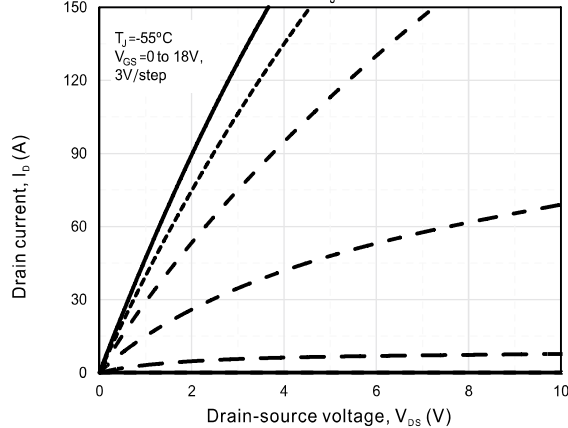
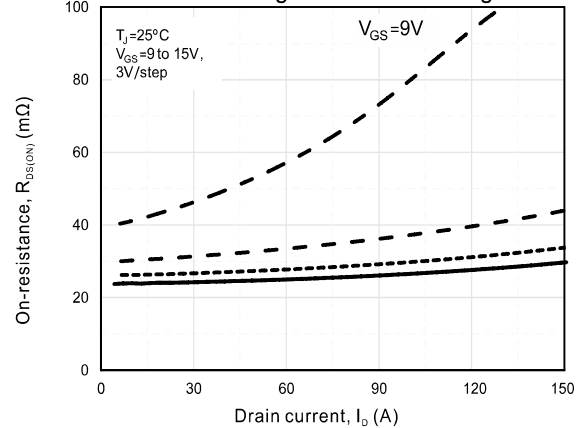
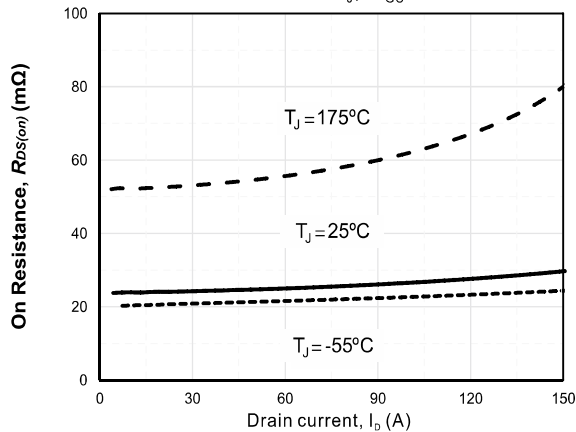
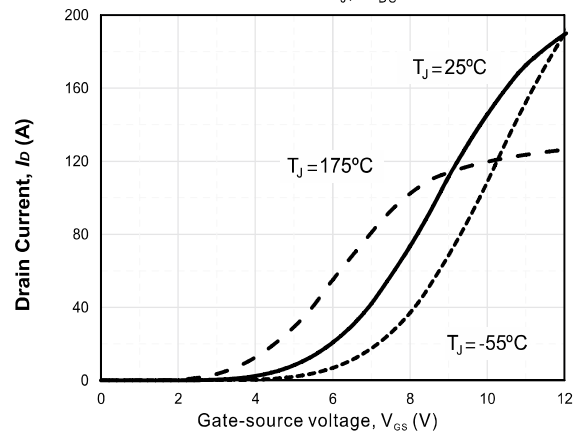
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	BV_{DS}	$I_D=100\mu\text{A}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	1200			V
		$I_D=100\mu\text{A}$, $V_{GS}=0\text{V}$, $T_J=175^\circ\text{C}$		1200		
Drain-source leakage current	I_{DSS}	$V_{DS}=1200\text{V}$, $V_{GS}=0\text{V}$		1	60	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=18\text{V}$, $V_{DS}=0\text{V}$			100	nA
On characteristics						
Gate threshold voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=60\text{mA}$		2.8		V
Static drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=18\text{V}$, $I_D=30\text{A}$, $T_J=25^\circ\text{C}$		30	42	m Ω
		$V_{GS}=18\text{V}$, $I_D=30\text{A}$, $T_J=175^\circ\text{C}$		50		
Transconductance	g_{FS}	$V_{DS}=20\text{V}$, $I_{DS}=40\text{A}$		15.1		S
Dynamic parameters						
Input capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=800\text{V}$, $f=250\text{kHz}$, $V_{AC}=25\text{mV}$		3700		pF
Out capacitance	C_{oss}			106		
Reverse capacitance	C_{rss}			15		
Effective output capacitance, energy related (Note1)	$C_{o(er)}$			131		
Effective output capacitance, time related (Note2)	$C_{o(tr)}$			216		
C_{OSS} Stored energy	E_{OSS}	$V_{GS}=0\text{V}$, $V_{DS}=800\text{V}$, $f=250\text{kHz}$, $V_{AC}=25\text{mV}$		41.9		μJ
Output capacitive charge	Q_{oss}	$V_{GS}=0\text{V}$, $V_{DS}=800\text{V}$, $f=250\text{kHz}$, $V_{AC}=25\text{mV}$		173		nC
Internal gate resistance	$R_{G_int.}$	$f=1.0\text{MHz}$, $V_{AC}=25\text{mV}$		2.2		Ω

Note: 1. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 800V.

2. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 800V.

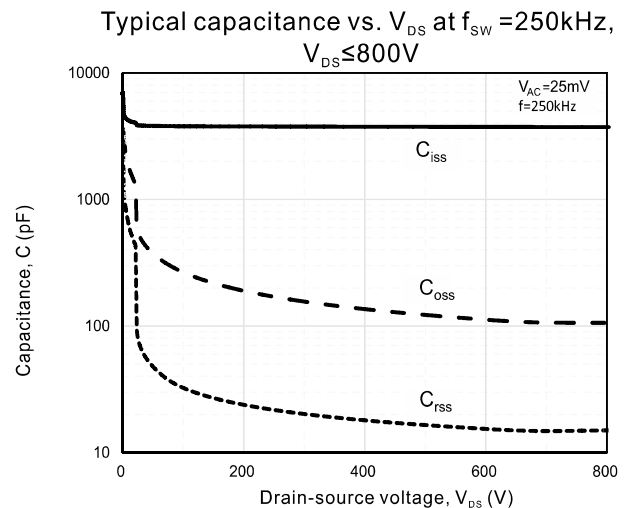
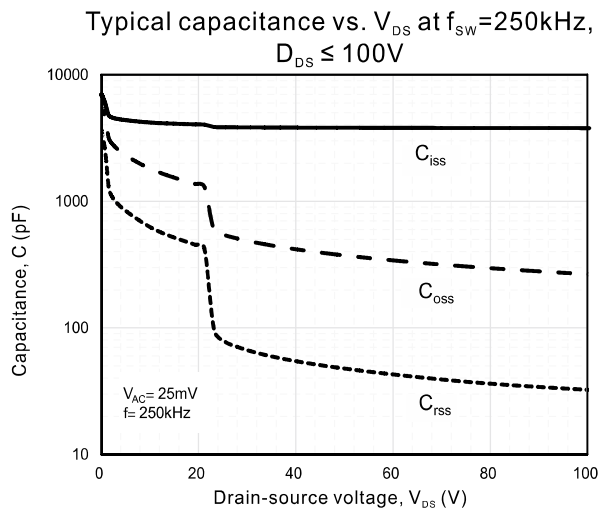
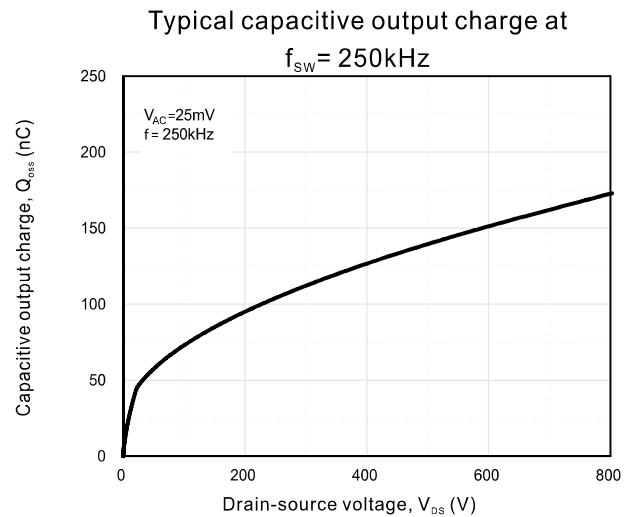
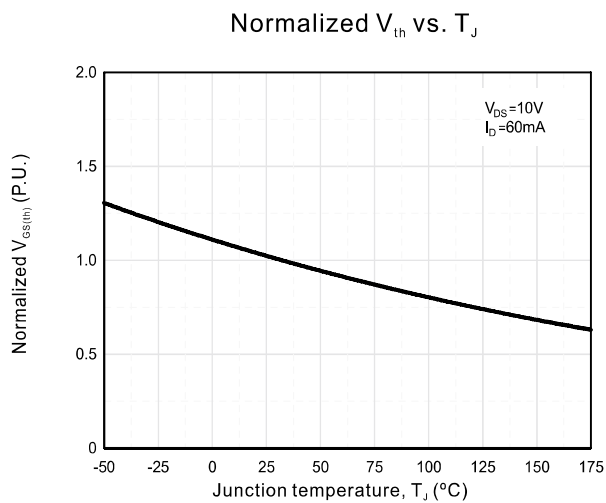
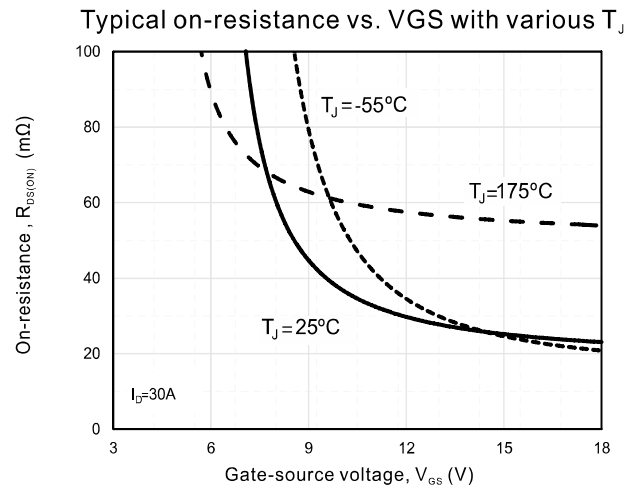
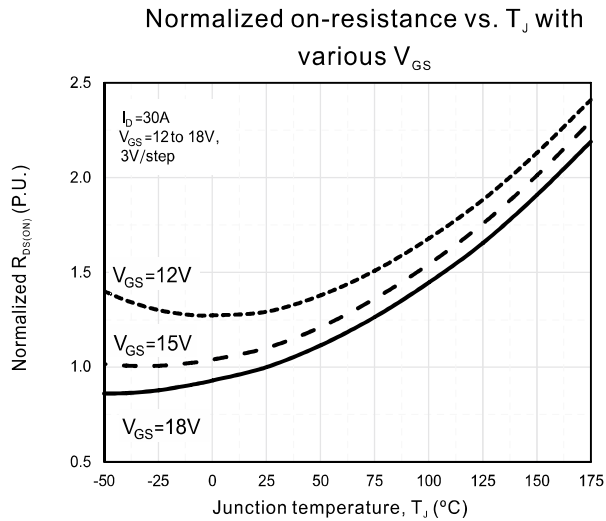
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Rating and characteristic curves

Typical output characteristics
at $T_J = 25^\circ\text{C}$ Typical output characteristics
at $T_J = 175^\circ\text{C}$ Typical output characteristics
at $T_J = -55^\circ\text{C}$ Typical on-resistance vs. Drain current with
various gate-source voltageTypical on-resistance vs. Drain current with
various T_J , $V_{GS} = 18\text{V}$ Typical drain current vs. Gate-source voltage with
various T_J , $V_{DS} = 10\text{V}$ 

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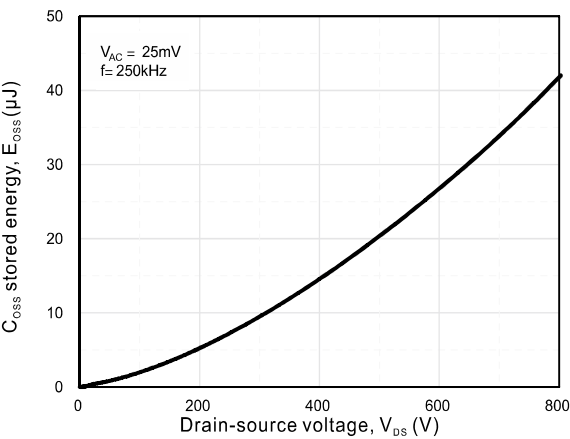
Rating and characteristic curves



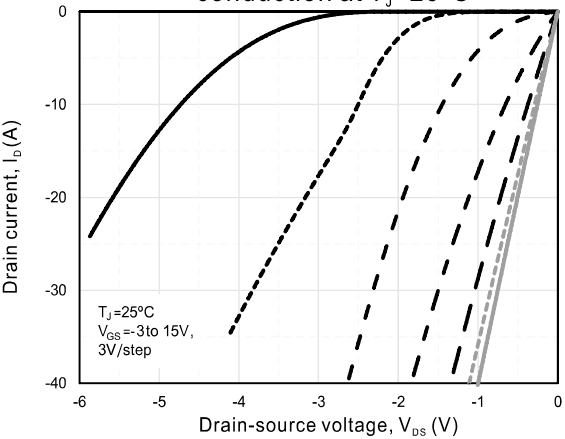
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Rating and characteristic curves

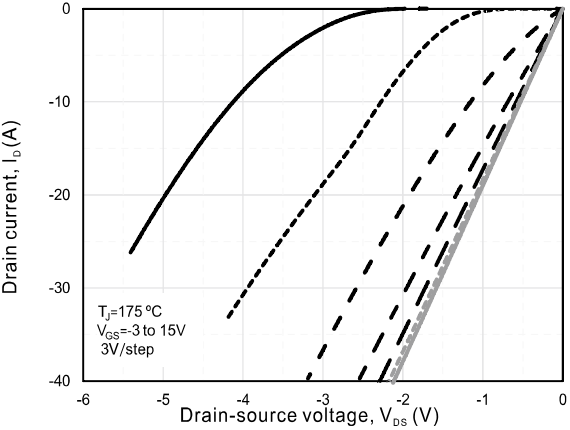
Typical C_{oss} stored energy at $f_{sw}=250kHz$



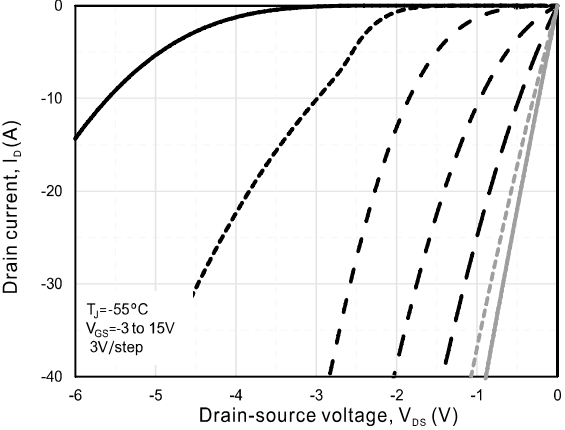
Typical forward characteristics of reverse conduction at $T_J=25^{\circ}C$



Typical forward characteristics of reverse conduction at $T_J=175^{\circ}C$



Typical forward characteristics of reverse conduction at $T_J=-55^{\circ}C$



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Pinning information

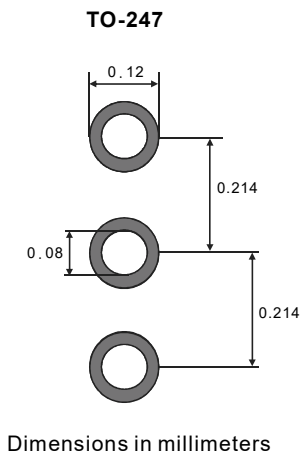
Pin	Simplified outline	Symbol
Pin 1 Gate Pin 2 Drain Pin 3 Source		

Marking

Type number	Marking code
FMOSCPW70N120-H	FMS CPW70N120 XXYYWW

*XXX: Lot ID or other information.
YYWW: Wafer lot code.
YY: Year
WW: Week

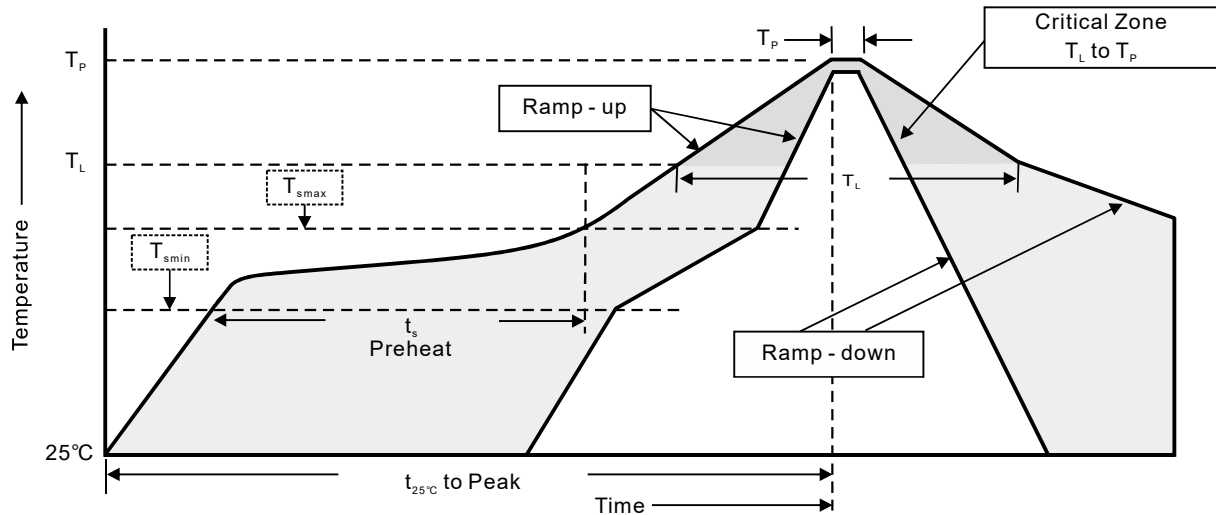
Suggested solder pad layout



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Suggested thermal profiles for soldering processes

1. Storage environment : Temperature = 5°C ~ 40°C, Humidity = 55%, ±25%.
2. Reflow soldering of surface - Mount devices.



3. Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_p)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C / sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_p)	255 °C -0 / +5°C
Time with 5°C of actual peak temperature (T_p)	10 ~ 30 sec
Ramp-down rate	< 6°C / sec
Time 25°C to peak temperature	< 6 minutes