

FMOSVDN3134E-Q1-H

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FMOSVDN3134E-Q1-H

0.75A 20V Dual N-Channel Enhancement Mode MOSFET ESD Protection

Features

- $V_{DS}=20V$, $I_D=0.75A$.
- $R_{DS(ON)} \leq 380m\Omega$, @ $V_{GS}=4.5V$, $I_D=0.65A$.
- $R_{DS(ON)} \leq 450m\Omega$, @ $V_{GS}=2.5V$, $I_D=0.55A$.
- $R_{DS(ON)} \leq 800m\Omega$, @ $V_{GS}=1.8V$, $I_D=0.45A$.
- N-channel switch with low on-resistance.
- Operated at low logic level gate drive.
- ESD protected.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21).

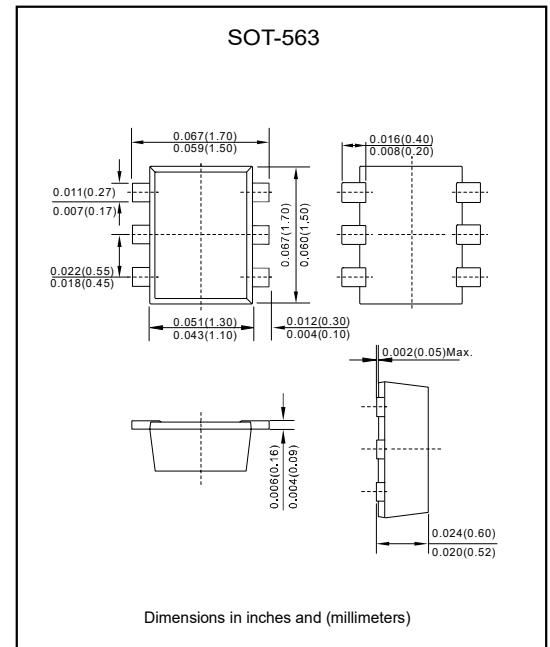
Application

- Load/ power switching and interfacing switching.
- Battery management for ultra small portable electronics.
- Logic level shift.

Mechanical data

- Epoxy: UL94-V0 rated flame retardant.
- Case : Molded plastic, SOT-563.
- Terminals : Solder plated, solder able per MIL-STD-750, Method 2026.
- Weight : Approximated 3mg.

Package outline



Maximum ratings (At $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	± 12	V
Continuous drain current ($t \leq 10s$)	I_D	0.75	A
Power dissipation (Note1)	P_D	0.15	W
Thermal resistance, junction to ambient	$R_{\theta JA}$	833	$^\circ C/W$
Junction temperature	T_J	+150	$^\circ C$
Storage temperature range	T_{STG}	-55 to +150	$^\circ C$

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Electrical characteristics (At $T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off characteristics						
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
Drain-source leakage current	I_{DSS}	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=\pm 10\text{V}$, $V_{DS}=0\text{V}$			± 20	μA

On characteristics

Gate threshold voltage (Note2)	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.35	0.54	1.10	V
Static drain-source on-state resistance (Note2)	$R_{DS(ON)}$	$V_{GS}=4.5\text{V}$, $I_D=0.65\text{A}$		270	380	m Ω
		$V_{GS}=2.5\text{V}$, $I_D=0.55\text{A}$		320	450	
		$V_{GS}=1.8\text{V}$, $I_D=0.45\text{A}$		390	800	
Forward tranconductance (Note2)	g_{FS}	$V_{DS}=10\text{V}$, $I_D=0.8\text{A}$		1.6		S

Dynamic parameters (Note3)

Input capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=16\text{V}$, $f=1.0\text{MHz}$		79	120	pF
Out capacitance	C_{oss}			13	20	
Reverse transfer capacitance	C_{rss}			9	15	

Switching parameters (Note3)

Total gate charge	Q_g	$V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=7\text{A}$		20		nC
Gate-source charge	Q_{gs}			1		
Gate-drain charge	Q_{gd}			4		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $R_{GEN}=10\Omega$, $I_D=0.5\text{A}$		6.7		ns
Turn-on rise time	t_r			4.8		
Turn-off delay time	$t_{d(off)}$			17.3		
Turn-off fall time	t_f			7.4		

Source-drain diode ratings and characteristics

Diode forward voltage (Note2)	V_{SD}	$I_S=0.15\text{A}$, $V_{GS}=0\text{V}$			1.2	V
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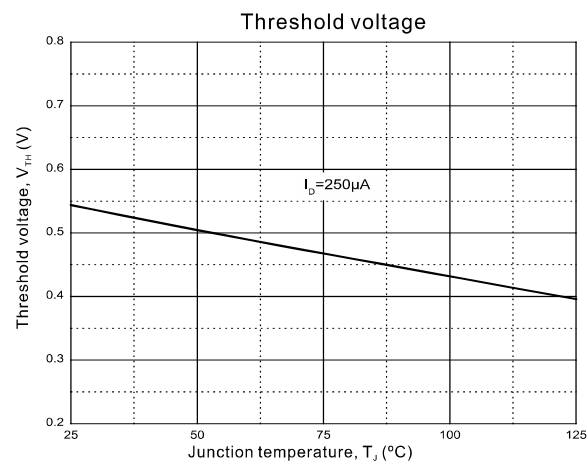
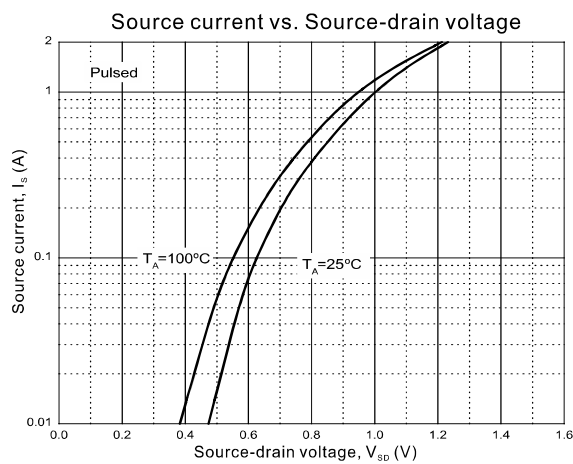
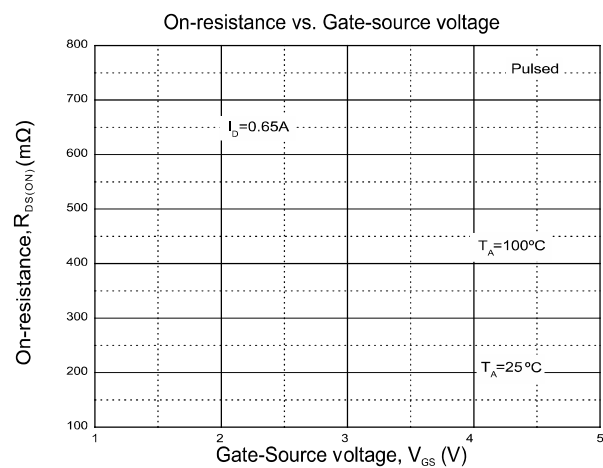
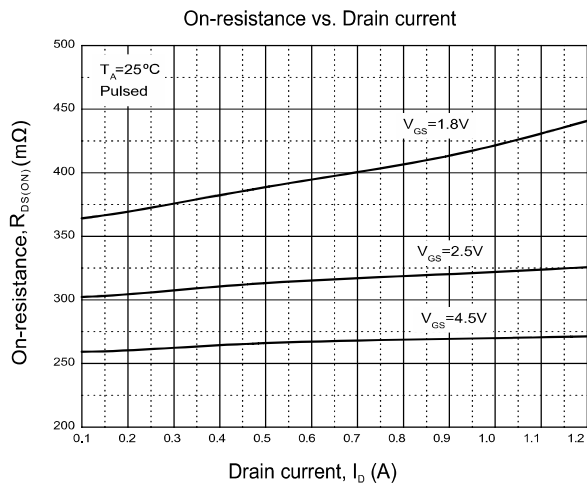
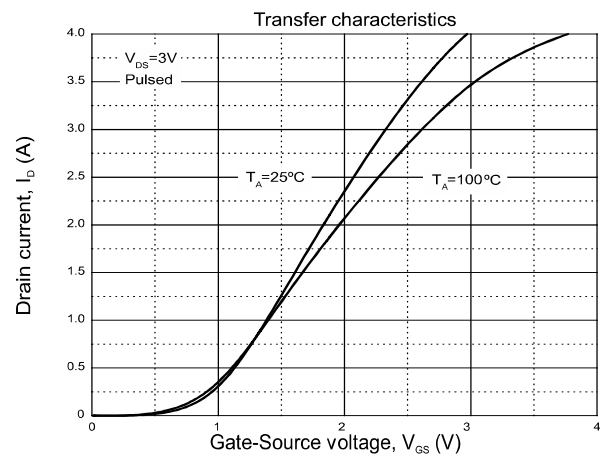
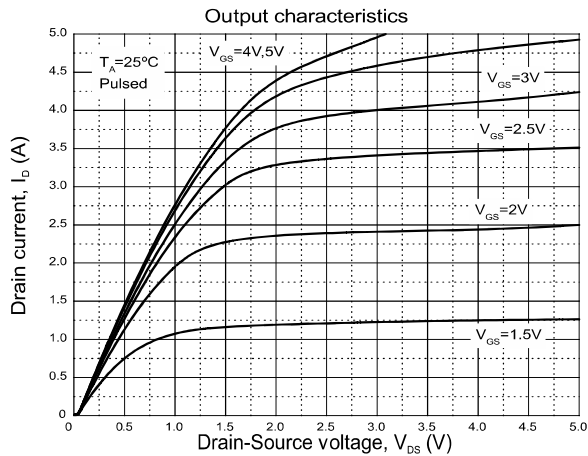
Note : 1. Repetitive rating: pulse width limited by junction temperature.

2. Pulse test : pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 0.5\%$.

3. Guaranteed by design, not subject to production testing.

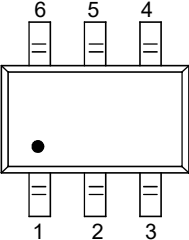
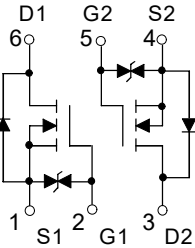
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Rating and characteristic curves



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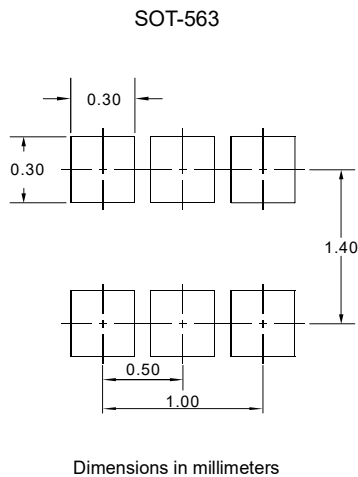
Pinning information

Pin	Simplified outline	Symbol
Pin1 Source1 Pin2 Gate1 Pin3 Drain2 Pin4 Source2 Pin5 Gate2 Pin6 Drain1		

Marking

Type number	Marking code
FMOSVDN3134E-Q1-H	34K

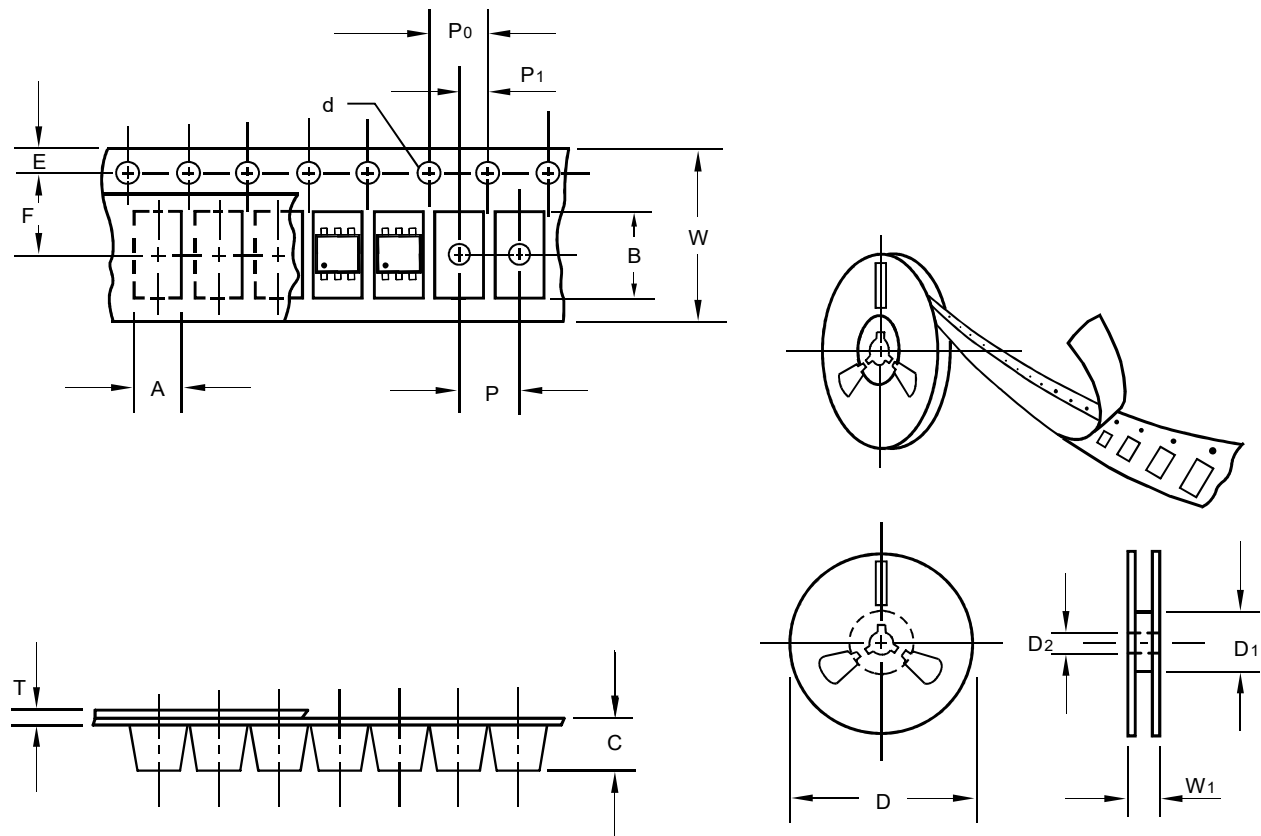
Suggested solder pad layout



- Note :
- 1. Controlling dimension : in millimeters.
 - 2. General tolerance : $\pm 0.05\text{mm}$.
 - 3. The pad layout is for reference purposes only.

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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-563
Carrier width	A	0.3	1.78
Carrier length	B	0.3	1.78
Carrier depth	C	0.3	0.69
Sprocket hole	d	0.3	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	54.00
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W1	3.0	12.10

Note:Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

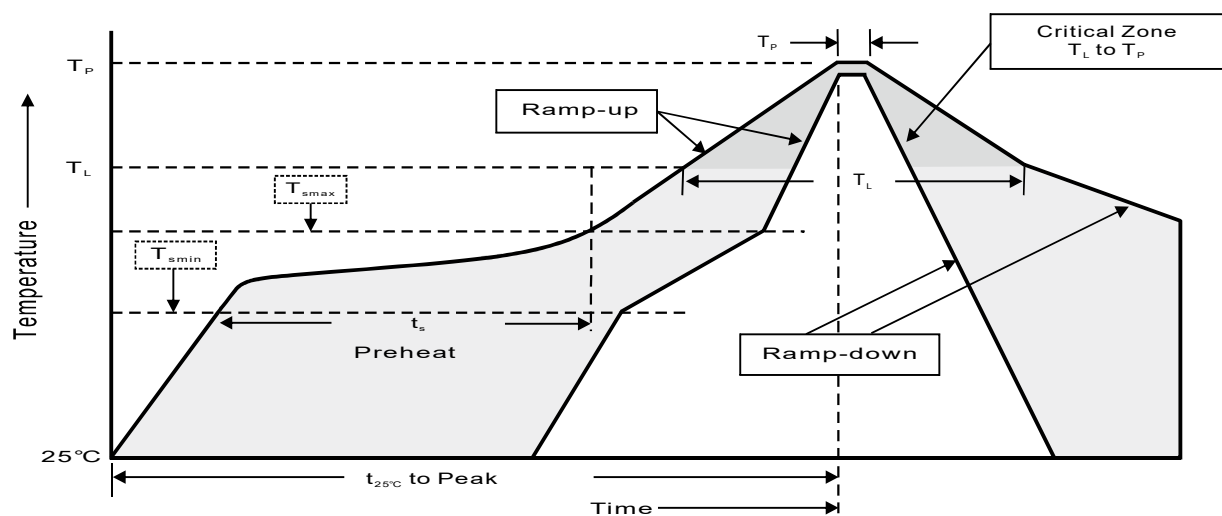
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Reel packing

TYPE NUMBER	PACKAGE	REEL SIZE	REEL (pcs)	REEL DIA, (m/m)
FMOSVDN3134E-Q1-H	SOT-563	7"	3,000	178

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_p)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_p)	255 °C -0/+5°C
Time with 5°C of actual peak temperature (T_p)	10 ~30 sec
Ramp-down rate	< 6 °C/sec
Time 25°C to peak temperature	< 6 minutes