

FMOSTHAE2N7002E-Q1-H

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FMOSTHAE2N7002E-Q1-H

280mA 60V N-Channel Trench Enhancement Mode MOSFET ESD Protection

Features

- ESD protected 2kV HBM
- Low $R_{DS(on)}$
- Surface mount package
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements
- Halogen-free (IEC61249-2-21)

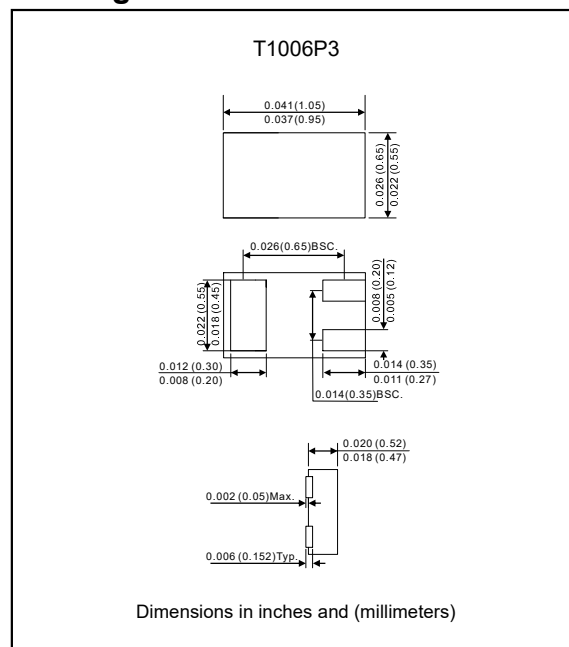
Applications

- Low side load switch
- Level shift circuits
- DC-DC converter
- Portable applications i.e. DSC, PDA, Cell phone, etc.

Mechanical data

- Epoxy: UL94-V0 rated flame retardant
- Case : Molded plastic, T1006P3
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any

Package outline



Maximum ratings (AT $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DS}	60	V
Drain current Steady state $T_A=25^{\circ}\text{C}$, $t < 5\text{s}$	I_D	280	mA
Pulsed drain current $t_p=10\mu\text{s}$	I_{DM}	1.5	A
Gate-source voltage	V_{GS}	± 20	V
Power dissipation (Note 1) Steady state $t < 5\text{s}$	P_D	300 420	mW
Source current (body diode)	I_S	300	mA
Lead temperature for soldering purposes (1/8" from case for 10s)	T_L	260	$^{\circ}\text{C}$
Gate-source ESD rating (HBM, Method)	ESD	2000	V
Thermal resistance junction to ambient steady (Note 1) Thermal resistance junction to ambient $t \leq 5\text{s}$ (Note 1)	$R_{\theta JA}$	417 300	$^{\circ}\text{C/W}$ $^{\circ}\text{C/W}$
Operation junction temperature range	T_J	-55 to +150	$^{\circ}\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^{\circ}\text{C}$

1. FR-4 = 1.0×0.75×0.062 in.

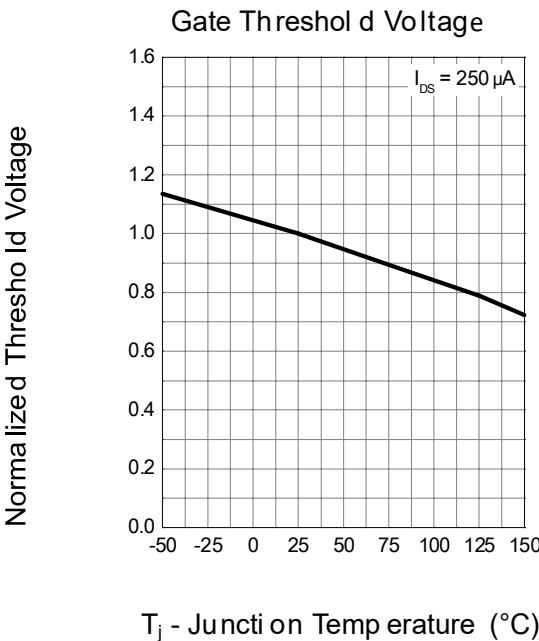
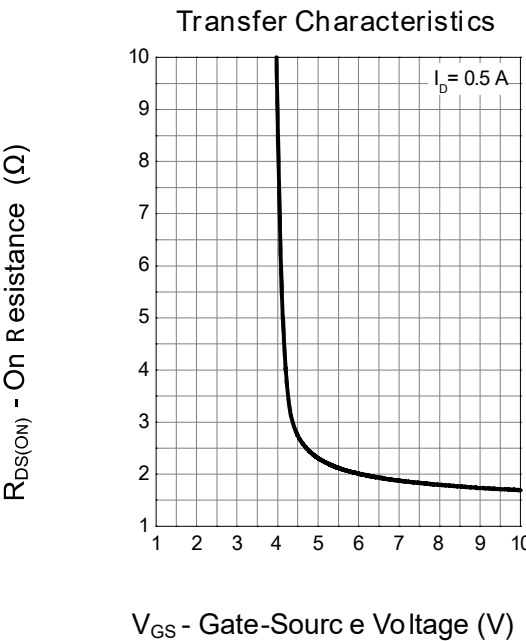
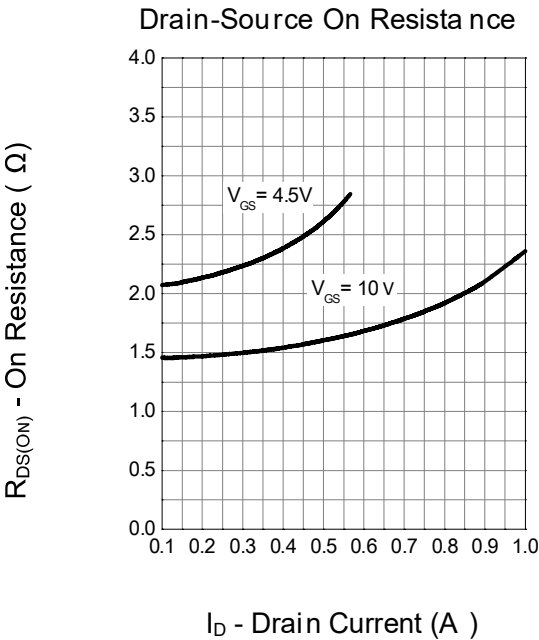
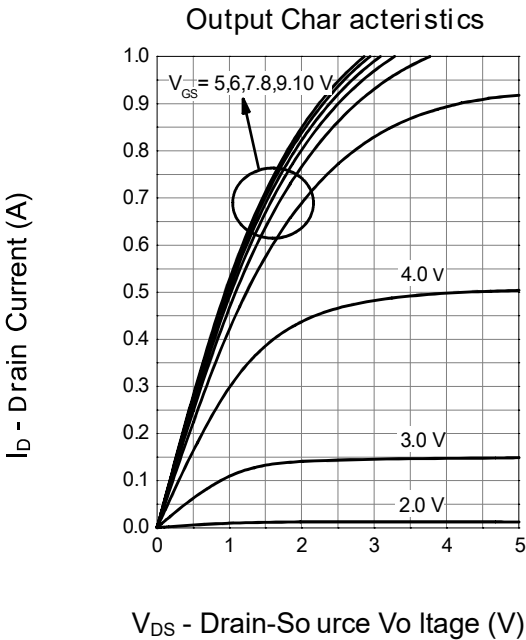
FMOSTHAE2N7002E-Q1-H**Electrical characteristics** (At $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	MIN.	TYP.	MAX.	Unit
OFF CHARACTERISTICS						
Drain-source breakdown voltage	VGS=0V, ID=250μA	V(BR)DSS	60			V
Drain-to-source breakdown voltage temperature coefficient		V(BR)DSS/TJ		71		mV/°C
Zero gate voltage drain current	VDS=60V,VGS=0V,TJ=25°C VDS=60V,VGS=0V,TJ=125°C VDS=50V,VGS=0V,TJ=25°C	IDSS			1.0 500 100	μA μA nA
Gate-body leakage current	VGS=±20V, VDS=0V	IGSS			±10	μA
ON CHARACTERISTICS (Note 2)						
Gate threshold voltage	VDS=VGS, ID=250μA	VGS(th)	1.0		2.2	V
Negative threshold temperature coefficient		VGS(th)/TJ		4.0		mV/°C
Drain-source on-resistance	VGS=10V, ID=500mA VGS=4.5V, ID=200mA	RDS(on)			2.8 3.2	Ω
Forward tranconductance	VDS=5.0V, ID=200mA	gFS	80			mS
DYNAMIC CHARACTERISTICS						
Input capacitance	VDS=25V,VGS=0V,f=1MHz	Ciss		21		pF
Output capacitance		Coss		12		
Reverse transfer capacitance		Crss		0.35		
Total gate charge	VDS=10V,VGS=4.5V,ID=500mA	QG(TOT)		0.44		nC
Gate-to-source charge		QGS		0.20		
Gate-to-drain charge		QGD		0.10		
SWITCHING CHARACTERISTICS						
Turn-on delay time	VDS=30V, VGEN=10V,ID=500mA RG=25Ω ,RL=60Ω	td(on)		2.7		ns
Turn-on rise time		tr		2.5		
Turn-off delay time		td(off)		13		
Turn-off fall time		trf		8		
BODY-DRAIN DIODE RATINGS						
Diode forward on-voltage	IS=0.5A,VGS=0V	VSD		0.85		V

2. Pulse Test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

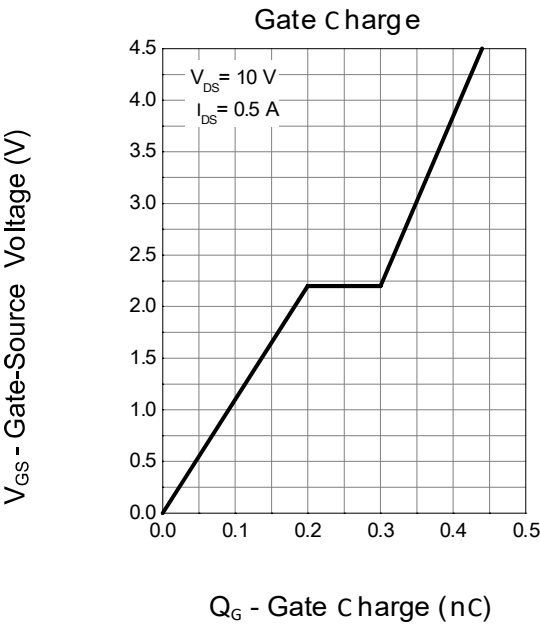
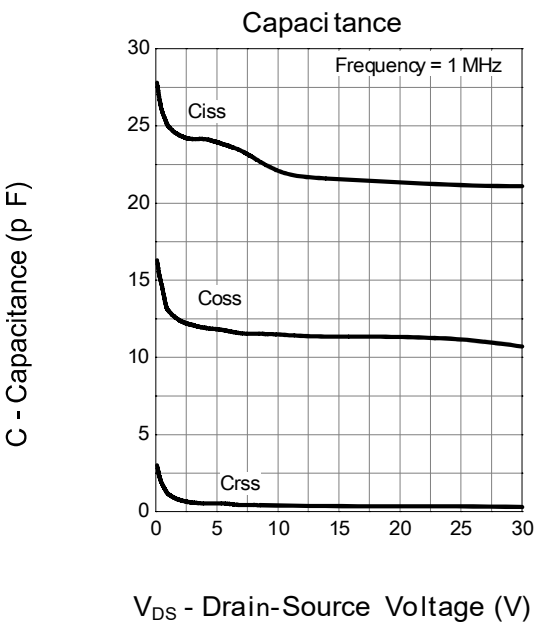
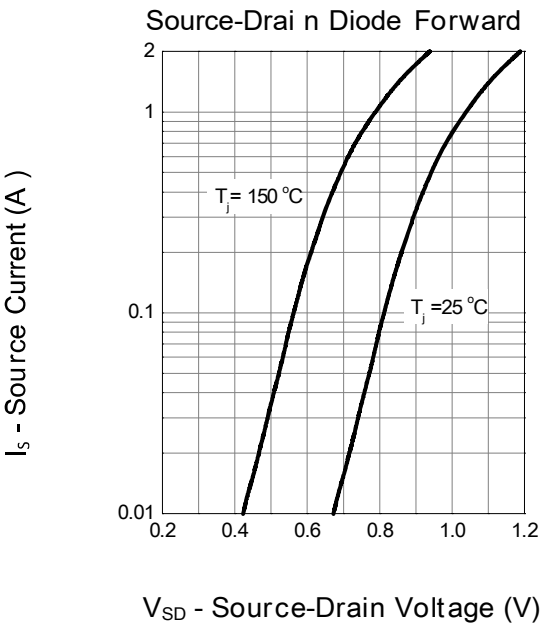
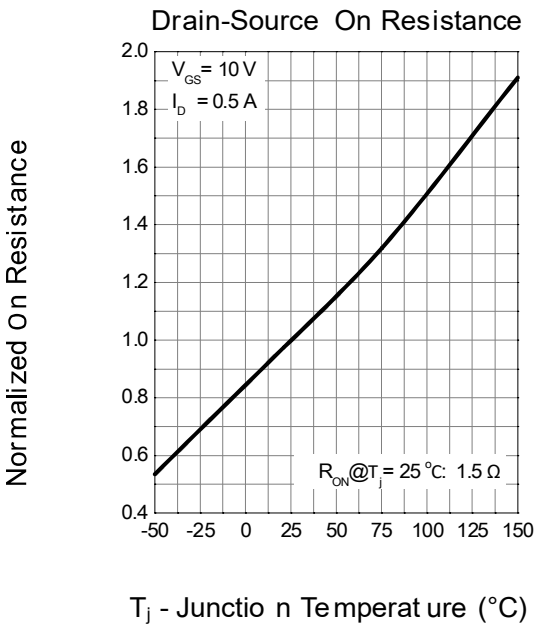
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Rating and characteristic curves



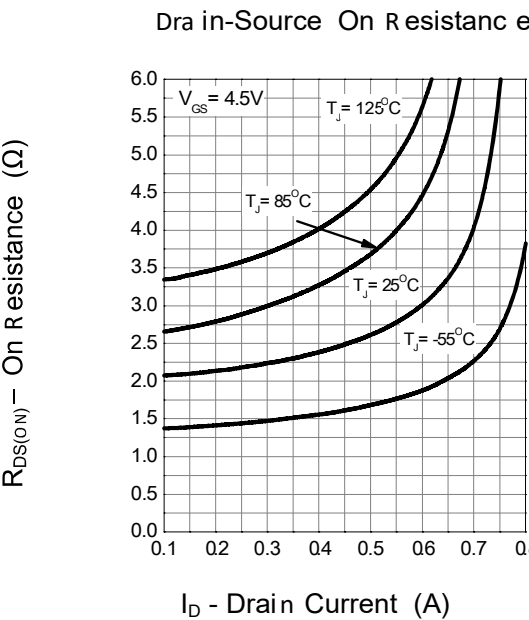
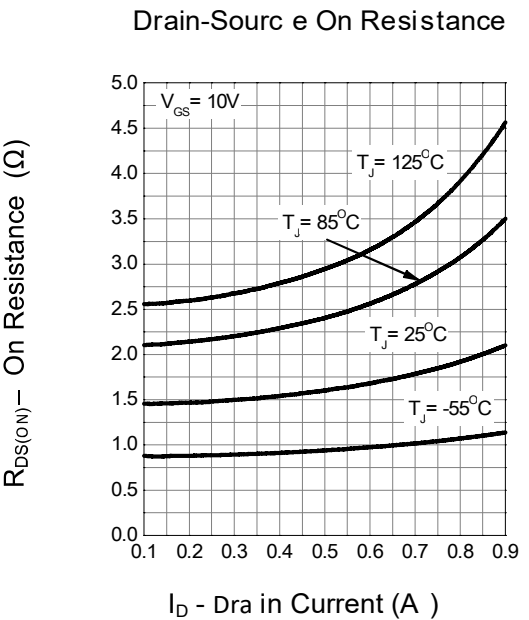
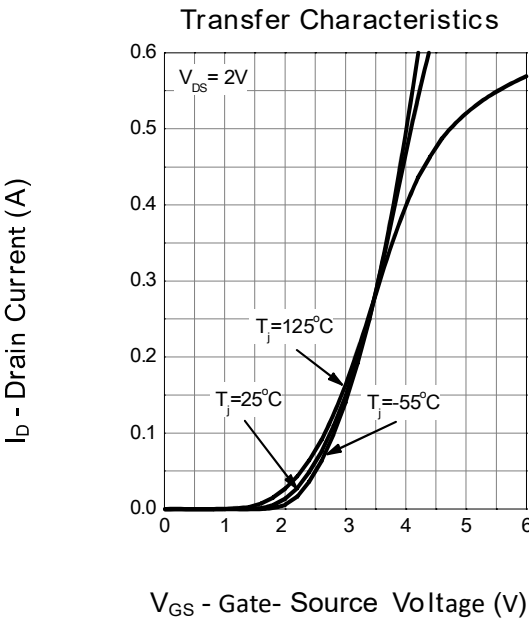
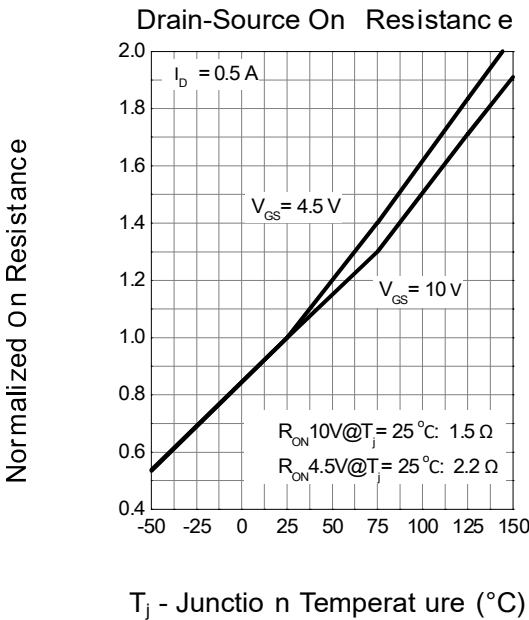
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Rating and characteristic curves



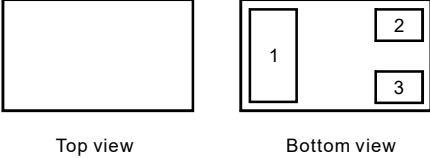
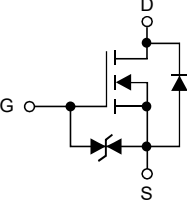
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Rating and characteristic curves



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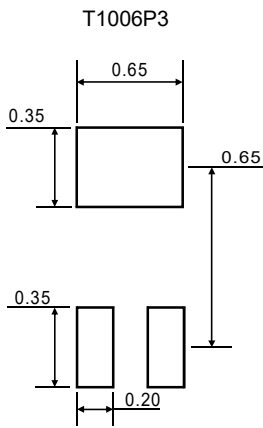
Pinning information

Pin	Simplified outline	Symbol
Pin 1 Drain Pin 2 Gate Pin 3 Source	 Top view Bottom view	

Marking

Type number	Marking code
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Suggested solder pad layout



DIMENSIONS: MILLIMETERS

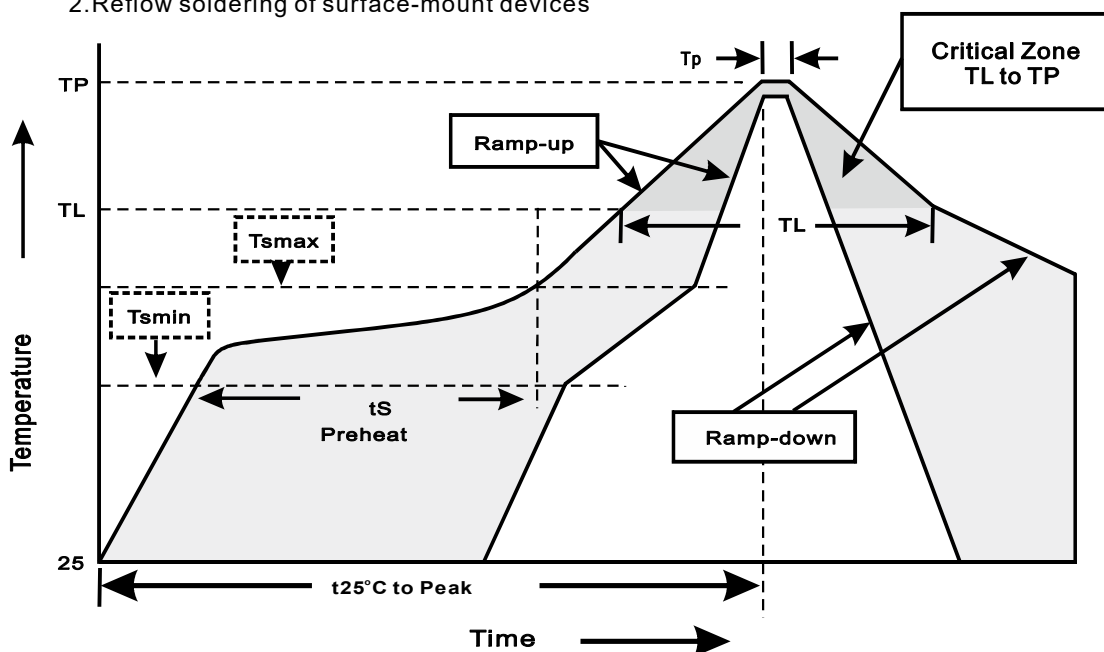
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
T1006P3	7"	10,000	4.0	100,000	210*210*205	178	445*445*230	400,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smín}) -Temperature Max(T _{smáx}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smáx} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _p)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes

FMOSTHAE2N7002E-Q1-H**High reliability test capabilities**

Item Test	Conditions	Reference
1. MSL Preconditioning	24hr bake@125°C+168hrs@85°C /85%RH+3xIR@260°C+1flux immersion+alcohol+DI H2O rinse	JESD22-A113
2. High Temperature Reverse Bias	$V_{DS}=V_{DS}^*80\%$ ($T_J=T_J \text{ max.}$) Test Duration:1000hrs	JESD22-A108
3. High Temperature Storage Life	$T_a=150^\circ\text{C}$ Test Duration:1000hrs	JESD22 A-103
4. Temperature Cycle	-55°C (15min) to 150°C (15min) Test Cycles:1000cycles	JESD22 A-104
5. Autoclave	$P=2\text{atm}$ $T_a=121^\circ\text{C}$ RH=100% Test Duration:96hrs	JESD22 A-102
6. Solderability	$245\pm5^\circ\text{C}$ for 5sec	J-STD-002
7. Moisture Resistance	$T_a=85^\circ\text{C}$ /85% Relative humidity Test Duration:1000hrs	MIL-STD-750E METHOD 1021.2
8. Resistance To Solder Heat	$260\pm5^\circ\text{C}$ for 10sec	JESD22 B-106
9. High Temperature High Humidity Reverse Bias	$T_a=85^\circ\text{C}$, 85%RH, $V_{DS}=80\%$ rated V_{DS} Test Duration: 1000hrs	JESD22-A101