

FMOSTHAC41N10-H

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FMOSTHAC41N10-H

41A 100V N-Channel Trench
Enhancement Mode Power MOSFET

Features

- $V_{DS} = 100V$, $I_D = 41A$.
- $R_{DS(ON)} \leq 15 m\Omega$, @ $V_{GS} = 10V$, $I_D = 12A$.
- $R_{DS(ON)} \leq 25 m\Omega$, @ $V_{GS} = 4.5V$, $I_D = 8A$.
- Optimized high performance of on-resistance and Gate charge.
- Reliable and rugged.
- 100% UIS and R_g tested.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21) .

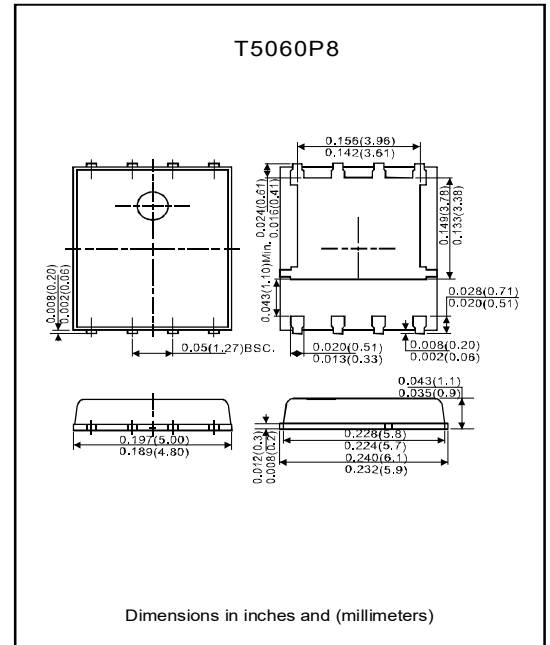
Applications

- DC/DC converters.
- Motor drivers.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, T5060P8 (DFN5060-8) .
- Weight : Approximated 105mg.

Package outline

Maximum ratings (At $T_j = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($T_c = 25^\circ C$) ($T_c = 100^\circ C$)	I_D	41	A
		26	
Pulsed drain current tested (Note 1)	I_{DM}	71	A
Avalanche current, single pulse (Note 2)	I_{AS}	10	A
Avalanche energy, single pulse (Note 2)	E_{AS}	5	mJ
Power dissipation ($T_c = 25^\circ C$) ($T_c = 100^\circ C$)	P_D	46	W
		19	
Thermal resistance, junction to ambient (Note 3) (Steady state)	$R_{\theta JA}$	50	$^\circ C/W$
Thermal resistance, junction to case (Steady state)	$R_{\theta JC}$	2.7	$^\circ C/W$
Operating Junction temperature	T_j	+150	$^\circ C$
Storage temperature range	T_{STG}	-55 to +150	$^\circ C$

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Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	BV_{DSS}	100			V
Drain-source leakage current	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$	I_{DSS}			1	μA
Gate-source leakage current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	I_{GSS}			± 100	nA

On characteristics

Gate threshold voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	$V_{GS(TH)}$	1	2	3	V
Static drain-source on-resistance (Note 4)	$V_{GS}=10\text{V}$, $I_D=12\text{A}$	$R_{DS(ON)}$		12.5	15	m Ω
	$V_{GS}=4.5\text{V}$, $I_D=8\text{A}$			19	25	
Forward trans conductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$	g_{FS}		22.8		S

Dynamic parameters (Note 5)

Input capacitance	$V_{GS}=0\text{V}$, $V_{DS}=50\text{V}$, $f=1.0\text{MHz}$	C_{iss}		1055		pF
Out capacitance		C_{oss}		182		
Reverse transfer capacitance		C_{rss}		5		
Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1.0\text{MHz}$	R_g		3		Ω

Switching parameters (Note 5)

Total gate charge	$V_{GS}=4.5\text{V}$, $V_{DS}=50\text{V}$, $I_D=12\text{A}$	Q_g		12.9		nC
				22.5		
Gate to source charge	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $I_D=12\text{A}$	Q_{gs}		3.2		
Gate to drain charge		Q_{gd}		7.6		
Turn-on delay time	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $R_G=3\Omega$, $I_D=1\text{A}$	$t_{d(on)}$		6		nS
Rise time		t_r		15		
Turn-off delay time		$t_{d(off)}$		16		
Fall time		t_f		25		

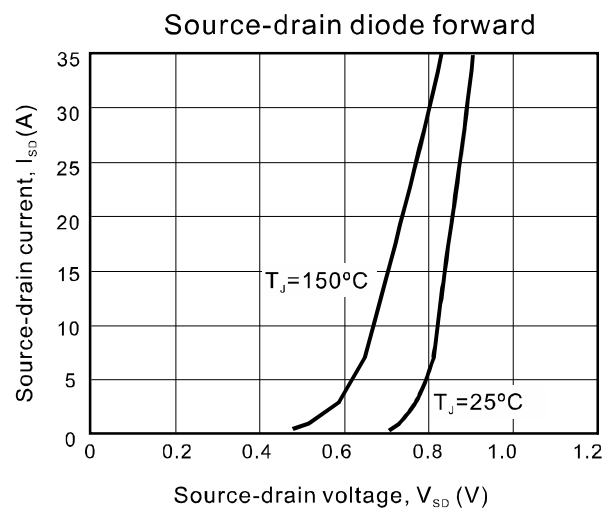
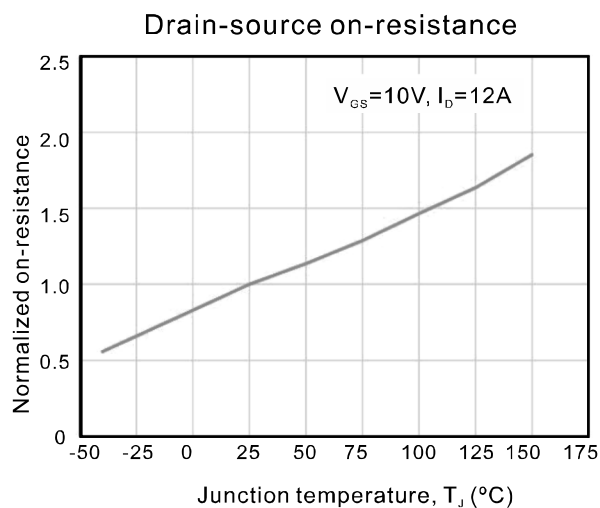
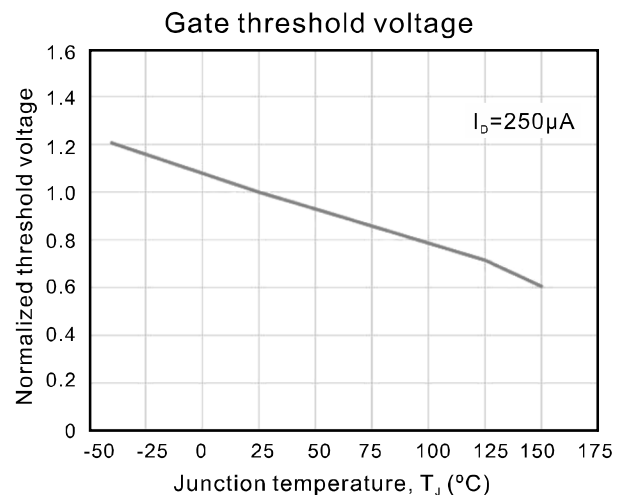
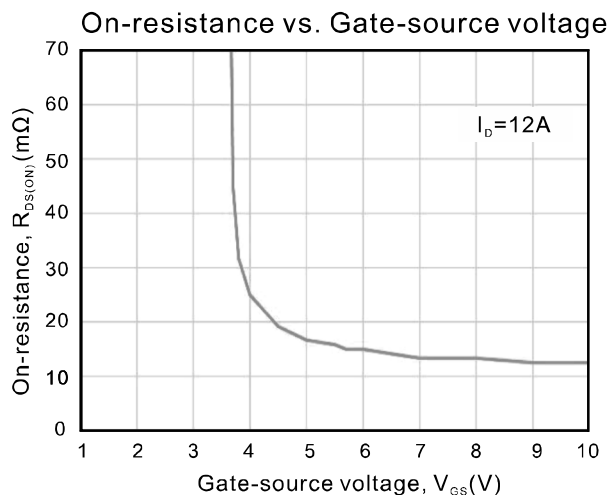
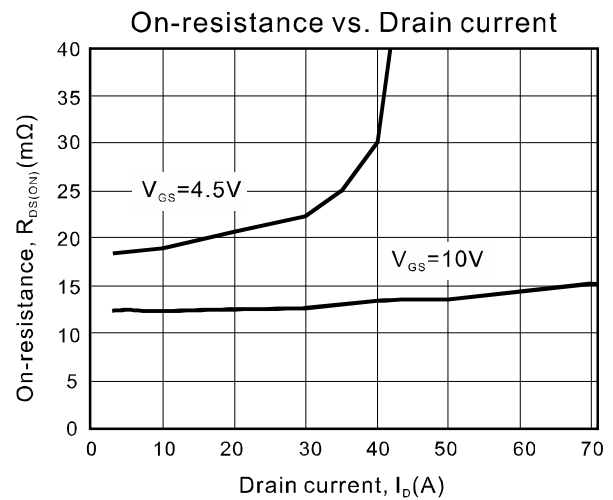
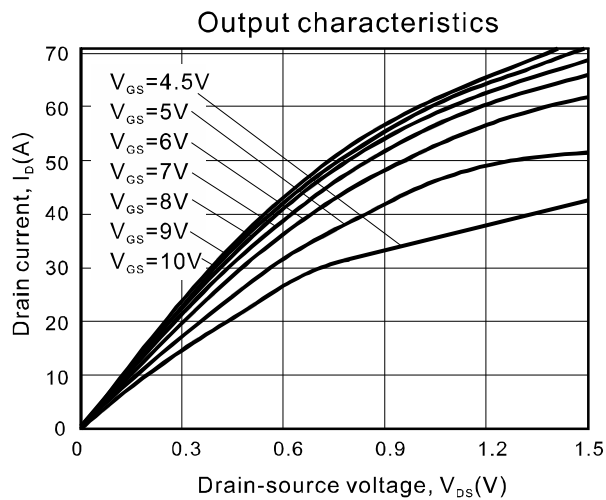
Source-drain diode ratings and characteristics

Drain-source diode forward voltage (Note 4)	$I_{SD}=20\text{A}$, $V_{GS}=0\text{V}$	V_{SD}		0.85	1.1	V
Body diode reverse recovery time	$V_R=50\text{V}$, $I_F=20\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$	t_{rr}		40		nS
Body diode reverse recovery charge		Q_{rr}		58.9		nC

Note : 1.Maximum current is limited by bonding wire.
 2.UIS tested and pulse width are limited by maximum junction temperature 150°C .
 3.Surface mounted on 1in^2 FR-4 board with 1oz.
 4.Pulse test: pulse width $\leq 300\mu\text{A}$, duty cycle $\leq 2\%$.
 5.Guaranteed by design, not subject to production testing.

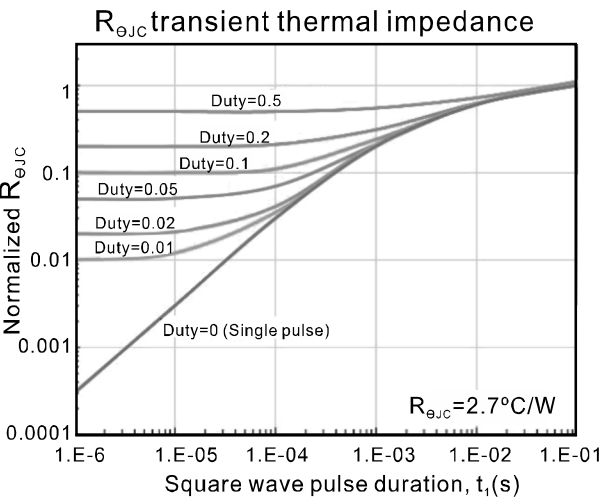
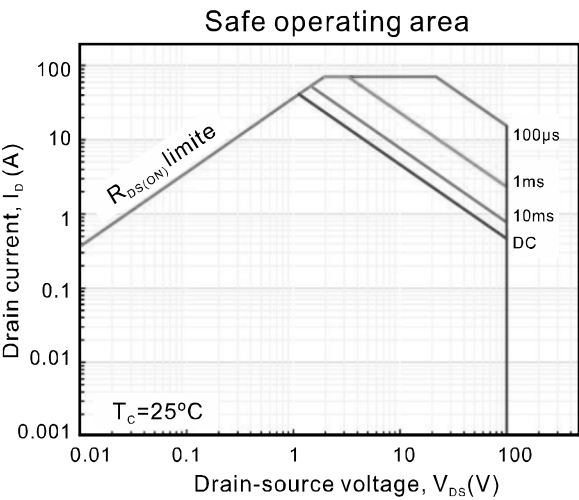
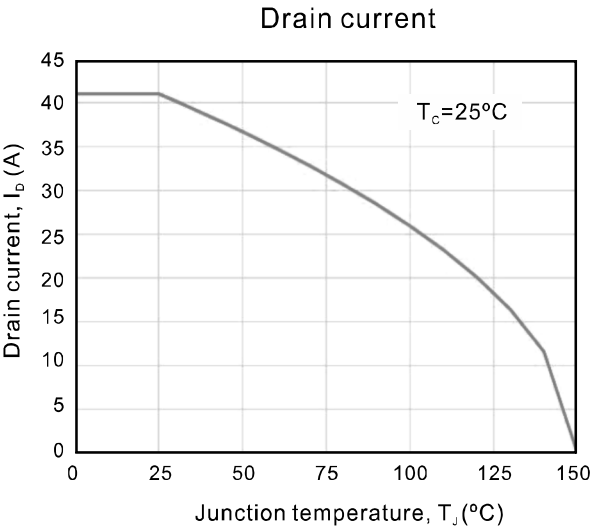
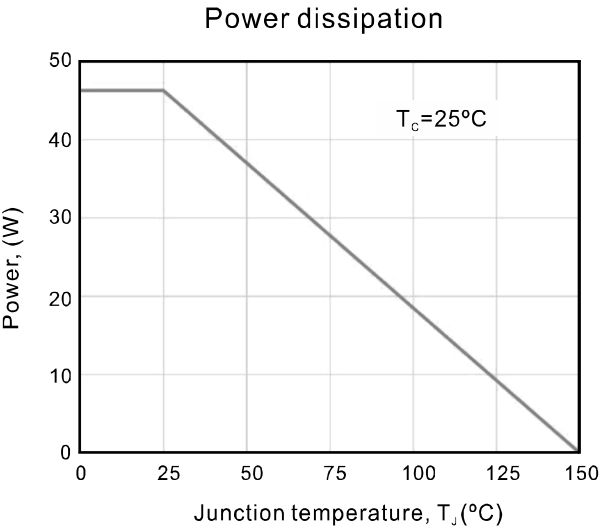
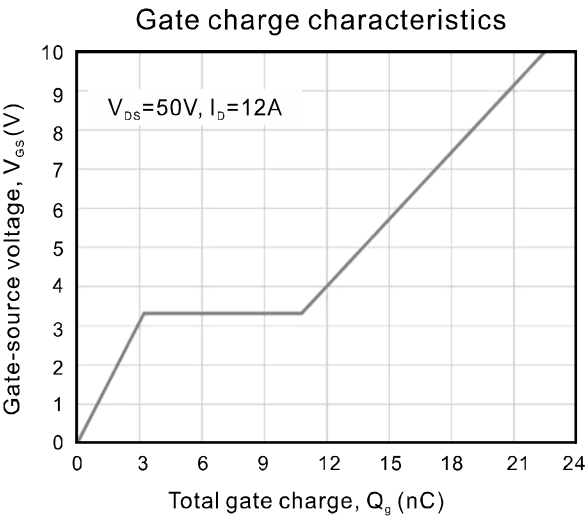
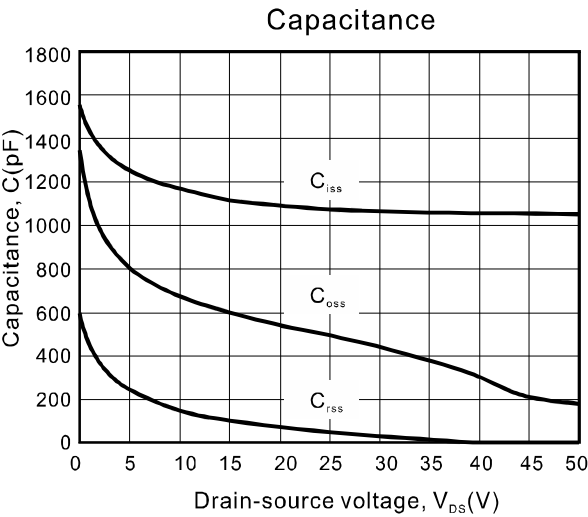
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Rating and characteristic curves



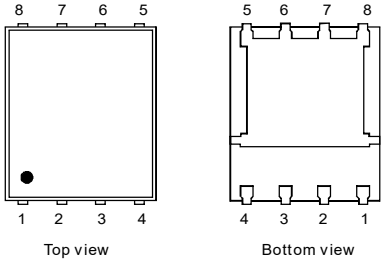
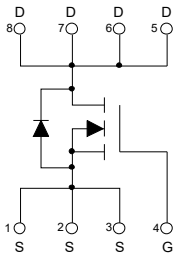
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Rating and characteristic curves

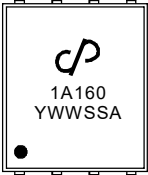


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Pinning information

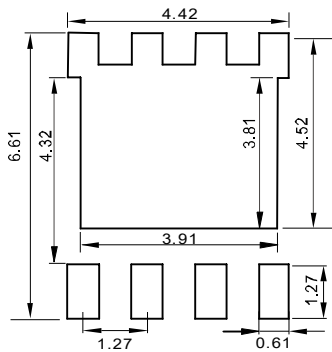
Pin	Simplified outline	Symbol
Pin 1, 2, 3 Source Pin 4 Gate Pin 5, 6, 7, 8 Drain	 Top view Bottom view	

Marking

Type number	Marking code
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* YWW: Wafer lot code
Y: Year
W: Week
SS: Sequence
A: Assy. code

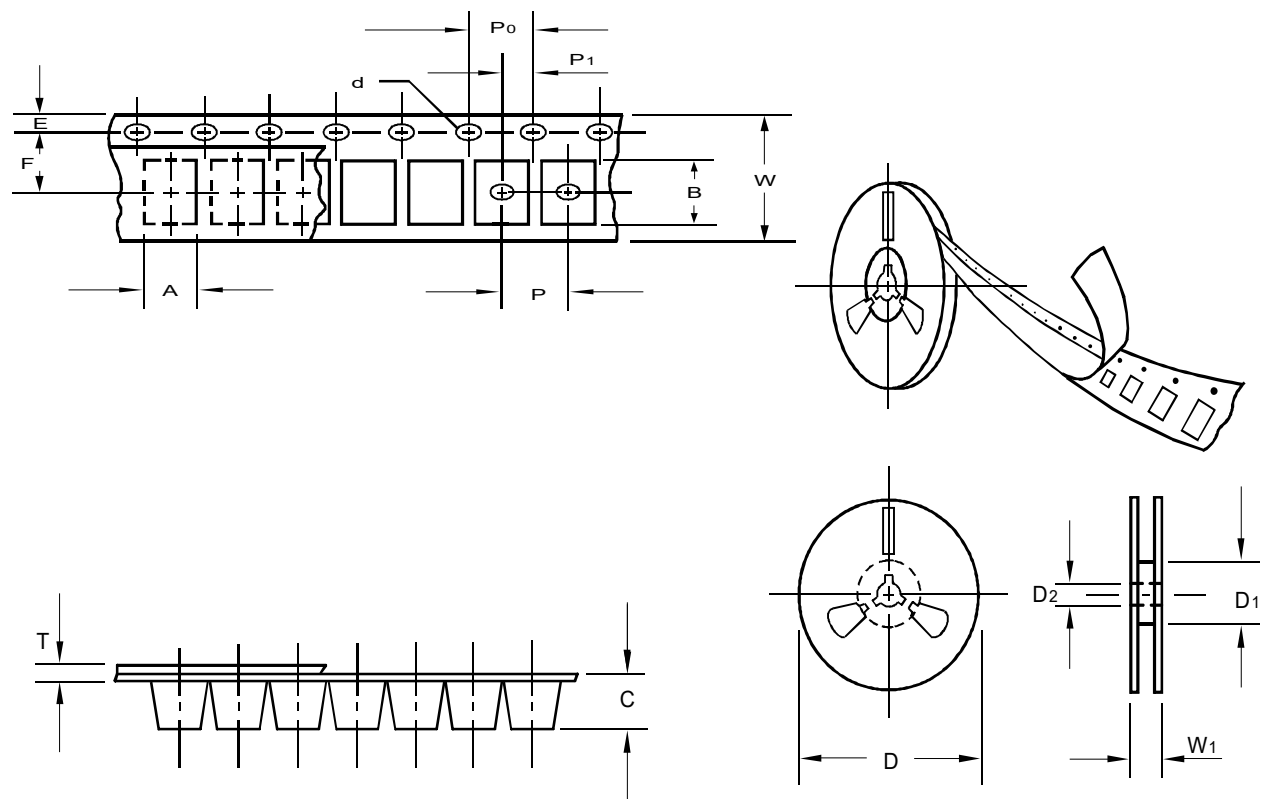
Suggested solder pad layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only.

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Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8
Carrier width	A	0.5	6.40
Carrier length	B	0.5	5.40
Carrier depth	C	0.5	1.25
Sprocket hole	d	0.5	1.55
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D1	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D1	min	-
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.5	0.30
Tape width	W	0.5	12.00
Reel width	W1	5.0	17.60

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

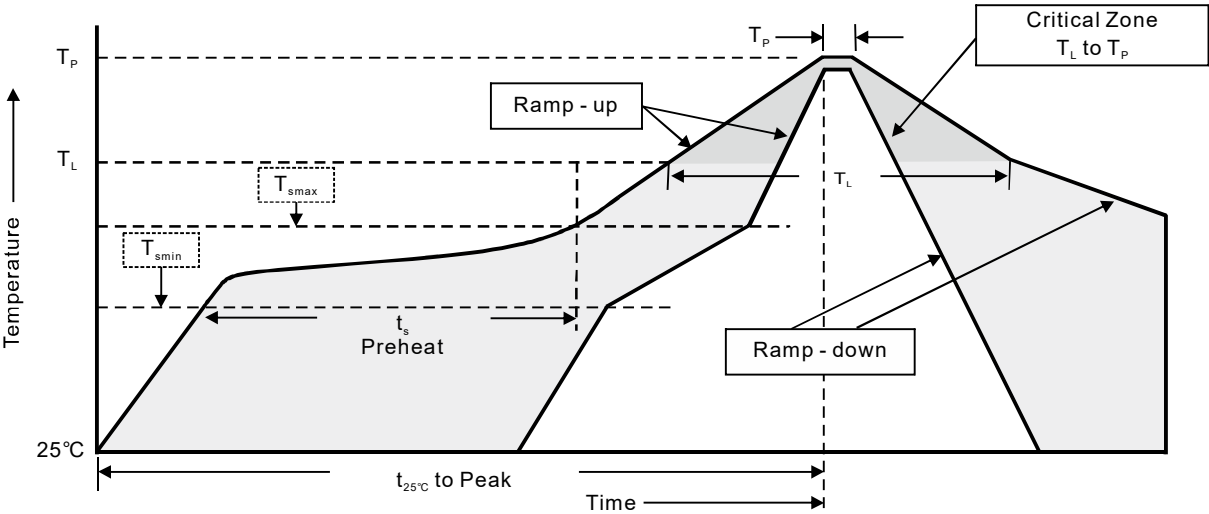
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Reel packing

Device	Outline	Device Package	Reel Size	Reel (pcs)
FMOSTHAC41N10-H	Taping	T5060P8	13 inch	5,000

Suggested thermal profiles for soldering processes

1. Storage environment : Temperature = 5°C ~ 40°C, Humidity = 55%, ±25%.
2. Reflow soldering of surface - Mount devices.



3. Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_P)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C / sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_P)	255 °C -0 / +5°C
Time with 5°C of actual peak temperature (T_P)	10 ~ 30 sec
Ramp-down rate	< 6°C / sec
Time 25°C to peak temperature	< 6 minutes