

FMOSTHAC212N06-H**List**

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FMOSTHAC212N06-H

212A 60V N-Channel Trench
Enhancement Mode Power MOSFET

Features

- $V_{DS}=60V$, $I_D=212A$.
- $R_{DS(ON)} \leq 1.6m\Omega$, @ $V_{GS}=10V$, $I_D=20A$.
- Low on-resistance.
- Excellent FOM.
- 100% UIS and R_g tested.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21).

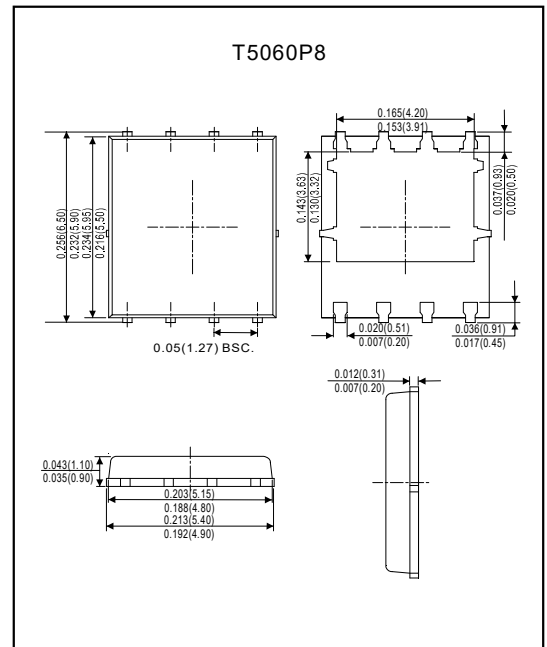
Application

- Load Switching.
- Motor driver.
- High frequency switching and synchronous rectification.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Moisture Sensitivity: Level 1 per J-STD-020.
- Case : Molded plastic, T5060P8.
- Mounting Position : Any.

Package outline

Maximum ratings (AT $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Ratings	Units
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current, @ $V_{GS}=10V$ (Note1)	I_D	212	A
($T_c=100^{\circ}C$)		134	
Pulsed drain current (Note2)	I_{DM}	849	A
Avalanche current ($L=0.1mH$)	I_{AS}	70	A
Avalanche energy (Note3)	E_{AS}	740	mJ
Power dissipation	P_D	125	W
($T_c=100^{\circ}C$)		50	
Thermal resistance junction to ambient (Note 4)	$R_{\theta JA}$	42	$^{\circ}C/W$
Thermal resistance junction to case (Note 5)	$R_{\theta JC}$	1	$^{\circ}C/W$
Operation junction temperature	T_J	+150	$^{\circ}C$
Storage temperature range	T_{STG}	-55 to +150	$^{\circ}C$

Notes :

1. This current is chip limited, which is calculated based on $R_{\theta JC}$.
2. This current is calculated on single pulse with 10 μs Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^{\circ}C$, $V_{DD}=30V$, $V_{GS}=10V$, $L=1.0mH$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

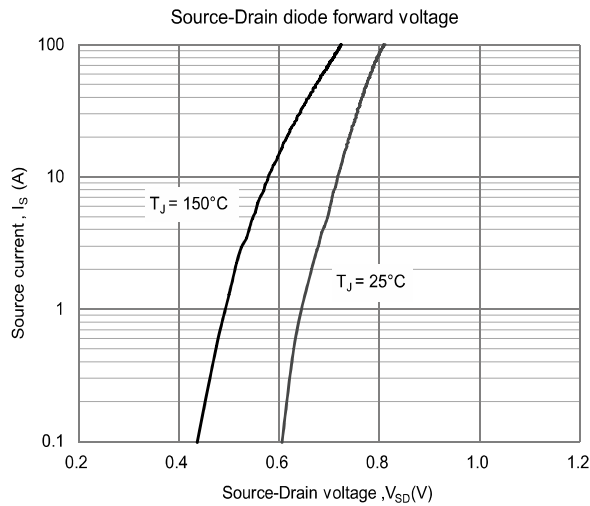
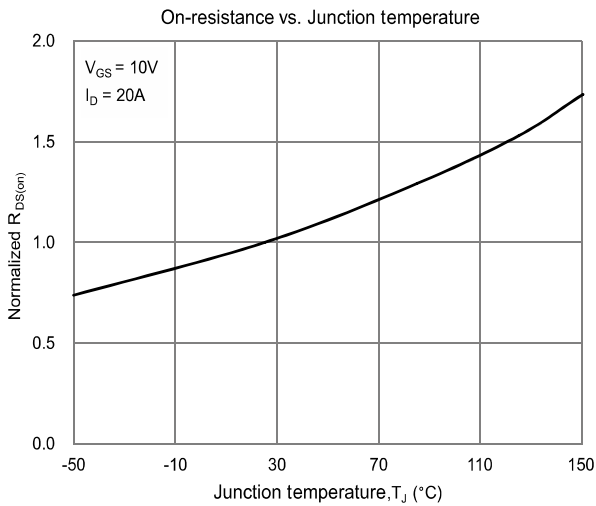
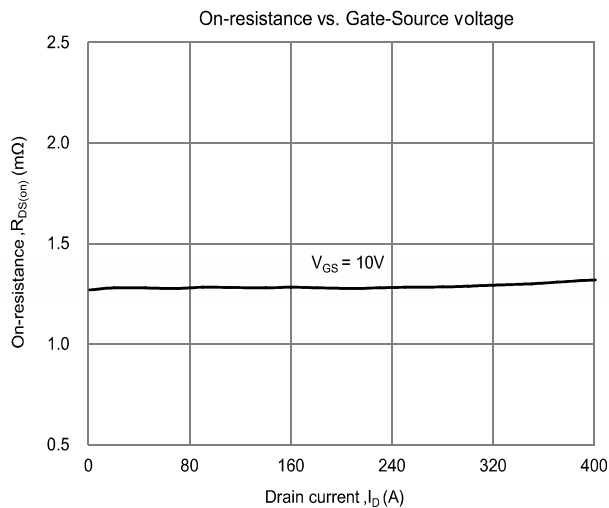
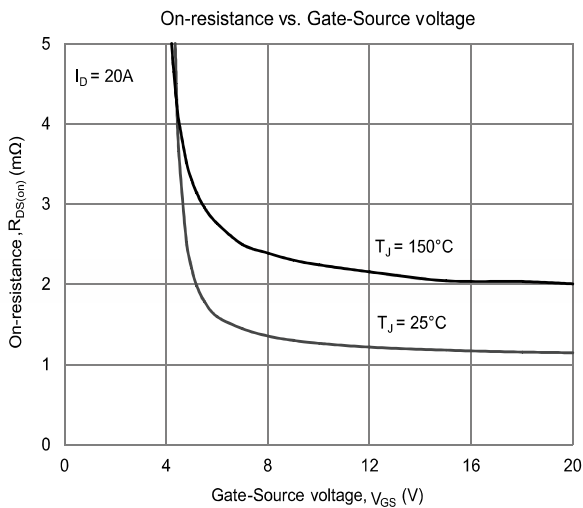
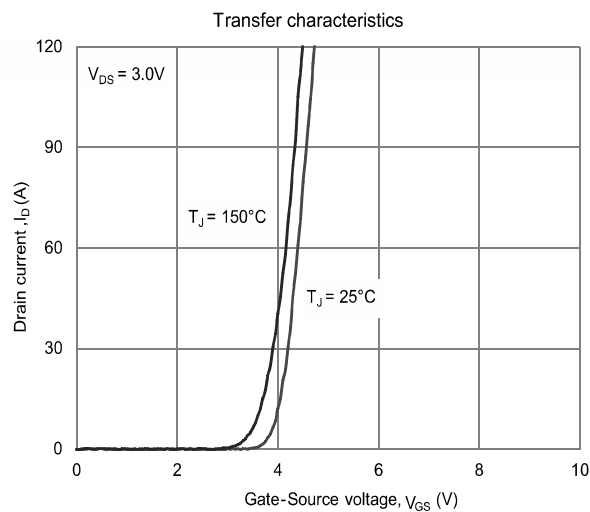
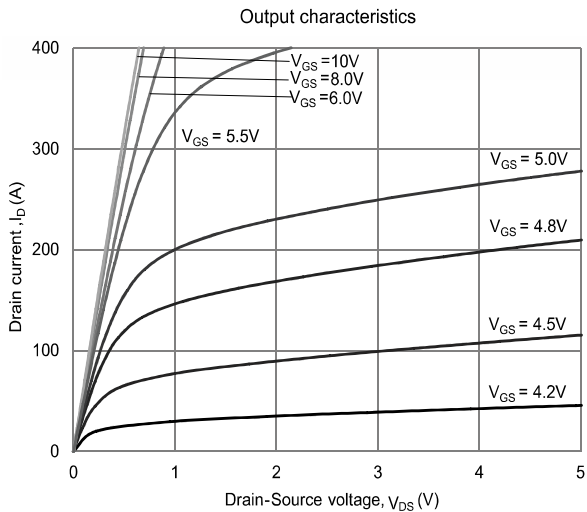
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Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Units
Off characteristics (Note 6)						
Drain-source breakdown voltage	$V_{GS} = 0V, I_D = 250\mu A$	$V_{(BR)DSS}$	60			V
Gate- source leakage current	$V_{DS} = 60V, V_{GS} = 0V$	I_{DSS}			1	μA
	$V_{DS} = 60V, V_{GS} = 0V, T_J=125^{\circ}C$				100	
Gate-body leakage current	$V_{DS} = 0V, V_{GS} = \pm 20V$	I_{GSS}			± 100	nA
On characteristics (Note 6)						
Gate threshold voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(th)}$	2	3	4	V
Drain-source on-resistance	$V_{GS} = 10V, I_D = 20A$	$R_{DS(on)}$		1.3	1.6	m Ω
Forward transconductance	$V_{DS} = 5V, I_D = 20A$	g_{FS}		68		S
Dynamic characteristics (Note 7)						
Input capacitance	$V_{DS} = 30V, V_{GS} = 0V, f = 1.0MHz$	C_{iss}		5483		pF
Output capacitance		C_{oss}		2514		
Reverse transfer capacitance		C_{rss}		98		
Gate resistance	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	R_g		1.8		Ω
Switching characteristics (Note 7)						
Total gate charge	$V_{GS} = 10V, V_{DS} = 30V, I_D = 20A$	Q_g		94		nC
	$V_{GS} = 6V, V_{DS} = 30V, I_D = 20A$			60		
Gate-source charge	$V_{GS} = 10V, V_{DS} = 30V, I_D = 20A$	Q_{gs}		25		
Gate-drain charge		Q_{gd}		23		
Gate plateau voltage		$V_{plateau}$		4.4		V
Turn-on delay time	$V_{DS} = 30V, V_{GS} = 10V, R_G = 3\Omega, I_D = 20A$	$t_{d(on)}$		8.5		nS
Turn-on rise time		t_r		18		
Turn-off delay time		$t_{d(off)}$		65		
Turn-off fall time		t_f		28		
Drain-source diode characteristics (Note 7)						
Drain-source diode forward voltage	$I_S = 2.0A, V_{GS} = 0V$	V_{SD}		0.7	1.2	V
Continuous drain-source diode forward current	$T_C = 25^{\circ}C$	I_S			212	A
Body diode reverse recovery time	$I_F = 20A, dI/dt = 100A/\mu s, T_J = 25^{\circ}C$	t_{rr}		66		nS
Body diode reverse recovery charge		Q_{rr}		131		nC

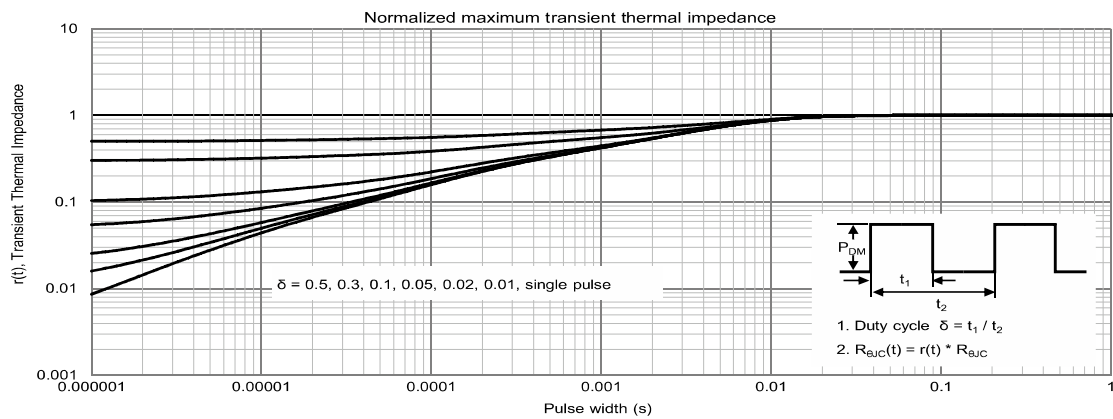
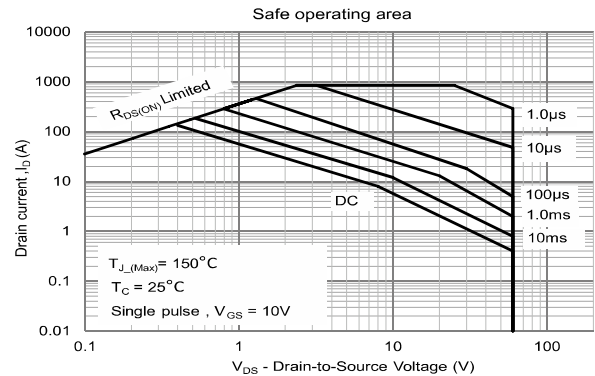
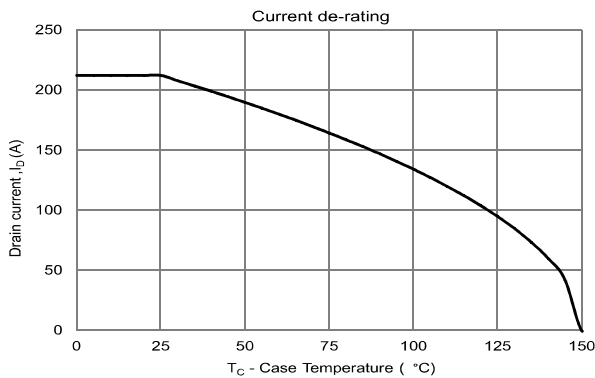
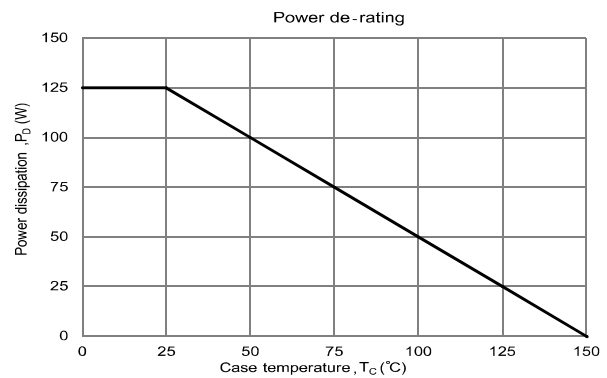
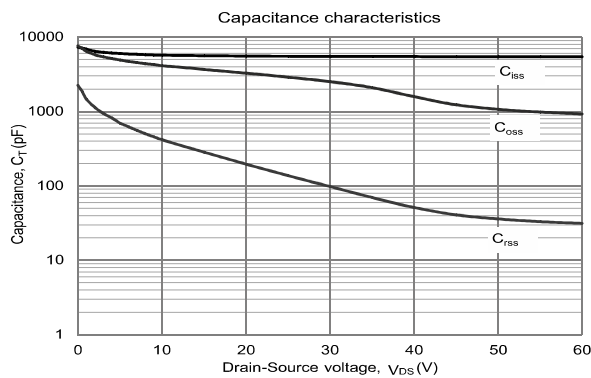
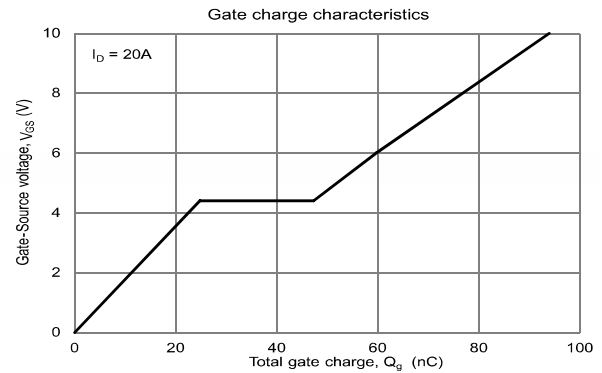
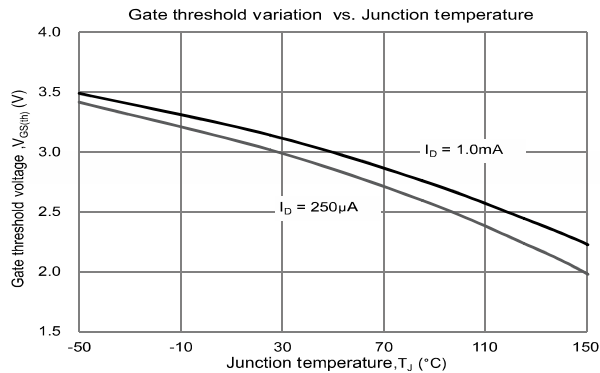
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Rating and characteristics curves



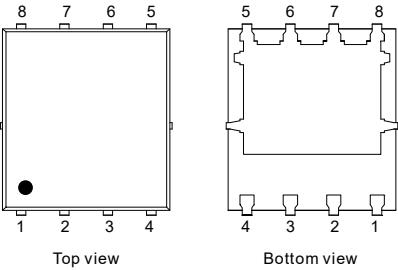
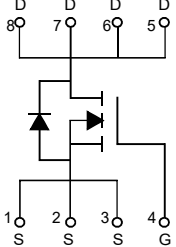
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Rating and characteristics curves



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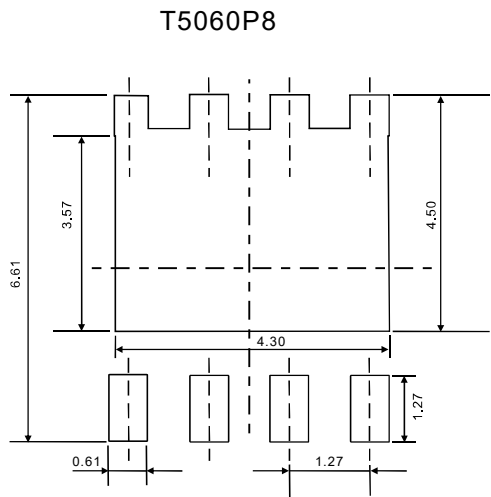
Pinning information

Pin	Simplified outline	Symbol
Pin 1, 2, 3, Source Pin 4 Gate Pin 5, 6, 7, 8 Drain	 Top view Bottom view	

Marking

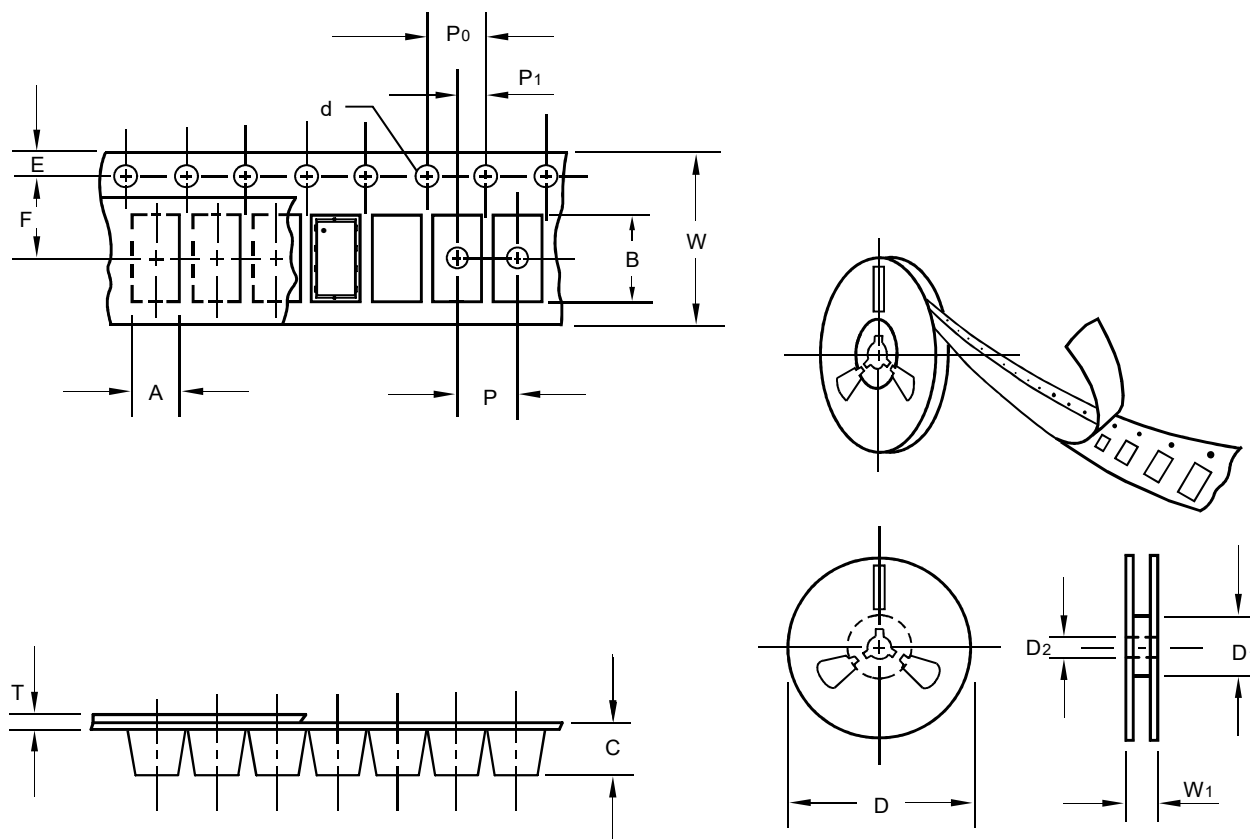
Type number	Marking code
FMOSTHAC212N06-H	AC212N06

Suggested solder pad layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.1\text{mm}$
3. The pad layout is for reference purposes only.

Packing information



Item	Symbol	Tolerance	T5060P8
Carrier width	A	0.1	6.40
Carrier length	B	0.1	5.40
Carrier depth	C	0.1	1.25
Sprocket hole	d	0.1	1.55
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D ₁	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D ₁	min	-
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.30
Tape width	W	0.3	12.00
Reel width	W ₁	1.0	17.60



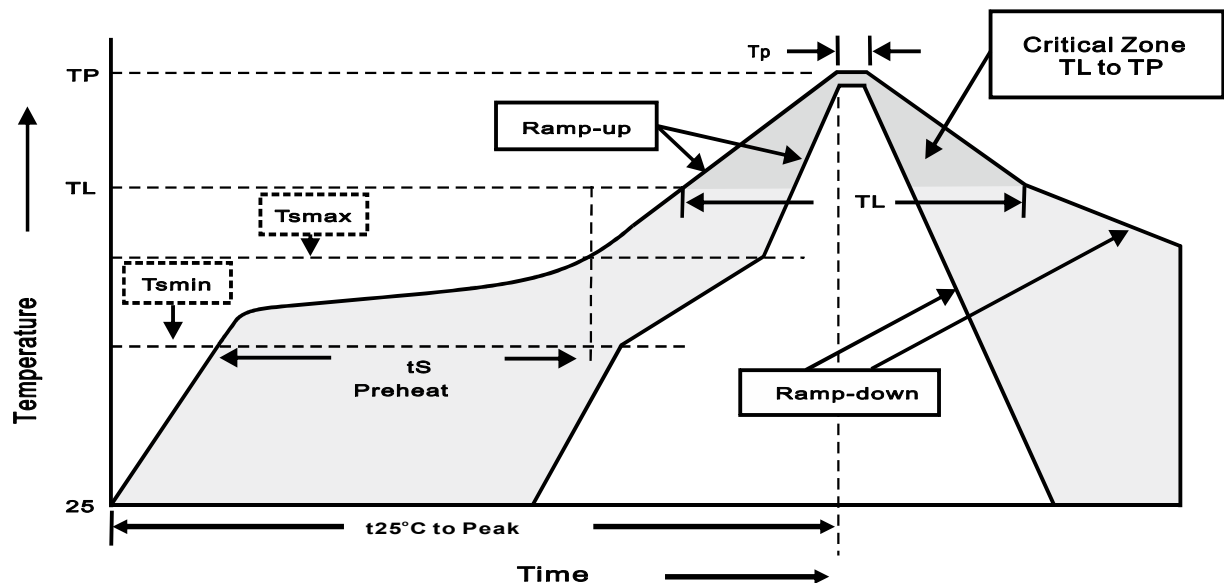
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Reel packing

Device	Outline	Package	Reel Size	Reel (PCS)
FMOSTHAC212N06-H	TAPING	T5060P8	13inch	5,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	$<3^\circ\text{C/sec}$
Preheat -Temperature Min(T_{smin}) -Temperature Max(T_{smax}) -Time(min to max)(t_s)	150°C 200°C 60~120sec
T_{smax} to T_L -Ramp-upRate	$<3^\circ\text{C/sec}$
Time maintained above: -Temperature(T_L) -Time(t_L)	217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	$<3^\circ\text{C/sec}$
Time 25°C to Peak Temperature	$<6\text{minutes}$