

FMOSL02N10

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FMOSL02N10

2.1A 100V N-Channel Enhancement Mode Power MOSFET

Features

- $V_{DS} = 100V$, $I_D = 2.1A$.
- $R_{DS(ON)} < 126m\Omega$, @ $V_{GS} = 10V$, $I_D = 2A$.
- $R_{DS(ON)} < 169m\Omega$, @ $V_{DS} = 4.5V$, $I_D = 1A$.
- Low on-resistance and low gate charge.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen-free part, ex. FMOSL02N10-H.

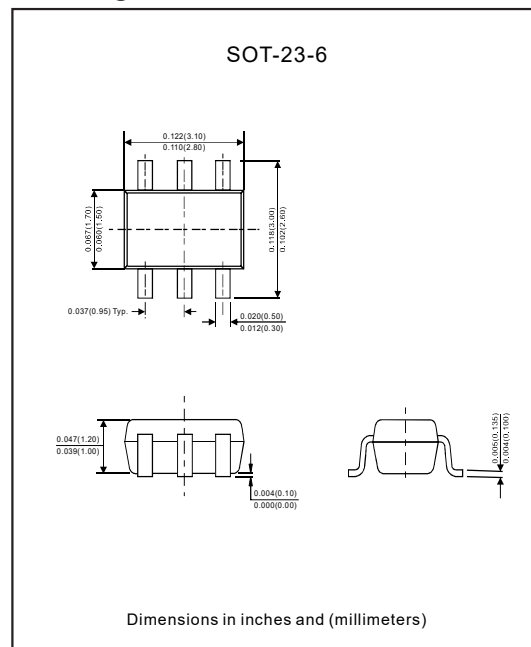
Applications

- Power management in mobile computing, CE, industrial automation.
- Load switching in LED lighting and backlight.
- Current switching in DC/DC (buck or boost), point-of-load(PoL).

Mechanical data

- Epoxy : UL94-V0 rated flame retardant.
- Case : Molded plastic, SOT-23-6.
- Terminals : Solder plated, solderable per MIL-STD750, Method 2026.
- Mounting Position : Any.

Package outline



Maximum Ratings (At $T_A = 25^\circ C$ Unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Drain current continuous (Note 1)	I_D	2.1	A
		1.7	
Pulsed drain current (Note 2)	I_{DM}	20	A
Avalanche current (Note 3)	I_{AS}	4.3	A
Avalanche energy (Note 3)	E_{AS}	0.9	mJ
Power dissipation (Note 4)	P_D	1.0	W
		0.6	
Thermal resistance junction to ambient	$R_{\theta JA}$	125	$^\circ C/W$
Operating junction temperature	T_J	+150	$^\circ C$
Storage temperature range	T_{STG}	-55 to +150	$^\circ C$

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Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise specified)

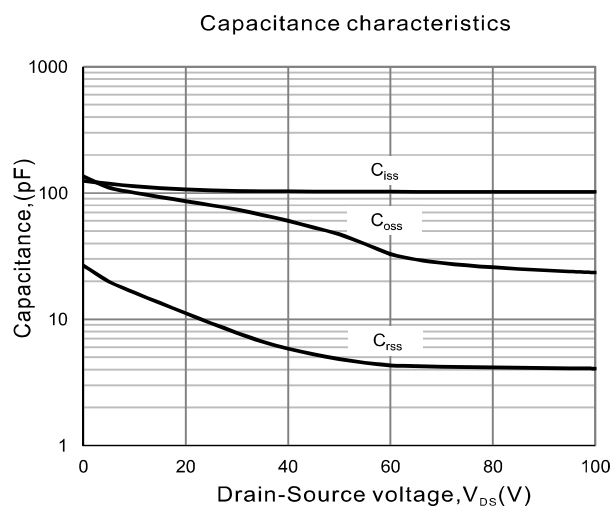
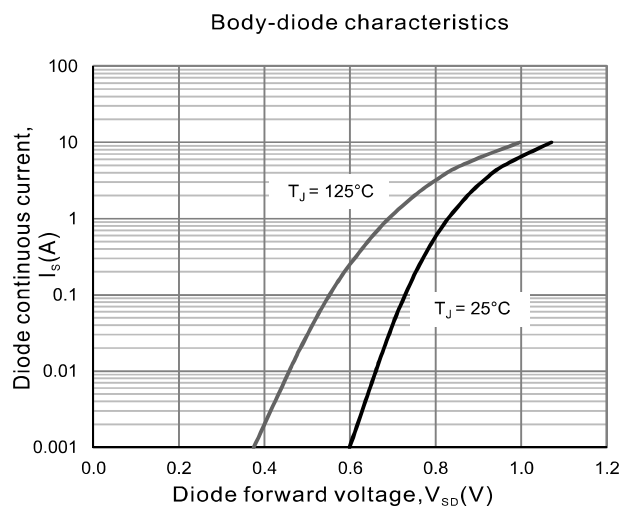
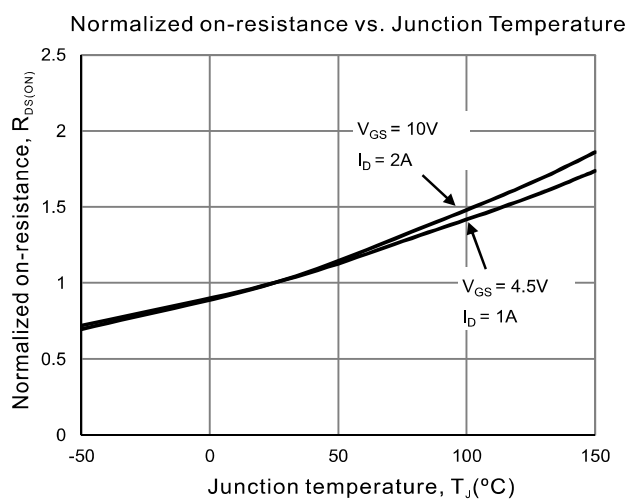
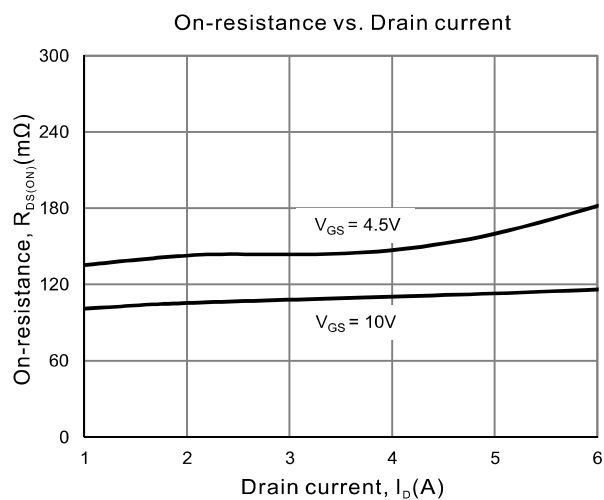
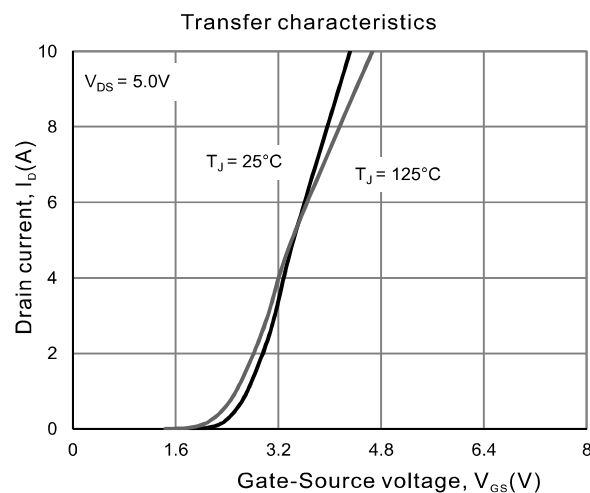
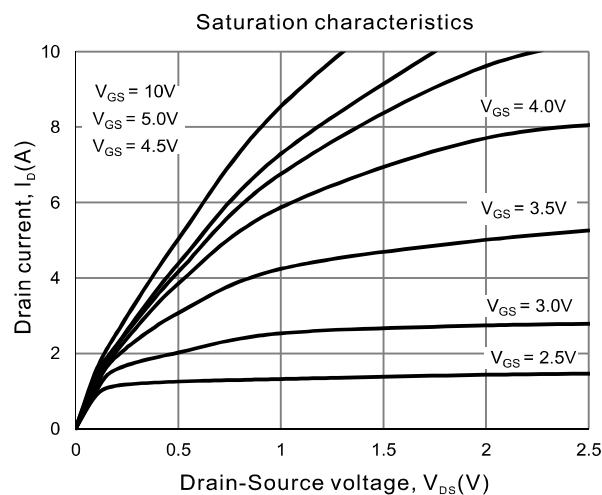
Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Static parameters						
Drain-source breakdown voltage	I _D =250μA, V _{GS} =0V	BV _{DSS}	100			V
Drain-source leakage current	V _{DS} =80V, V _{GS} =0V	I _{DSS}			1.0	μA
	V _{DS} =80V, V _{GS} =0V, T _J =55°C				5.0	
Gate-source leakage current	V _{GS} =±20V, V _{DS} =0V	I _{GSS}			±100	nA
Gate threshold voltage	V _{DS} =V _{GS} , I _D =250μA	V _{GS(TH)}	1.2	1.9	2.5	V
Static drain-source on-state resistance	V _{GS} =10V, I _D =2A	R _{DS(ON)}		105	126	mΩ
	V _{GS} =4.5V, I _D =1A			135	169	
Forward transconductance	V _{DS} =5V, I _D =2A	g _{FS}		6.8		S
Dynamic parameters (Note 5)						
Input capacitance	V _{GS} =0V, V _{DS} =50V, f=1.0MHz	C _{iss}		103		pF
Out capacitance		C _{oss}		47		
Reverse transfer capacitance		C _{rss}		4.9		
Gate resistance	V _{GS} = 0V, V _{DS} = 0V, f = 1.0MHz	R _g		2.6		Ω
Switching parameters (Note 5)						
Total gate charge	V _{GS} =10V, V _{DS} =50V, I _D =2A	Q _g		2.3		nC
	V _{GS} =4.5V, V _{DS} =50V, I _D =2A			1.3		
Gate to source charge	V _{GS} =0 to 10V, V _{DS} =50V, I _D =2A	Q _{gs}		0.3		nC
Gate to drain charge		Q _{gd}		0.7		
Turn-on delay time	V _{DS} =50V, V _{GS} =10V, R _L =25Ω, R _G =6Ω	t _{d(on)}		2.1		ns
Rise time		t _r		3.3		
Turn-off delay time		t _{d(off)}		7.5		
Fall time		t _f		3.2		
Source-drain diode ratings and characteristics						
Diode continuous current	T _A =25°C	I _S			1.0	A
Drain-source diode forward voltage	I _{SD} =1A, V _{GS} =0V	V _{SD}		0.7	1.0	V
Reverse recovery time	I _F =2A, dI _F /dt=100A/μs	t _{rr}		21		ns
Reverse recovery charge		Q _{rr}		8.0		nC

Note:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under $T_{J_Max} = 150^{\circ}\text{C}$.
3. This single-pulse measurement was taken under the following condition [$L = 100\mu\text{H}$, $V_{GS} = 10\text{V}$, $V_{DS} = 50\text{V}$] while its value is limited by $T_{J_Max} = 150^{\circ}\text{C}$.
4. The power dissipation P_D is based on $T_{J_Max} = 150^{\circ}\text{C}$.
5. This value is guaranteed by design hence it is not included in the production test.

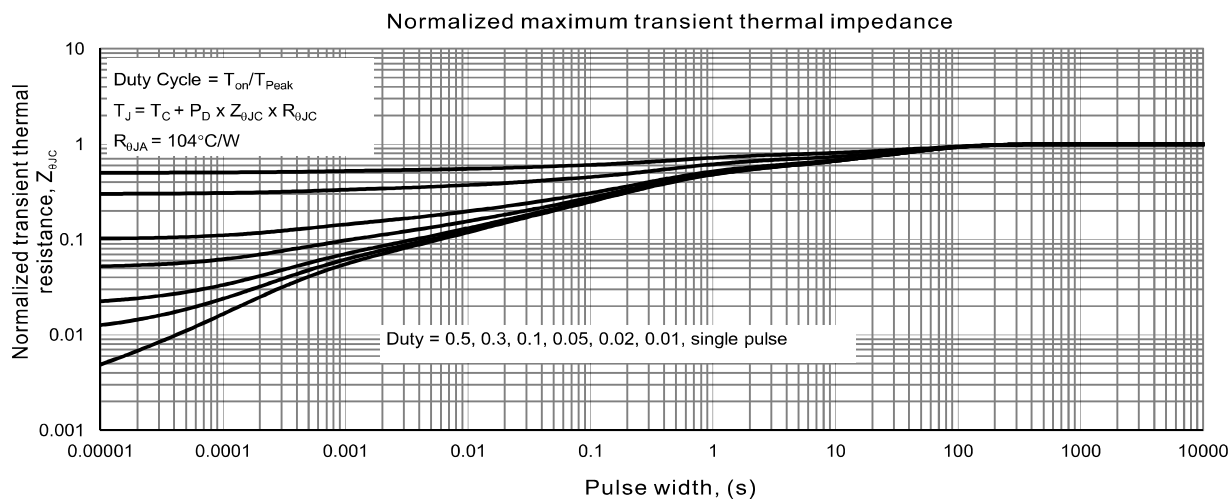
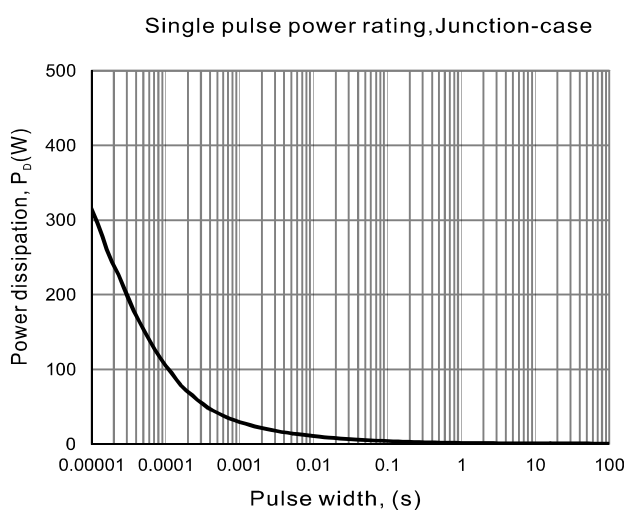
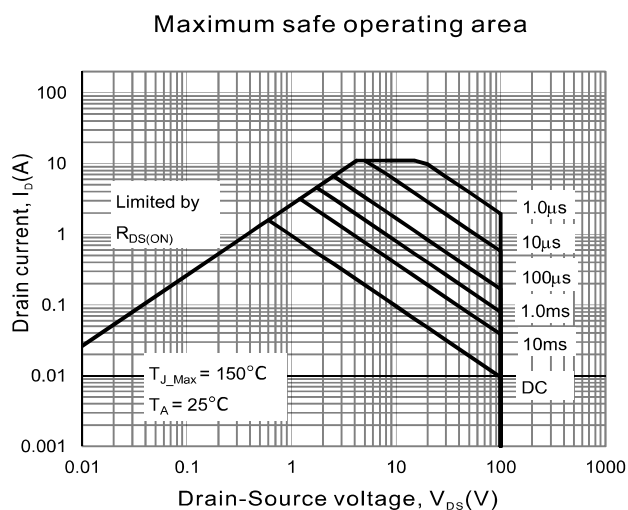
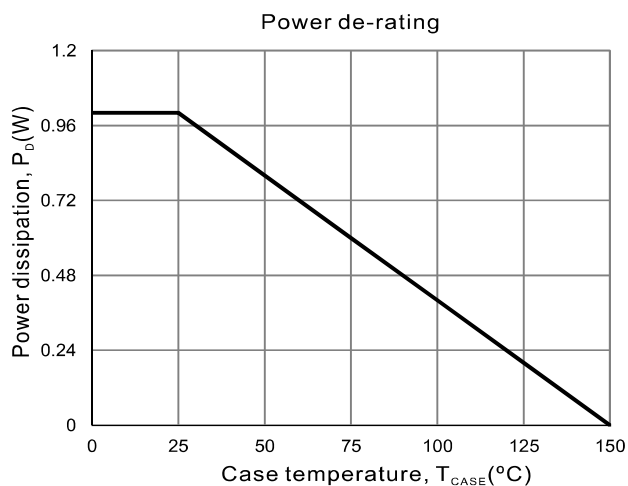
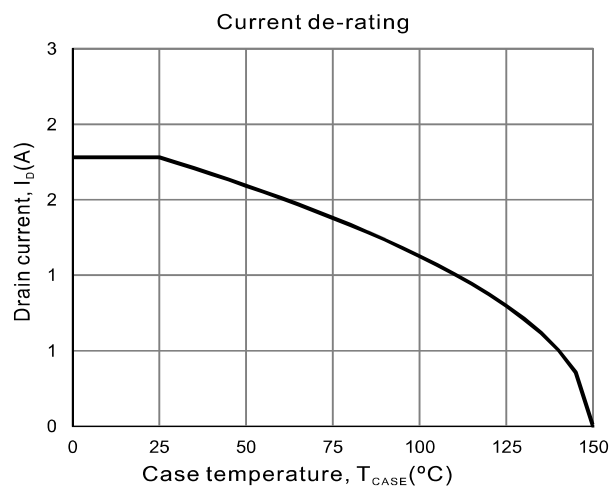
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Rating and Characteristic Curves



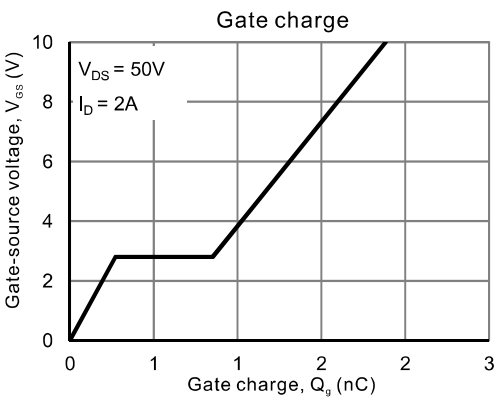
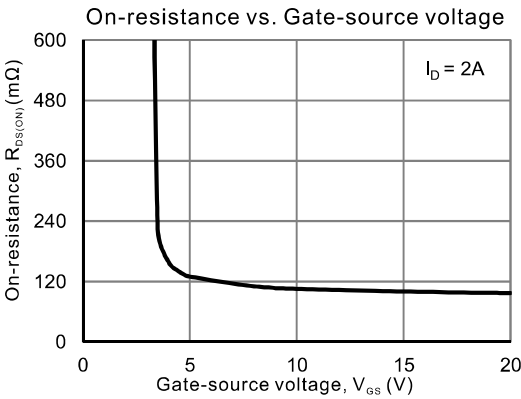
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Rating and Characteristic Curves



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Rating and Characteristic Curves



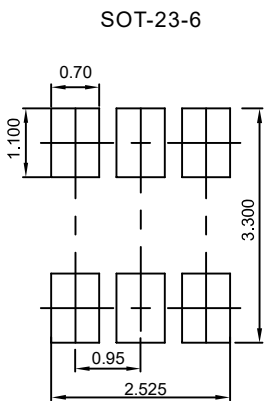
Pinning information

Pin	Simplified outline	Symbol
Pin 1, 2 Drain Pin 3 Gate Pin 4 Source Pin 5, 6 Drain	Top view	

Marking

Type number	Marking code
FMOSL02N10	1013

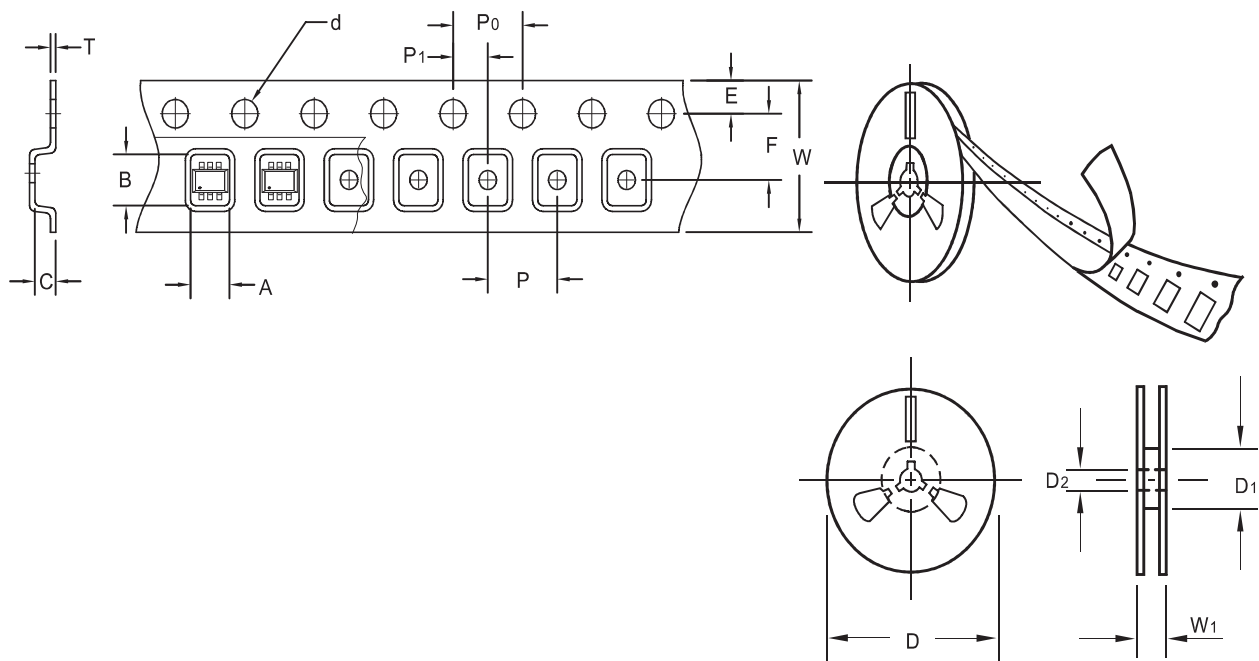
Suggested solder pad layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.1mm.
3.The pad layout is for reference purposes only.

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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-23-6
Carrier width	A	0.2	3.10
Carrier length	B	0.2	2.70
Carrier depth	C	0.1	1.20
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D ₁	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D ₁	min	62.00
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.20
Tape width	W	0.3	8.00
Reel width	W ₁	1.0	11.40

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

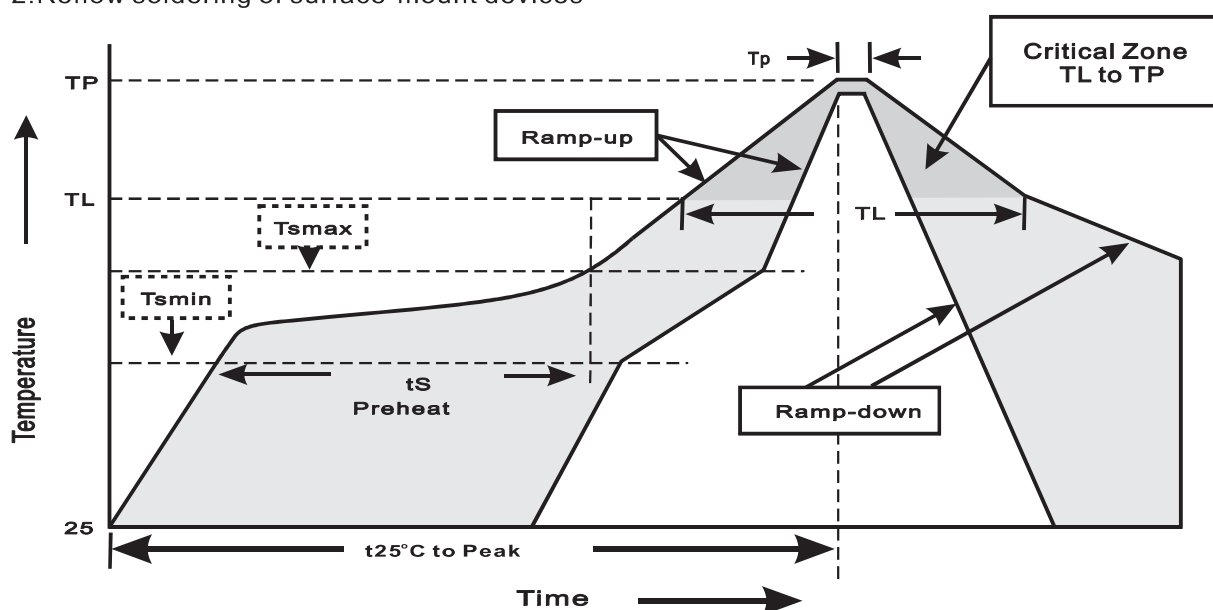
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
SOT-23-6	7"	3,000	4.0	30,000	210*208*203	178	440*435*22.7	180,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(TL to TP)	<3°C/sec
Preheat -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time(min to max)(ts)	150°C 200°C 60~120sec
Tsmax to TL -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(TL) -Time(tL)	217°C 60~260sec
Peak Temperature(TP)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(tp)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes