

FMOSGTQC393N10-Q1-H

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FMOSGTQC393N10-Q1-H

393A 100V N-Channel Shield Gate Trench
Enhancement Mode Power MOSFET

Features

- $V_{DS}=100V$, $I_D=393A$.
- $R_{DS(ON)} \leq 1.3m\Omega$, @ $V_{GS}=10V$, $I_D=20A$.
- Low on-resistance.
- Excellent FOM. (figure of merit)
- 100% and R_g tested.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21).

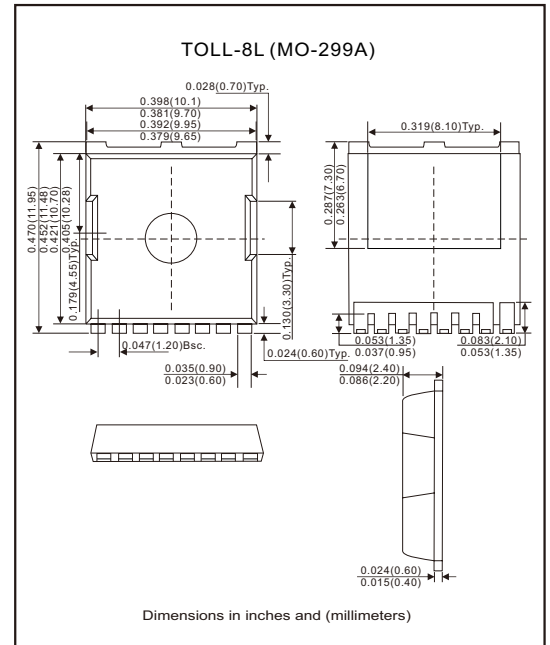
Applications

- DC/DC in telecoms and industrial.
- Synchronous rectification in SMPS.
- Hard switching and high speed circuit.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case: Molded plastic, TOLL-8L (MO-299A).
- Weight : Approximated 760mg.

Package outline

Maximum ratings (At $T_c=25^\circ C$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($V_{GS}=10V$) (Note 1)	I_D	($T_c=25^\circ C$) 393	A
		($T_c=100^\circ C$) 278	
Pulsed drain current (Note 2)	I_{DM}	1341	A
Single pulse, avalanche current ($L=0.3mH$)	I_{AS}	74	A
Single pulsed, avalanche energy (Note 3)	E_{AS}	2016	mJ
Power dissipation	P_D	($T_c=25^\circ C$) 429	W
		($T_c=100^\circ C$) 214	
Thermal resistance, junction to ambient (Note 4)	$R_{\theta JA}$	29	$^\circ C/W$
Thermal resistance, junction to case (Note 5)	$R_{\theta JC}$	0.35	$^\circ C/W$
Junction temperature	T_J	+175	$^\circ C$
Storage temperature range	T_{STG}	-55 to +175	$^\circ C$

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Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics (Note6)						
Drain-source breakdown voltage	B _V _{DSS}	I _D =250μA, V _{GS} =0V	100			V
Drain-source leakage current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =125°C			100	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
On characteristics (Note6)						
Gate threshold voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Static drain-source on-state resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		1.1	1.3	mΩ
Forward transconductance	g _{FS}	V _{DS} =5V, I _D =20A		80		S
Dynamic parameters (Note7)						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =50V, f=1.0MHz		9660		pF
Out capacitance	C _{oss}			3476		
Reverse transfer capacitance	C _{rss}			48		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		2.1		Ω
Switching parameters (Note7)						
Total gate charge (V _{GS} =10V)	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =20A		140		nC
Total gate charge (V _{GS} =6V)				88		
Gate to source charge	Q _{gs}			38		
Gate to drain charge	Q _{gd}			27		
Gate plateau voltage	V _{plateau}	V _{GS} =10V, V _{DS} =50V, I _D =20A		4.2		V
Turn-on delay time	t _{d(on)}	V _{DS} =50V, V _{GS} =10V, I _D =20A, R _{GEN} =3Ω		25		ns
Rise time	t _r			42		
Turn-off delay time	t _{d(off)}			87		
Fall time	t _f			63		
Source-drain diode ratings and characteristics						
Drain-source diode forward voltage (Note6)	V _{SD}	I _S =2A, V _{GS} =0V		0.7	1.2	V
Continuous drain-source diode forward current (Note7)	I _S	T _C =25°C			393	A
Body diode reverse recovery time (Note7)	t _{rr}	I _F =20A, di/dt=100A/μs, T _J =25°C		105		ns
Body diode reverse recovery charge (Note7)	Q _{rr}			394		nC

Note: 1. This current is chip limited, which is calculated based on $R_{\theta JC}$.2. This current is calculated on single pulse with $10\mu\text{s}$ pulse and duty cycle=1%.3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^{\circ}\text{C}$, $V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $L=1.0\text{mH}$.

4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.

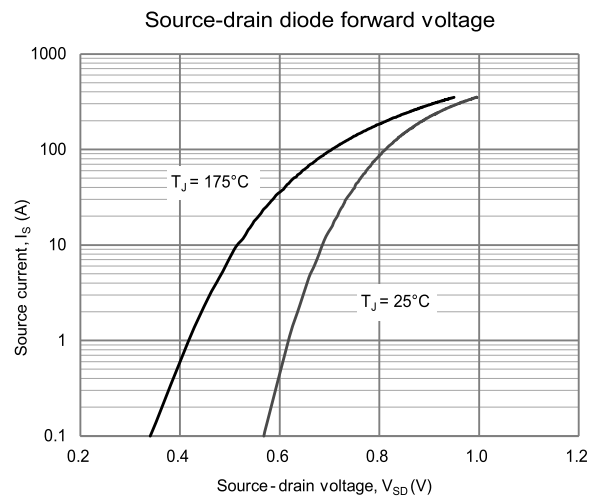
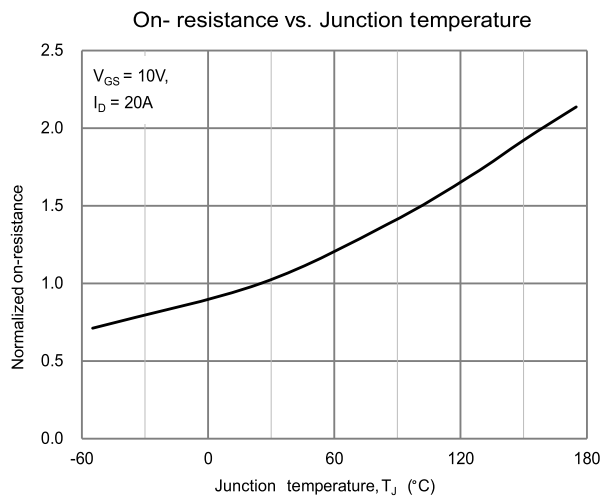
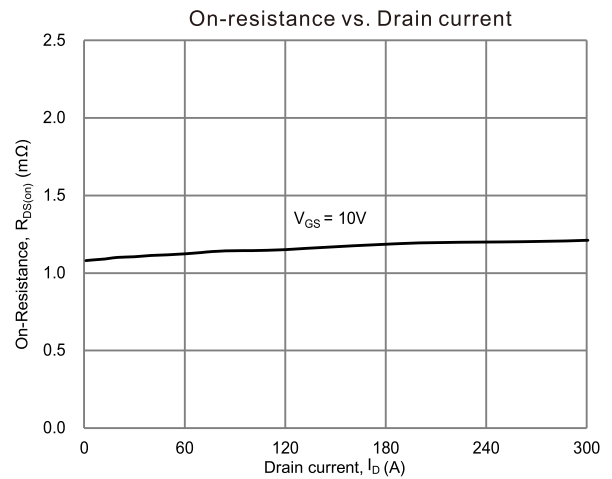
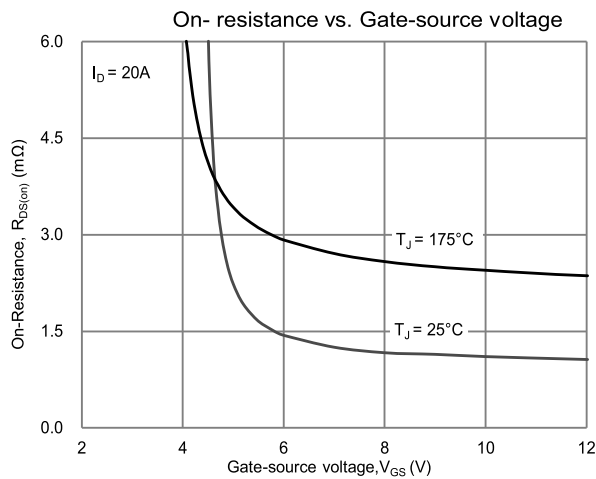
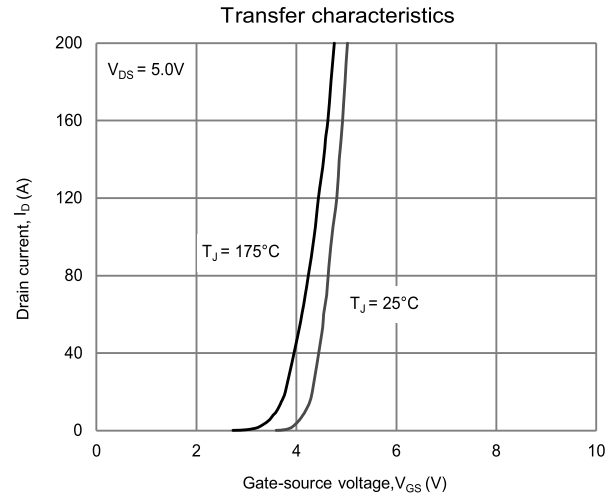
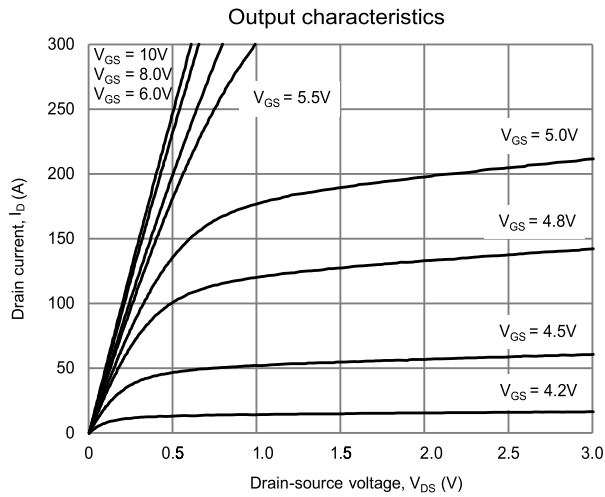
5. Thermal resistance from junction to soldering point (on the exposed drain pad).

6. Short duration pulse test used to minimize self-heating effect.

7. Defined by design, not subject to production.

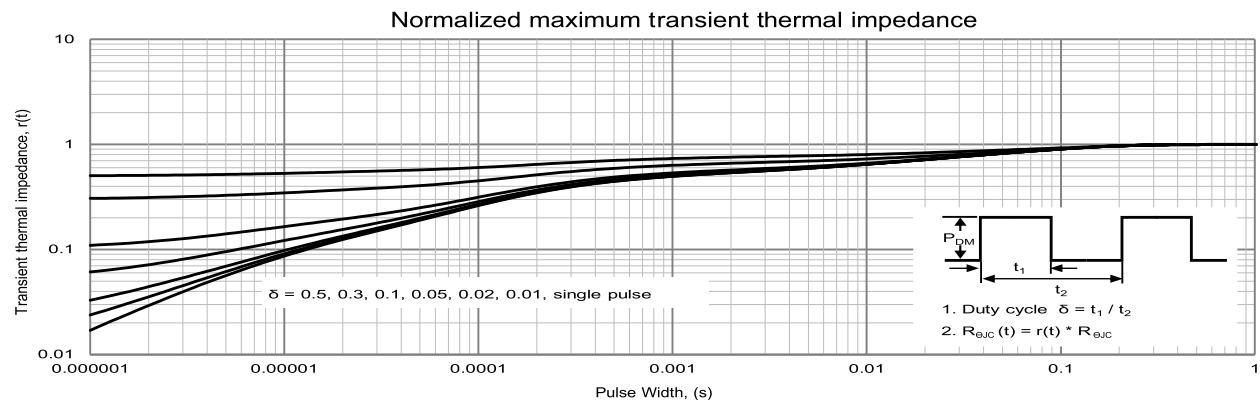
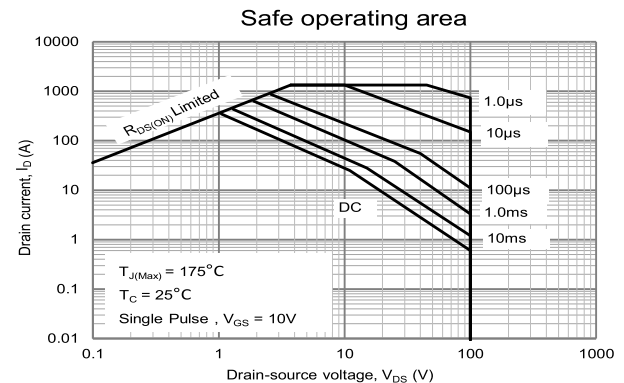
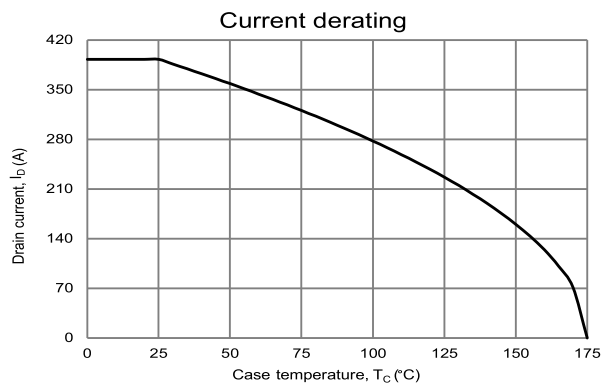
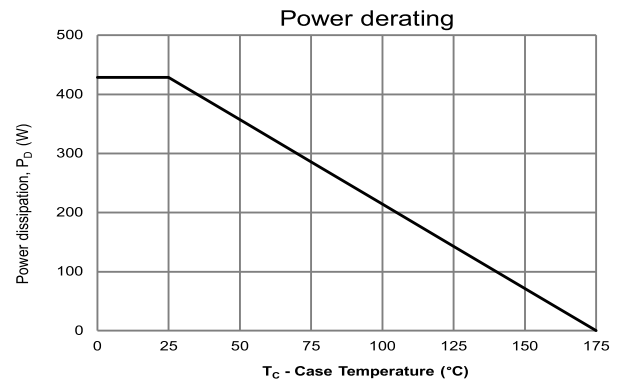
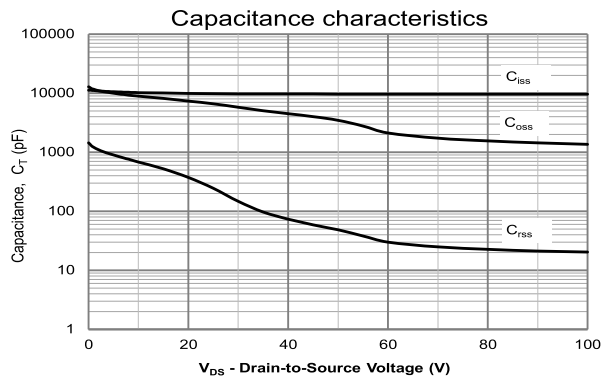
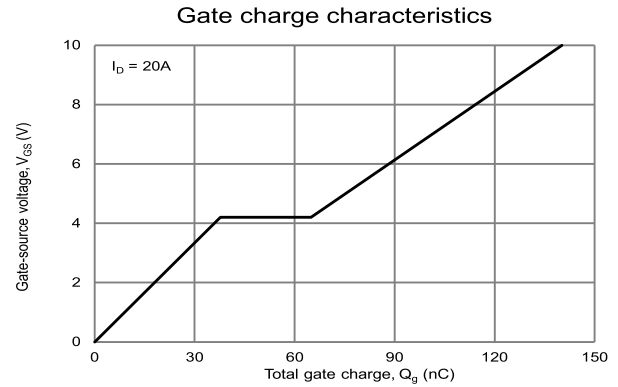
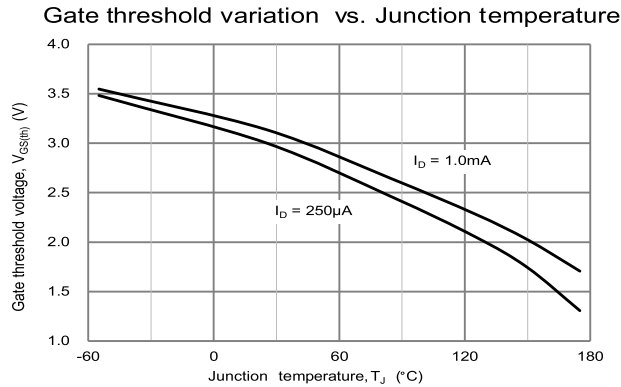
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Rating and characteristics curves



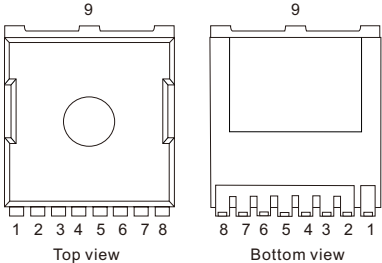
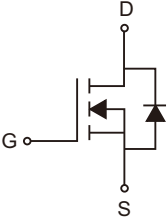
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Rating and characteristics curves



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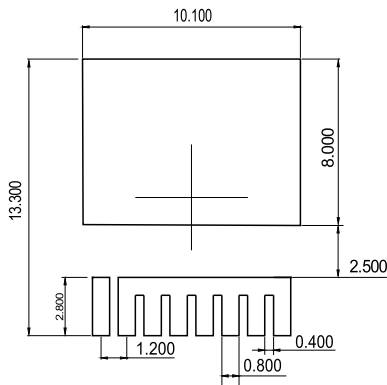
Pinning information

Pin	Simplified outline	Symbol
Pin 1 Gate Pin 2, 3, 4, 5, 6, 7, 8 Source Pin 9 Drain		

Marking

Type number	Marking code
FMOSGTQC393N10-Q1-H	10T01AHQ

Suggested solder pad layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.1 mm.
3. The pad layout is for reference purposes only.

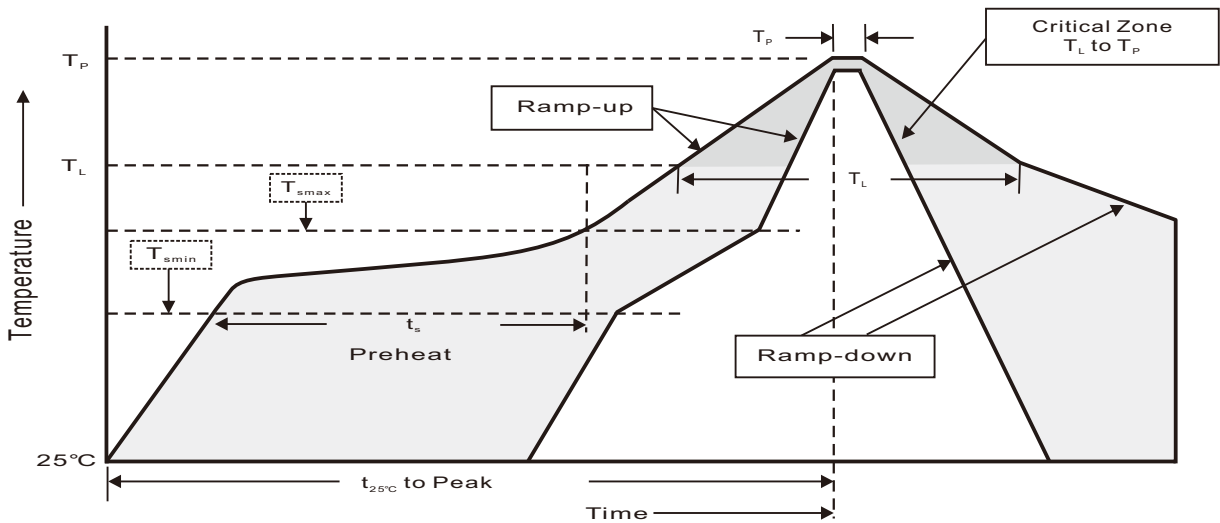
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Reel packing

DEVICE	PACKAGE	REEL SIZE	REEL (pcs)
FMOSGTQC393N10-Q1-H	TOLL-8L	13"	2,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%
2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_p)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_p)	255 °C -0/+5°C
Time with 5°C of actual peak temperature (T_p)	10 ~30 sec
Ramp-down rate	< 6 °C/sec
Time 25°C to peak temperature	< 6 minutes