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FMOSGTQC385N10-H

385A 100V N-Channel Shield Gate Trench Enhancement Mode Power MOSFET

Features

- V_{DS}= 100V, I_D= 385A.
- $R_{DS(ON)} \leq$ 1.35mΩ, @ V_{GS}=10V, I_D=20A.
- Low on-resistance.
- Excellent FOM. (figure of merit)
- 100% UIS and R_g and ΔV_{ds} tested.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21).

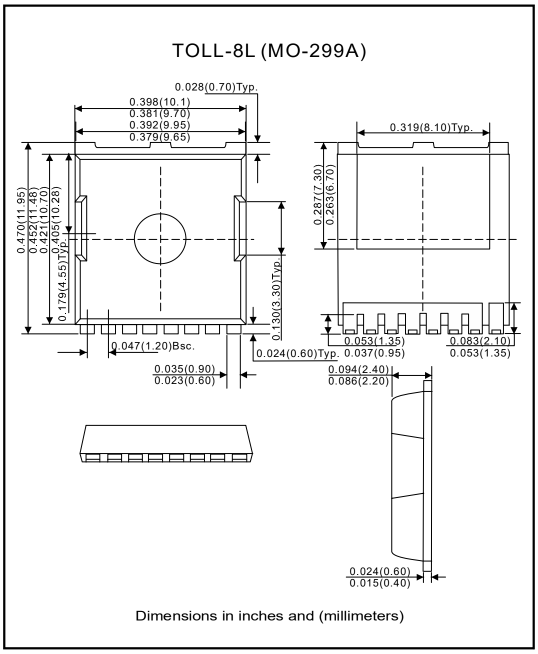
Applications

- DC/DC in telecoms and inductrial.
- Synchronous rectification in SMPS.
- Hard switching and high speed circuit.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case: Molded plastic, TOLL-8L (MO-299A).
- Mounting Position: Any.

Package outline



Maximum ratings (At T_C=25°C unless otherwise specified)

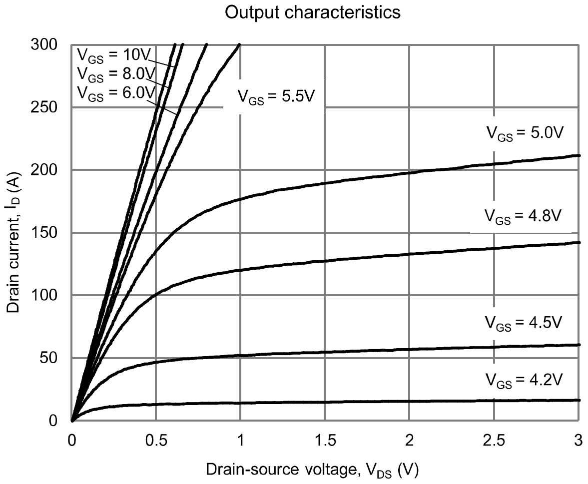
Parameter		Symbol	Ratings	Unit
Drain to source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	±20	V
Continuous drain current (V_{GS}=10V) (Note 1)	(T_C=25°C)	I_D	385	A
	(T_C=100°C)		273	
Pulsed drain current (Note 2)		I_{DM}	1316	A
Single pulse, avalanche current (L=0.3mH)		I_{AS}	74	A
Single pulsed, avalanche energy (Note 3)		E_{AS}	2016	mJ
Power dissipation	(T_C=25°C)	P_D	429	W
	(T_C=100°C)		214	
Thermal resistance, junction to ambient (Note 4)		$R_{\theta JA}$	29	°C/W
Thermal resistance, junction to case (Note 5)		$R_{\theta JC}$	0.35	°C/W
Junction temperature		T_J	+175	°C
Storage temperature range		T_{STG}	-55 to +175	°C

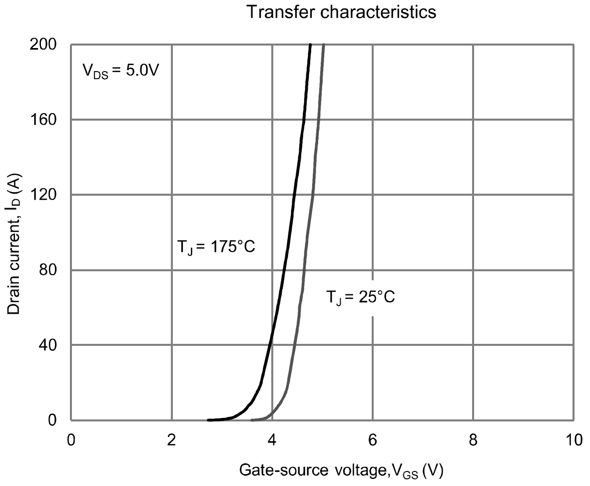
Electrical characteristics (At T_J=25°C unless otherwise noted)

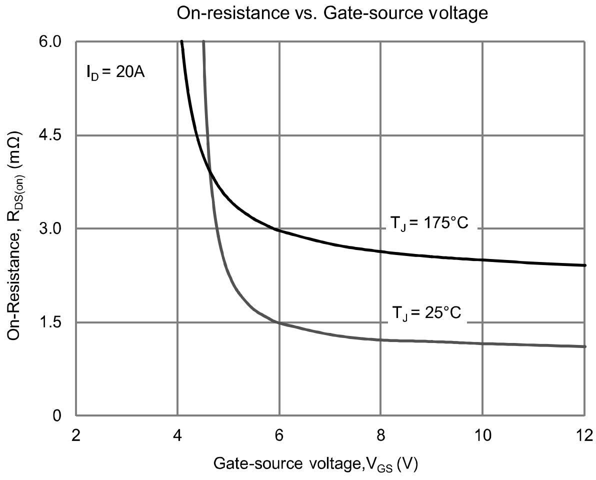
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics (Note6)						
Drain-source breakdown voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Drain-source leakage current	I_{DSS}	V_{DS}=100V, V_{GS}=0V			1	μA
		V_{DS}=100V, V_{GS}=0V, T_J=125°C			100	
Gate-source leakage current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
On characteristics (Note6)						
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2	3	4	V
Static drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		1.15	1.35	mΩ
Forward transconductance	g_{FS}	V_{DS}=5V, I_D=20A		80		S
Dynamic parameters (Note7)						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=50V, f=1.0MHz		9660		pF
Out capacitance	C_{oss}			3476		
Reverse transfer capacitance	C_{rss}			48		
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1.0MHz		2.1		Ω
Switching parameters (Note7)						
Total gate charge (V_{GS}=10V)	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=20A		140		nC
Total gate charge (V_{GS}=6V)				88		
Gate to source charge	Q_{gs}			38		
Gate to drain charge	Q_{gd}			27		
Gate plateau voltage	$V_{plateau}$	V_{GS}=10V, V_{DS}=50V, I_D=20A		4.2		V
Turn-on delay time	$t_{d(on)}$	V_{DS}=50V, V_{GS}=10V, I_D=20A, R_{GEN}=3Ω		25		ns
Rise time	t_r			42		
Turn-off delay time	$t_{d(off)}$			87		
Fall time	t_f			63		
Source-drain diode ratings and characteristics						
Drain-source diode forward voltage (Note6)	V_{SD}	I_S=2A, V_{GS}=0V		0.7	1.2	V
Continuous drain-source diode forward current (Note7)	I_S	T_C=25°C			385	A
Body diode reverse recovery time (Note7)	t_{rr}	I_F=20A, di/dt=100A/μs, T_J=25°C		105		ns
Body diode reverse recovery charge (Note7)	Q_{rr}			394		nC

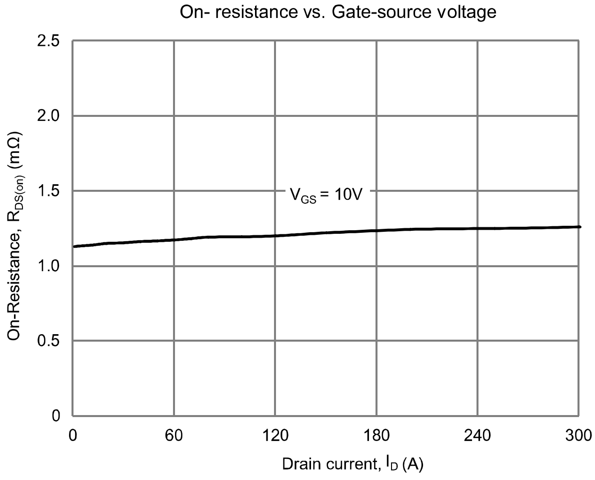
Note : 1. This current is chip limited, which is calculated based on $R_{\theta JC}$.
2. This current is calculated on single pulse with 10μs pulse and duty cycle=1%.
3. Defined by design, not subject to production test, E_{AS} condition: T_J=25°C, V_{DD}=50V, V_{GS}=10V, L=1.0mH.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

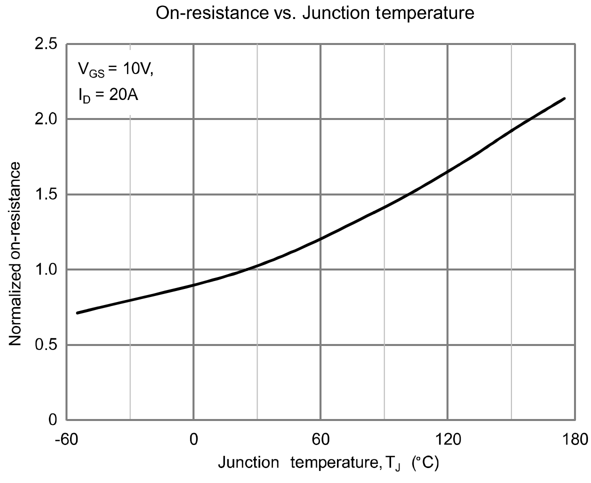
Rating and characteristics curves

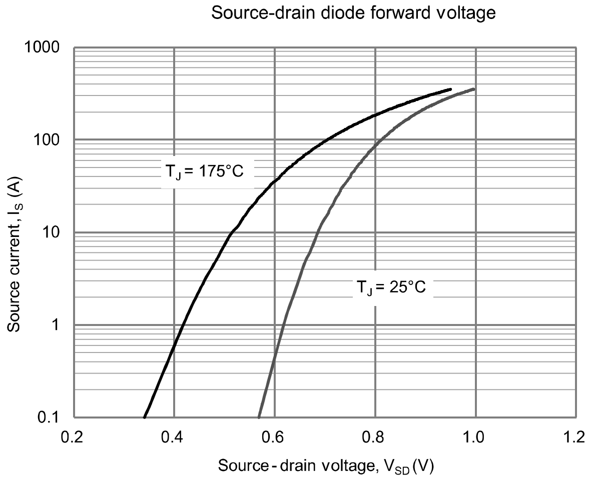

Output characteristics


Transfer characteristics


On-resistance vs. Gate-source voltage


On- resistance vs. Gate-source voltage


On-resistance vs. Junction temperature


Source-drain diode forward voltage

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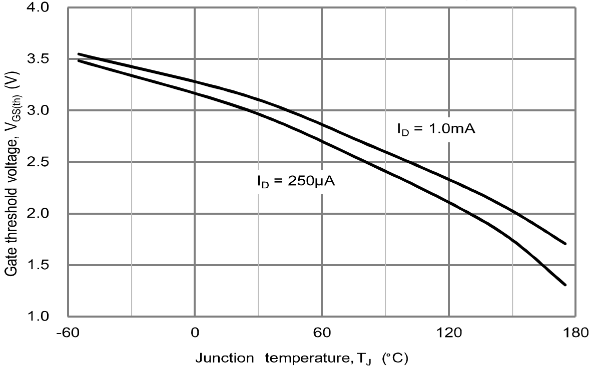
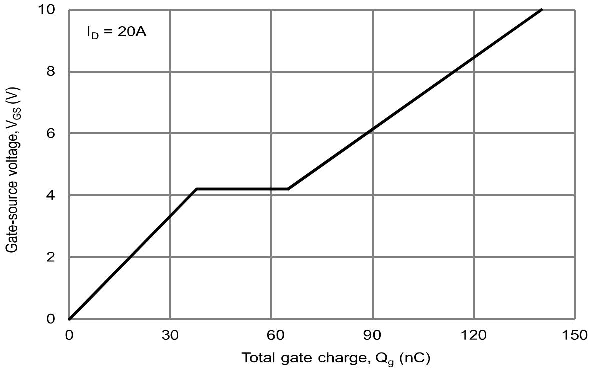
Rating and characteristics curves

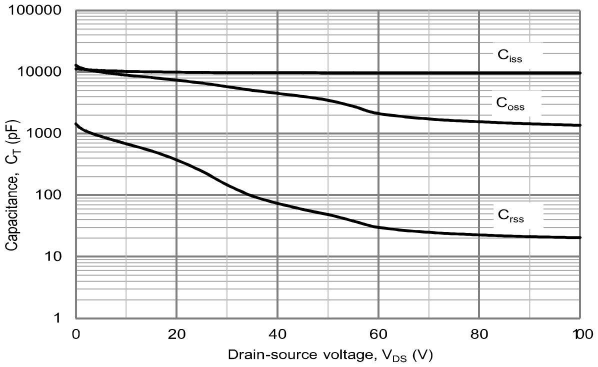
Gate threshold variation vs. Junction temperature



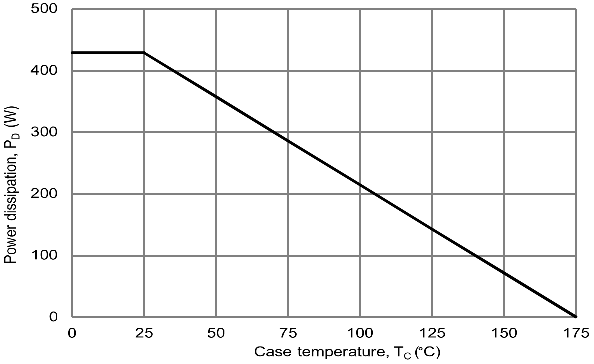
Gate charge characteristics



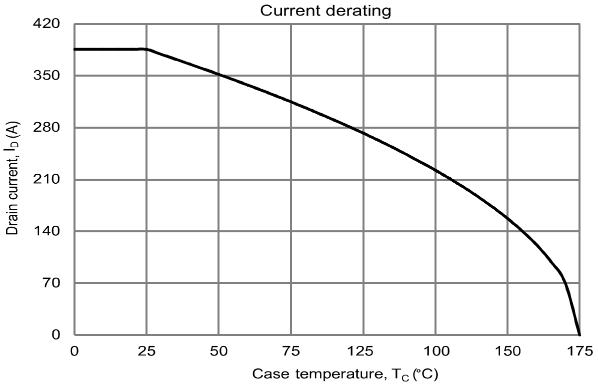
Capacitance characteristics



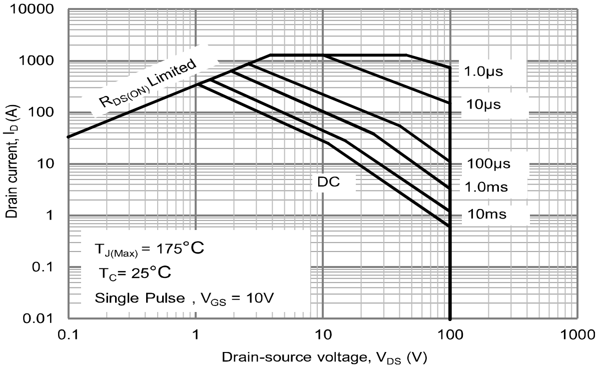
Power derating



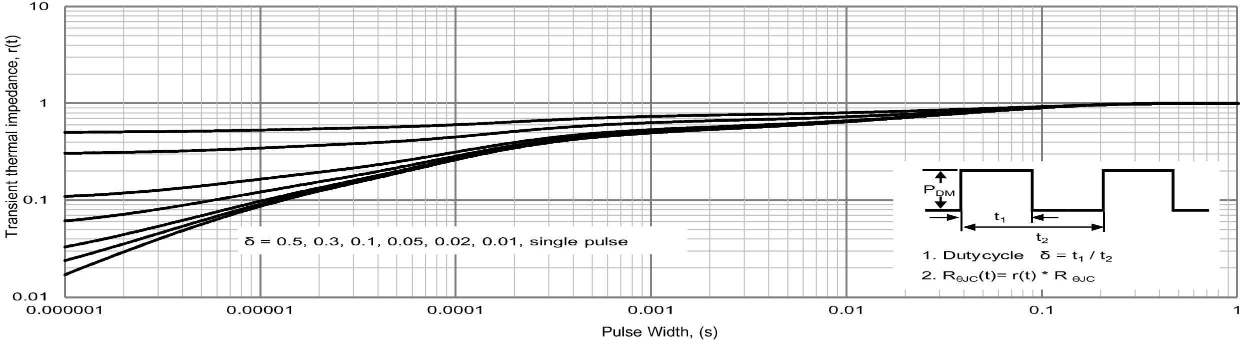
Current derating



Safe operating area



Normalized maximum transient thermal impedance



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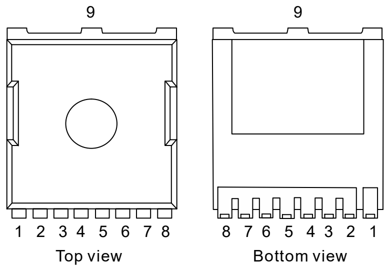
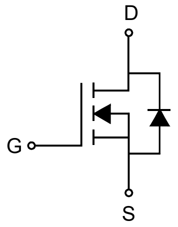
Pinning information

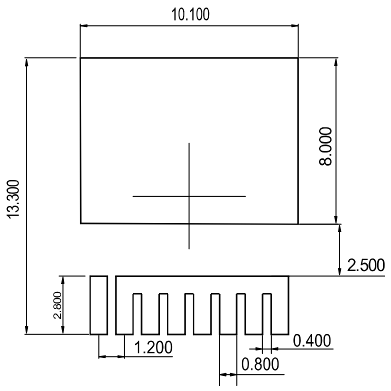
Pin	Simplified outline	Symbol
Pin 1 Gate Pin 2, 3, 4, 5, 6, 7, 8 Source Pin 9 Drain		

Marking

Type number	Marking code
FMOSGTQC385N10-H	10T01AH YYWWJX

YYWW:Wafer lot code
YY:Year
WW:Week
J:Fixed code
X:Traceability code

Suggested solder pad layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.1mm.
3.The pad layout is for reference purposes only.

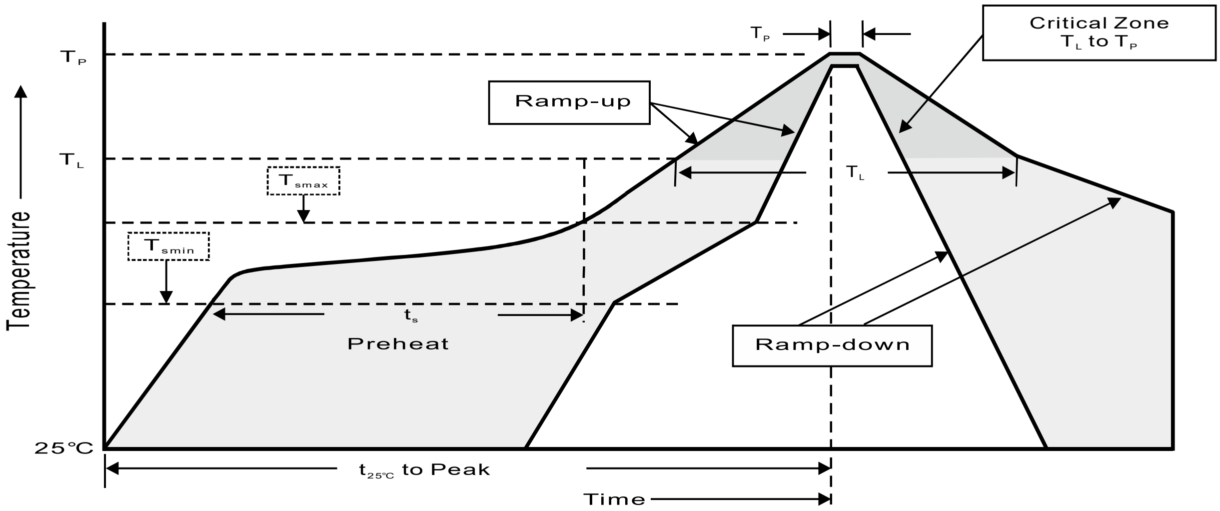
Reel packing

DEVICE	PACKAGE	REEL SIZE	REEL (pcs)
FMOSGTQC385N10-H	TOLL-8L	13"	2,000

Suggested thermal profiles for soldering processes

1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%

2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_P)	< 3 ℃/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150℃ 200℃ 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 ℃/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217℃ 60 ~ 260 sec
Peak temperature (T_P)	255 ℃ -0/+5℃
Time with 5℃ of actual peak temperature (T_P)	10 ~30 sec
Ramp-down rate	< 6 ℃/sec
Time 25℃ to peak temperature	< 6 minutes