# FMOSGTQ01P1P15-H

## List

# FMOSGTQ01P1P15-H

## -1.1A -150V P-Channel Shield Gate Trench Enhancement Mode Power MOSFET

## Features

- $-V_{DS}$=150V, $-I_D$=1.1A.
- $R_{DS(ON)}$≤ 780mΩ, @ $-V_{GS}$=10V, $-I_D$=1A.
- $R_{DS(ON)}$≤ 980mΩ, @ $-V_{GS}$=6V, $-I_D$=0.5A.
- Advanced trench MOS technology.
- 100% EAS guaranteed.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21).

## Applications

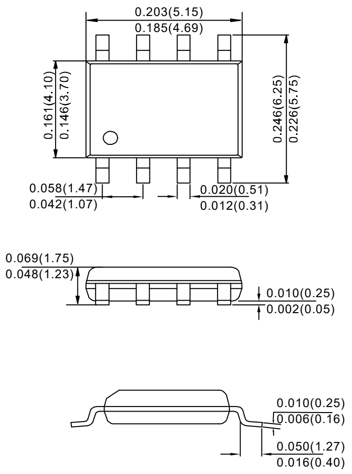
- Load switch.
- Power management.
- LED backlighting.
- Networking application.

## Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, SOP8 (SOP-08).
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026.
- Mounting Position : Any.

## Package outline

SOP8 (SOP-08)



Dimensions in inches and (millimeters)

## Maximum ratings ( At T=25°C unless otherwise specified)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain-source voltage | $-V_{DS}$ | 150 | V |
| Gate-source voltage | $V_{GS}$ | ±20 | |
| Continuous drain current, $V_{GS}$@-10V (note 1) ($T_A$= 25°C) | $-I_D$ | 1.1 | A |
| ($T_A$= 70°C) | | 0.88 | |
| Pulse drain current (note 2) | $-I_{DM}$ | 4.4 | A |
| Avalanche current | $-I_{AS}$ | 5 | A |
| Single pulse avalanche energy (note 3) | $E_{AS}$ | 12.5 | mJ |
| Maximum power dissipation (note 4) ($T_A$= 25°C) | $P_D$ | 2 | W |
| Thermal resistance, junction to ambient (note 1) | $R_{\theta JA}$ | 62 | °C/W |
| Thermal resistance, junction to case (note 1) | $R_{\theta JC}$ | 40 | °C/W |
| Maximum junction temperature | $T_J$ | +150 | °C |
| Storage temperature range | $T_{STG}$ | - 55 to +150 | °C |

## Electrical characteristics (At $T_J$=25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static parameters** | | | | | | |
| Drain-source breakdown voltage | $-BV_{DSS}$ | $-I_D$=250μA, $V_{GS}$=0V | 150 | | | V |
| Drain-source leakage current | $-I_{DSS}$ | $-V_{DS}$=120V , $V_{GS}$=0V , $T_J$=25°C | | | 1 | μA |
| | | $-V_{DS}$=120V , $V_{GS}$=0V , $T_J$=85°C | | | 30 | |
| Gate-source leakage current | $-I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$=0V | | | ±100 | nA |
| **On characteristics** | | | | | | |
| Gate threshold voltage | $-V_{GS(TH)}$ | $V_{DS}$=$V_{GS}$, $-I_D$=250μA | 2 | 3 | 4 | V |
| Static drain-source on-state resistance (Note 2) | $R_{DS(ON)}$ | $-V_{GS}$=10V, $-I_D$=1A | | 650 | 780 | mΩ |
| | | $-V_{GS}$=6V, $-I_D$=0.5A | | 700 | 980 | |
| **Dynamic parameters** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0V, $-V_{DS}$=75V, f=1.0MHz | | 706 | | pF |
| Out capacitance | $C_{oss}$ | | | 23 | | |
| Reverse transfer capacitance | $C_{rss}$ | | | 13 | | |
| Gate resistance | $R_g$ | $V_{DS}$=0V, $V_{GS}$=0V, f=1.0MHz | | 12 | | Ω |
| **Switching parameters** | | | | | | |
| Total gate charge | $Q_g$ | $-V_{GS}$=10V, $-V_{DS}$=75V, $-I_D$=1A | | 10.8 | | nC |
| Gate to source charge | $Q_{gs}$ | | | 3.1 | | |
| Gate to drain charge | $Q_{gd}$ | | | 2.2 | | |
| Turn-on delay time | $t_{d(on)}$ | $-V_{DD}$=30V, $-V_{GS}$=10V, $R_G$=6Ω, $-I_D$=1A | | 21 | | ns |
| Rise time | $t_r$ | | | 16 | | |
| Turn-off delay time | $t_{d(off)}$ | | | 40 | | |
| Fall time | $t_f$ | | | 18 | | |
| **Source-drain diode ratings and characteristics** | | | | | | |
| Drain-source diode forward voltage (Note 2) | $-V_{SD}$ | $V_{GS}$=0V, $-I_S$=1A, $T_J$=25°C | | | 1.2 | V |
| Diode continuous current (Note 1,5) | $-I_S$ | $V_G$=$V_D$=0V, force current | | | 1 | A |

Note:1. The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%.
3. The $E_{AS}$ data shows maximum rating. The test condition is $-V_{DD}$=50V, $-V_{GS}$=10V, L=1mH, $-I_{AS}$=5A.
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as $I_D$ and $I_{DM}$, in real applications, should be limited by total power dissipation.

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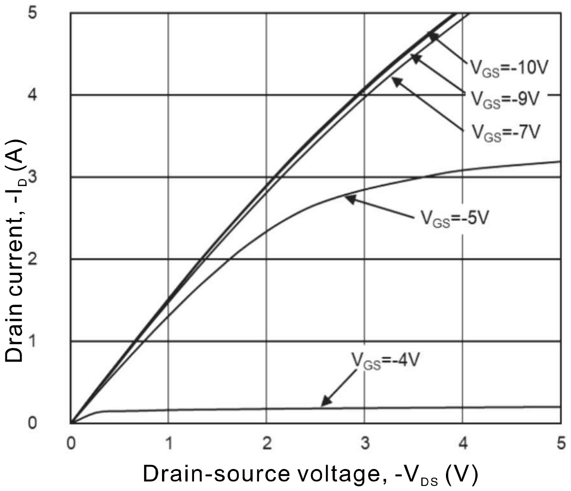
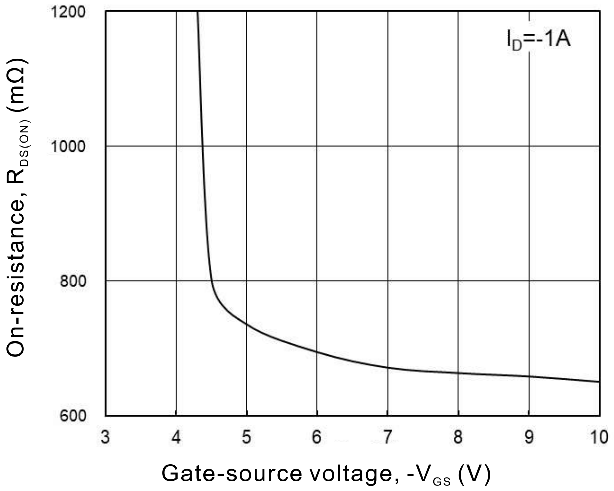
## Rating and characteristic curves

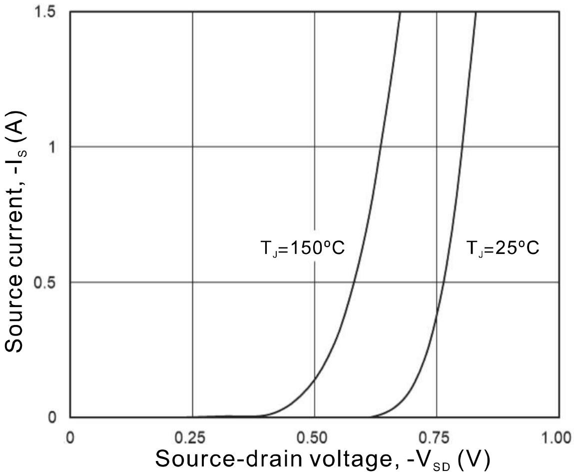
Typical output characteristics



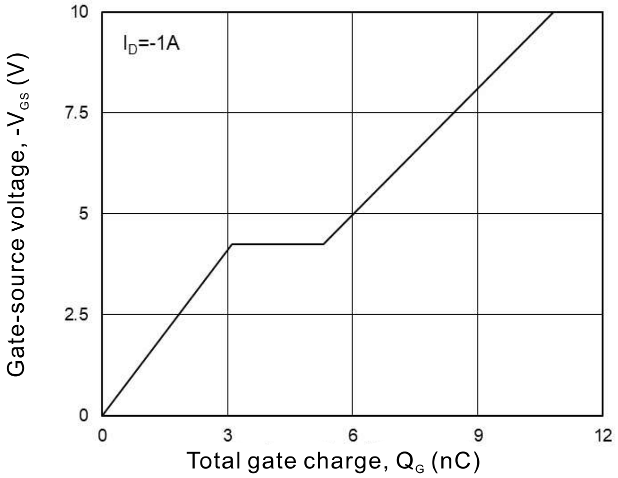
On-resistance vs. Gate-source voltage



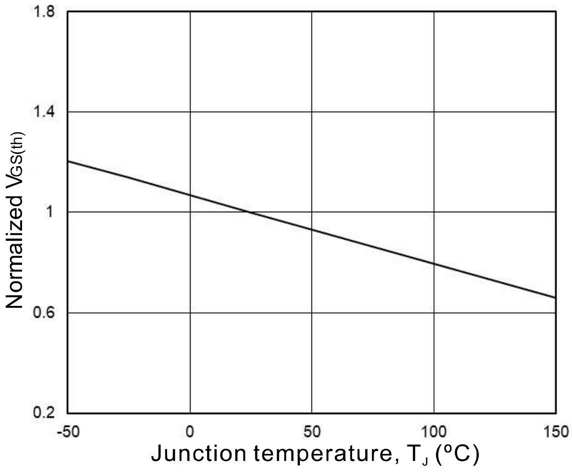
Source drain forward characteristics



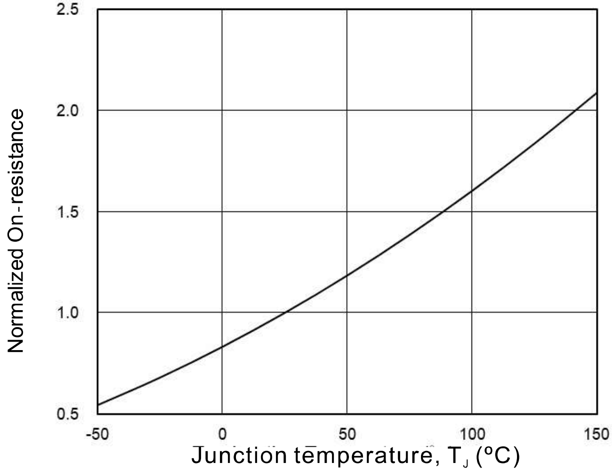
Gate-charge characteristics



Normalized gate threshold voltage vs. Junction temperature

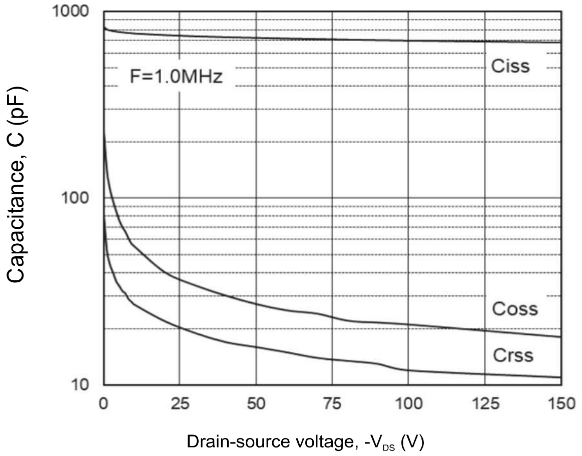


Normalized on-resistance vs. Junction temperature

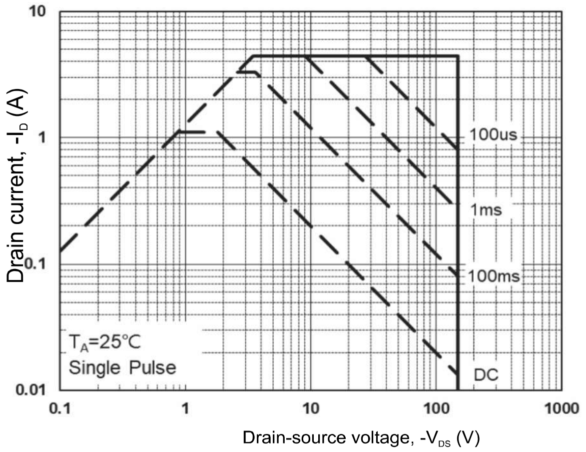


## Rating and characteristic curves

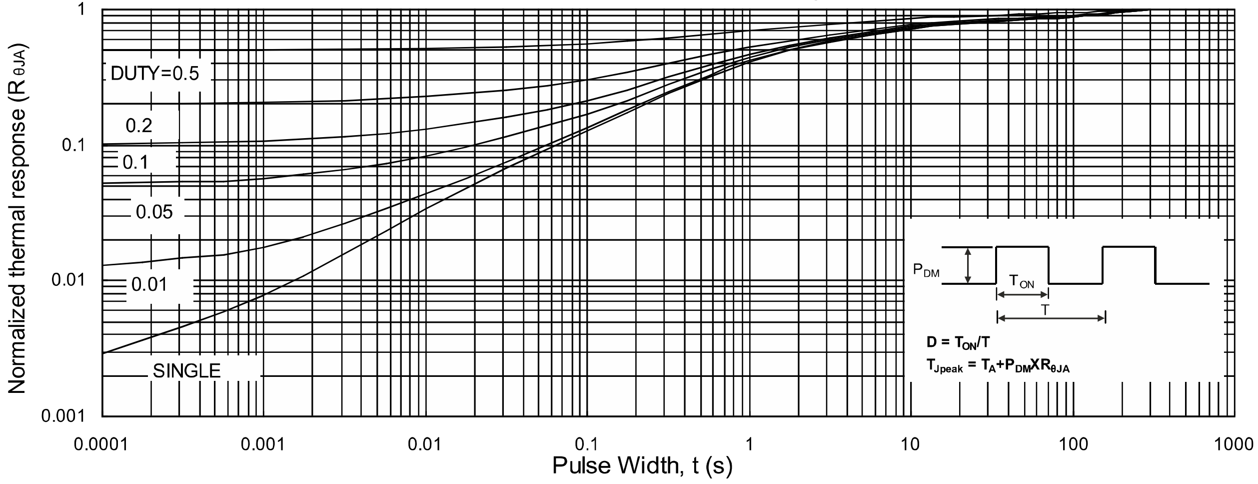
Capacitance



Safe operating area



Normalized maximum transient thermal impedance



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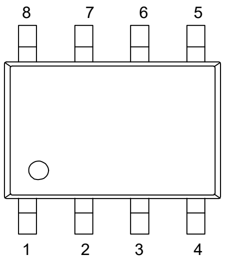
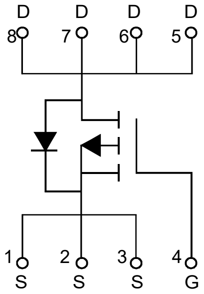
## Pinning information

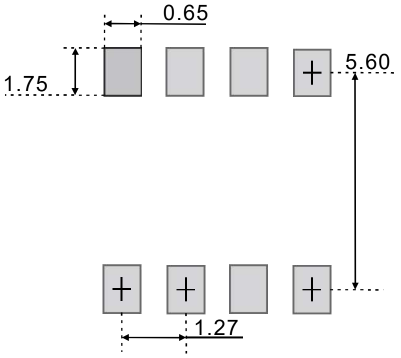
| Pin | Simplified outline | Symbol |
|---|---|---|
| Pin 1, 2, 3 Source<br>Pin 4 Gate<br>Pin 5, 6, 7, 8 Drain |  |  |

## Marking

| Type Number | Marking code |
|---|---|
| FMOSGTQ01P1P15-H | S01P15<br>YWWXXX |

* " YWW":Wafer lot code.
Y:Year
WW:Week
"XXX":Assy. code.

## Suggested solder pad layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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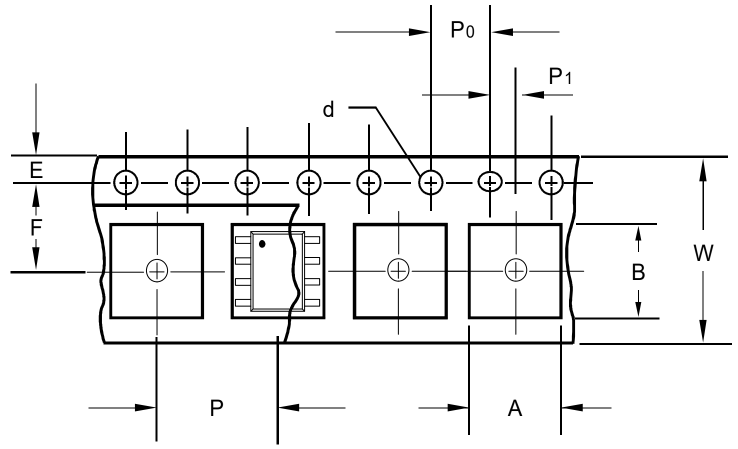
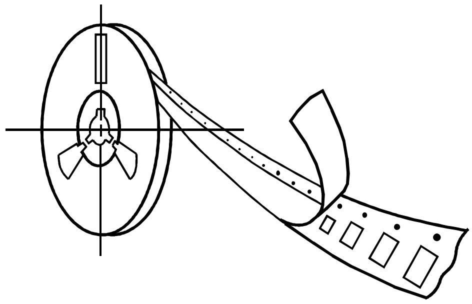
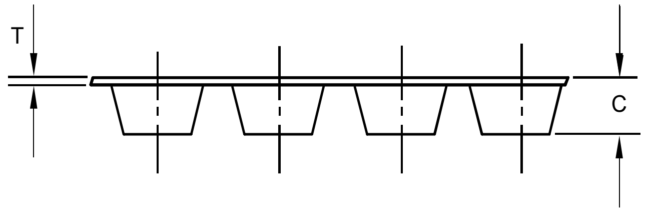
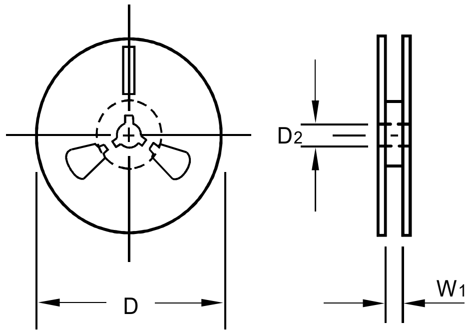
## Packing information









unit:mm

| Item | Symbol | Tolerance | SOP8 (SOP-08) |
|---|---|---|---|
| Carrier width | A | 0.1 | 6.50 |
| Carrier length | B | 0.1 | 5.30 |
| Carrier depth | C | 0.1 | 2.10 |
| Sprocket hole | d | 0.1 | 1.50 |
| 13" Reel outside diameter | D | 2.0 | 330.00 |
| Feed hole diameter | $D_2$ | 0.5 | 13.00 |
| Sprocket hole position | E | 0.1 | 1.75 |
| Punch hole position | F | 0.05 | 5.50 |
| Punch hole pitch | P | 0.1 | 8.00 |
| Sprocket hole pitch | $P_0$ | 0.1 | 4.00 |
| Embossment center | $P_1$ | 0.05 | 2.00 |
| Overall tape thickness | T | 0.05 | 0.30 |
| Tape width | W | 0.3 | 12.00 |
| Reel width | $W_1$ | 3.0 | 12.40 |

Note:Devices are packed in accor dance with EIA standar RS-481-A and specifications listed above.

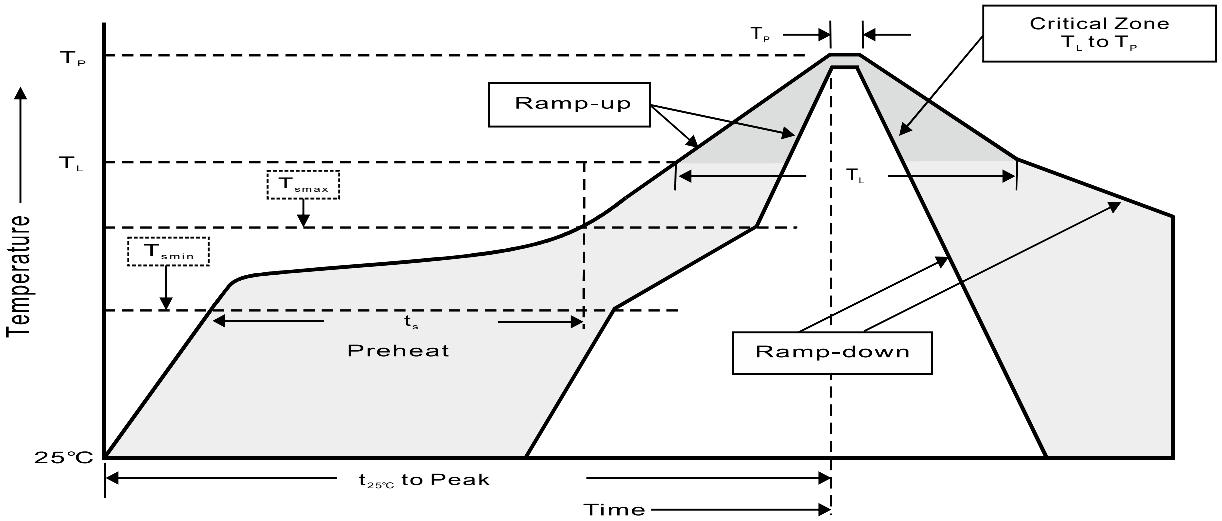
## Reel packing

| PACKAGE | REEL SIZE | REEL (pcs) | COMPONENT SPACING (m/m) | BOX (pcs) | INNER BOX (m/m) | REEL DIA, (m/m) | CARTON SIZE (m/m) | CARTON (pcs) |
|---|---|---|---|---|---|---|---|---|
| SOP8 (SOP-08) | 13" | 2,500 | 8.0 | 5,000 | 335*335*38 | 330 | 350*330*360 | 40,000 |

## Suggested thermal profiles for soldering processes

1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%

2.Reflow soldering of surface-mount devices



3.Reflow soldering

| Profile feature | Soldering condition |
|---|---|
| Average ramp-up rate ($T_L$ to $T_P$) | < 3 ℃/sec |
| Preheat<br>- Temperature Min ($T_{smin}$)<br>- Temperature Max ($T_{smax}$)<br>- Time (Min to Max) ($t_s$) | 150℃<br>200℃<br>60 ~ 120 sec |
| $T_{smax}$ to $T_L$<br>- Ramp-up rate | < 3 ℃/sec |
| Time maintained above :<br>- Temperature ($T_L$)<br>- Time ($T_L$) | 217℃<br>60 ~ 260 sec |
| Peak temperature ($T_P$) | 255 ℃ -0/+5℃ |
| Time with 5℃ of actual peak temperature ($T_P$) | 10 ~30 sec |
| Ramp-down rate | < 6 ℃/sec |
| Time 25℃ to peak temperature | < 6 minutes |