

FMOSGTAT42DN06-Q1-H**List**

List.....	1
Package outline.....	2
Features.....	2
Application.....	2
Mechanical data.....	2
Maximum ratings	2
Thermal Performance.....	2
Electrical characteristics.....	3
Rating and characteristic curves.....	4~5
Pinning information.....	6
Marking.....	6
Suggested solder pad layout.....	6
Packing information.....	7
Reel Packing.....	8
Suggested thermal profiles for soldering processes.....	8
High reliability test capabilities.....	9

FMOSGTAT42DN06-Q1-H**42A 60V Dual N-Channel Shield Gate
Trench Enhancement Mode Power MOSFET****Features**

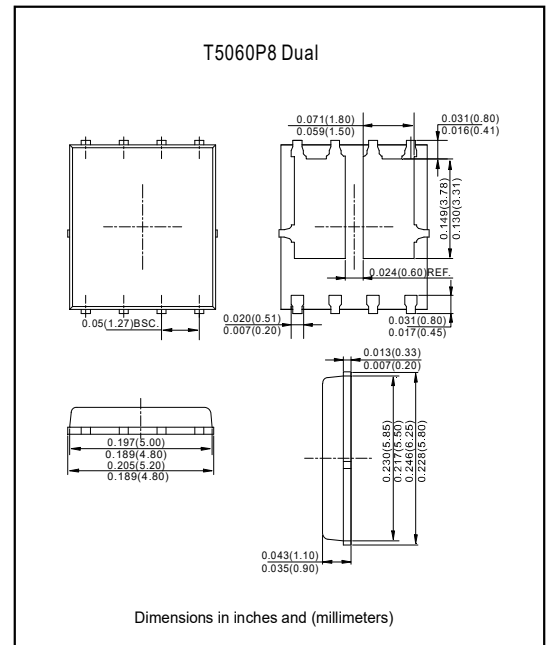
- $V_{DS}=60V$, $I_D=42A$.
- $R_{DS(ON)} \leq 11.2m\Omega$, @ $V_{GS}=10V$, $I_D=20A$.
- $R_{DS(ON)} \leq 15.8m\Omega$, @ $V_{GS}=4.5V$, $I_D=15A$.
- 100% UIS and R_g tested.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21) .

Application

- General automotive application.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, T5060P8 Dual (DFN5060-8 Dual) .
- Mounting Position : Any.

Package outline**Maximum ratings** (At $T_c=25^\circ C$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current @ $V_{GS}=10V$ (note 1)	I_D	42	A
($T_c=25^\circ C$) ($T_c=100^\circ C$)		30	
Pulse drain current tested (note 2)	I_{DM}	164	A
Avalanche current ($L=0.1mH$)	I_{AS}	19	A
Avalanche energy (note 3)	E_{AS}	54	mJ
Maximum power dissipation	P_D	38	W
($T_c=25^\circ C$) ($T_c=100^\circ C$)		19	
Thermal resistance, junction to ambient	$R_{\theta JA}$	68	$^\circ C/W$
Thermal resistance, junction to case	$R_{\theta JC}$	4	$^\circ C/W$
Maximum junction temperature	T_J	+175	$^\circ C$
Storage temperature range	T_{STG}	-55 to +175	$^\circ C$

FMOSGTAT42DN06-Q1-H

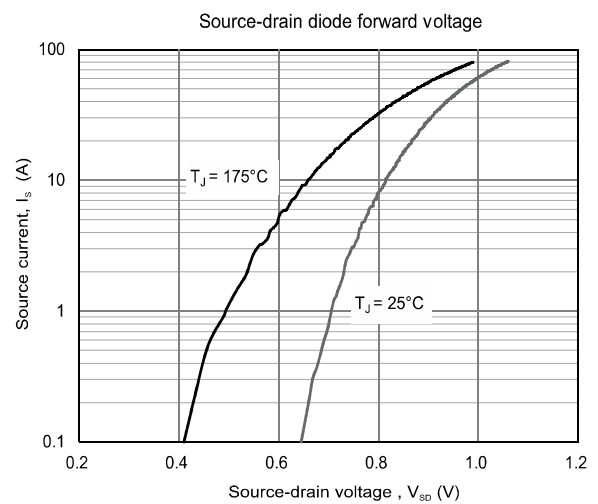
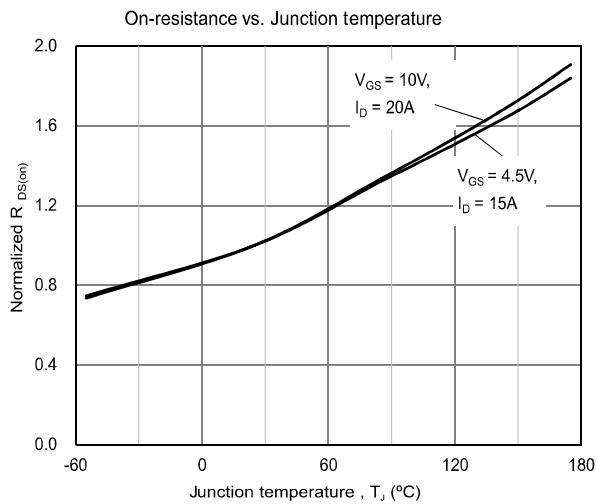
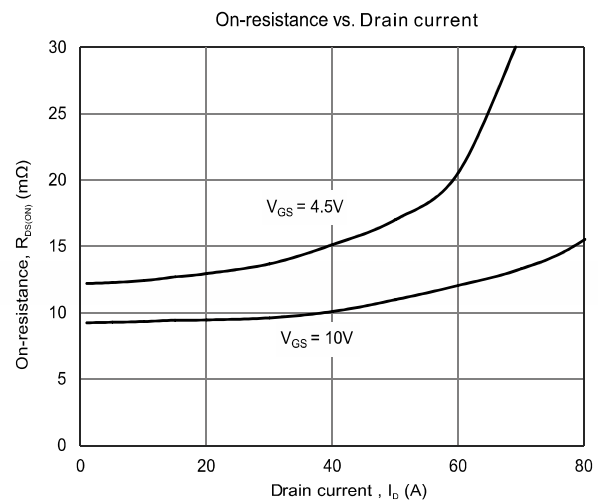
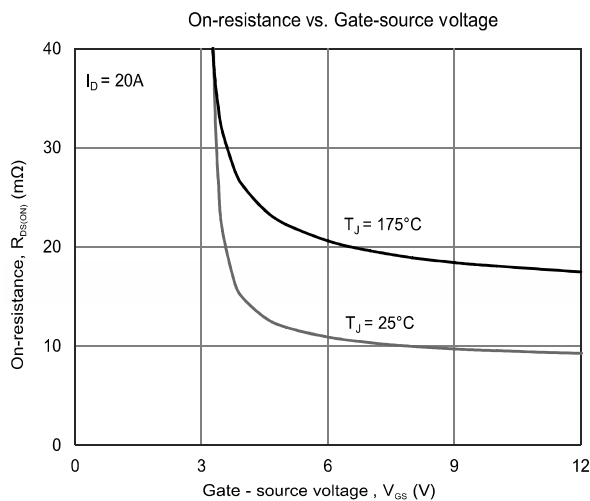
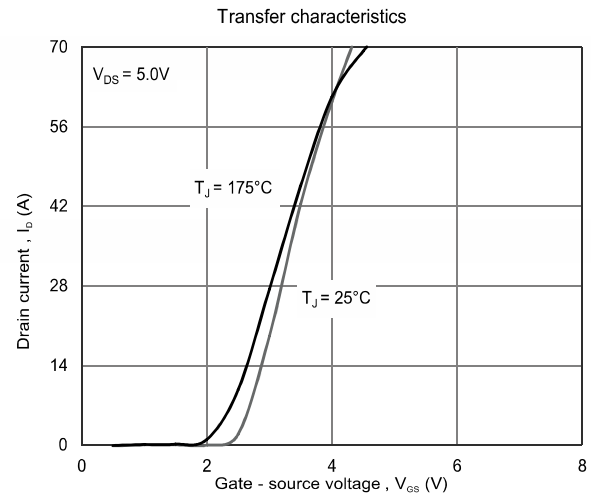
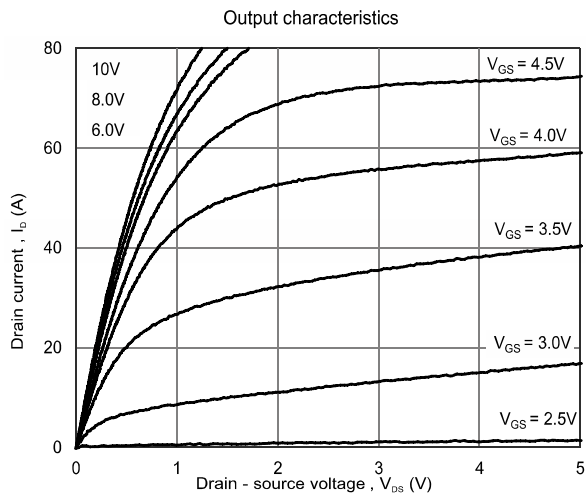
Electrical characteristics (Chip1 and Chip2) (At $T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off characteristics (Note 6)						
Drain-source breakdown voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	60			V
Drain-source leakage current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
		V _{DS} =60V, V _{GS} =0V, T _J =125°C			100	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
On characteristics (Note 6)						
Gate threshold voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.7	2.5	V
Static drain-source on-state resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		9.5	11.2	mΩ
		V _{GS} =4.5V, I _D =15A		12.5	15.8	mΩ
Forward transconductance	g _{FS}	V _{DS} =5V, I _D =20A		18		S
Dynamic parameters (Note 7)						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =30V, f=1.0MHz		596	775	pF
Out capacitance	C _{oss}			349	454	
Reverse transfer capacitance	C _{rss}			19	38	
Gate resistance	R _G	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		1.3		Ω
Switching parameters (Note 7)						
Total gate charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =20A		11.9	15.5	nC
Total gate charge		V _{GS} =4.5V, V _{DS} =30V, I _D =20A		5.9	7.7	
Gate to source charge	Q _{gs}	V _{GS} =10V, V _{DS} =30V, I _D =20A		2.0	3.0	
Gate to drain charge	Q _{gd}			2.7	4.1	
Gate plateau voltage	V _{plateau}			3.4		V
Turn-on delay time	t _{d(on)}	V _{DS} =30V, V _{GS} =10V, I _D =20A, R _{GEN} =3Ω		3.3		ns
Rise time	t _r			8.2		
Turn-off delay time	t _{d(off)}			11		
Fall time	t _f			4.3		
Source-drain diode ratings and characteristics (Note 7)						
Drain-source diode forward voltage	V _{SD}	I _S =2A, V _{GS} =0V		0.7	1.2	V
Diode continuous current	I _S	T _C =25°C			42	A
Reverse recovery time	t _{rr}	I _F =20A, dI/dt=100A/μs, T _J =25°C		25		ns
Reverse recovery charge	Q _{rr}				16	

Notes : 1. This current chip limited, which is calculated base on $R_{\theta JC}$.
2. This current is calculated on single pulse with $10\mu\text{s}$ pulse and duty cycle=1%.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^{\circ}\text{C}$, $V_{DS}=30\text{V}$, $V_{GS}=10\text{V}$, $L=1.0\text{mH}$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

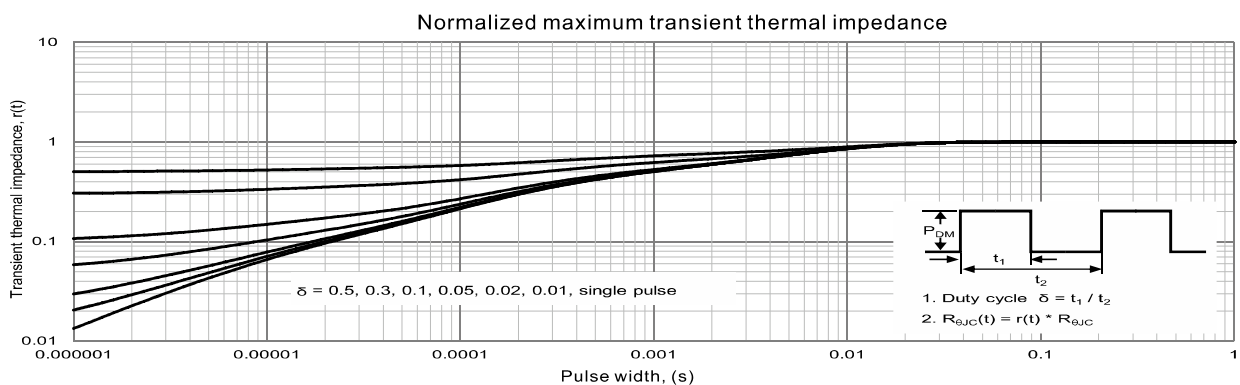
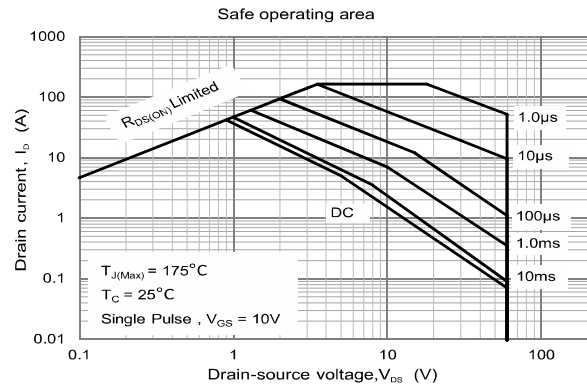
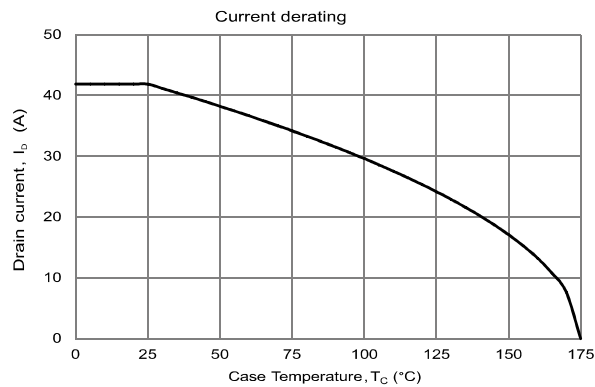
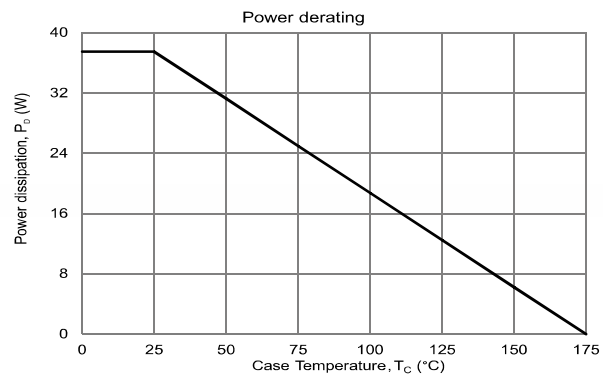
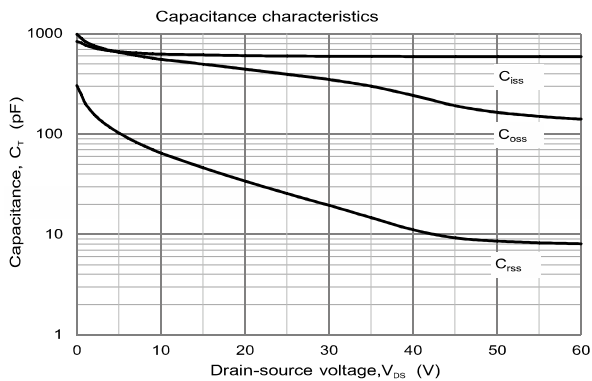
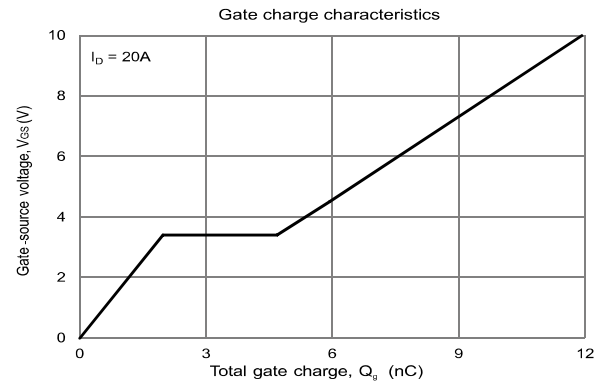
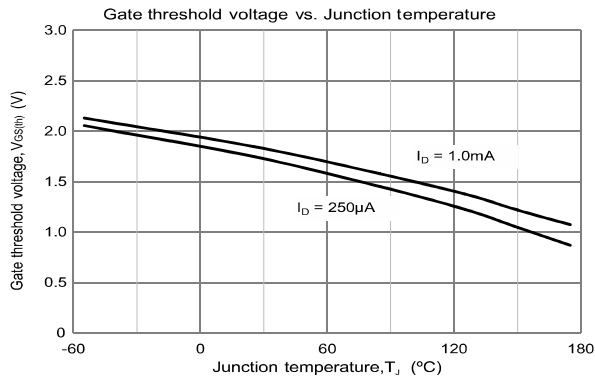
FMOSGTAT42DN06-Q1-H

Rating and characteristic curves (Chip1 and Chip2)



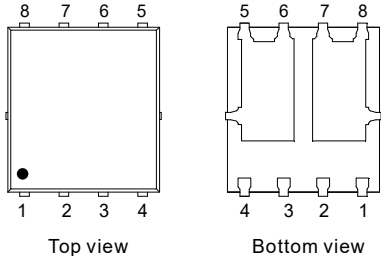
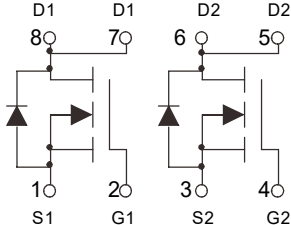
FMOSGTAT42DN06-Q1-H

Rating and characteristic curves (Chip1 and Chip2)



FMOSGTAT42DN06-Q1-H

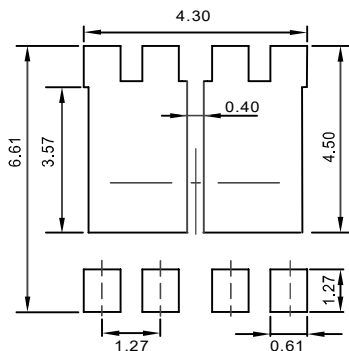
Pinning information

Pin	Simplified outline	Symbol
Pin 1 Source 1		
Pin 2 Gate 1		
Pin 3 Source 2		
Pin 4 Gate 2		
Pin 5, 6 Drain 2		
Pin 7, 8 Drain 1		

Marking

Type number	Marking code
FMOSGTAT42DN06-Q1-H	6012ALDQ

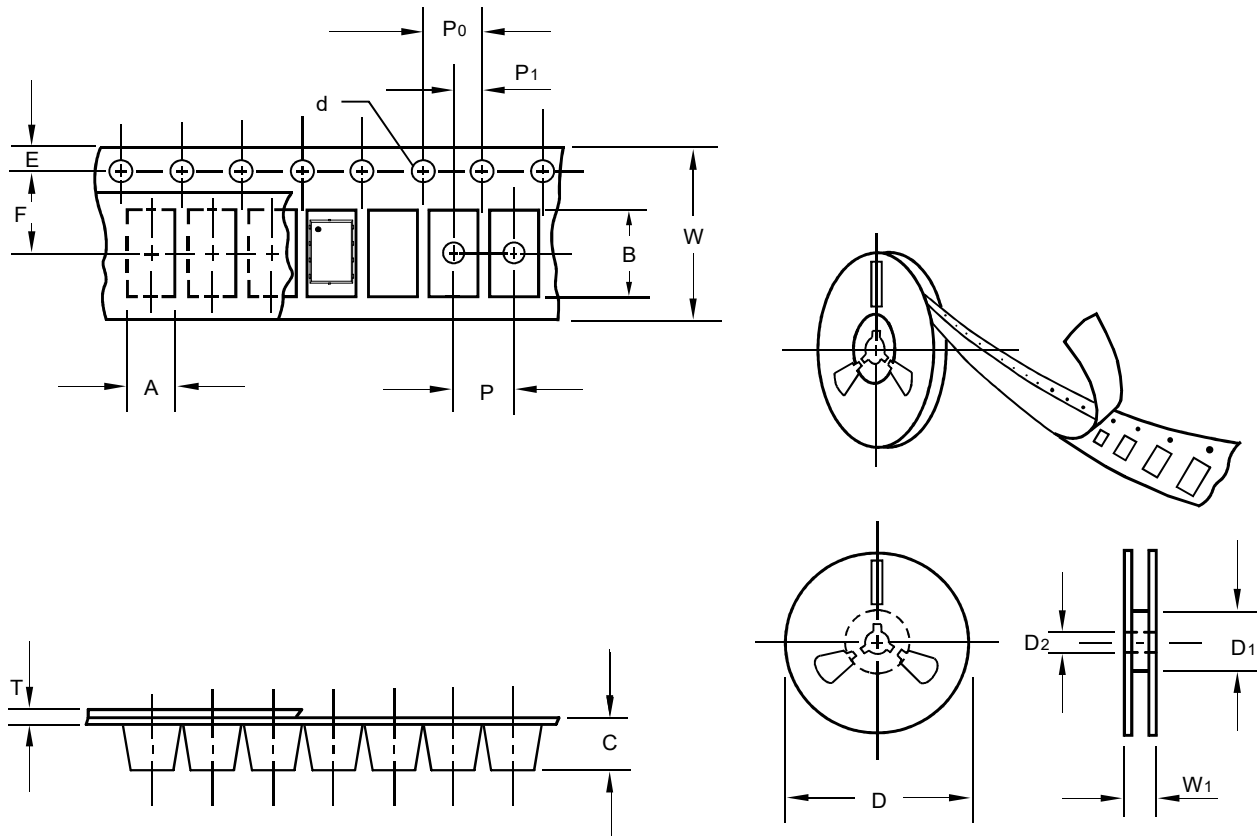
Suggested solder pad layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only.

FMOSGTAT42DN06-Q1-H

Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8 Dual
Carrier width	A	0.1	6.40
Carrier length	B	0.1	5.40
Carrier depth	C	0.1	1.25
Sprocket hole	d	0.1	1.55
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D ₁	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D ₁	min	-
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.30
Tape width	W	0.3	12.00
Reel width	W ₁	1.0	17.60

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

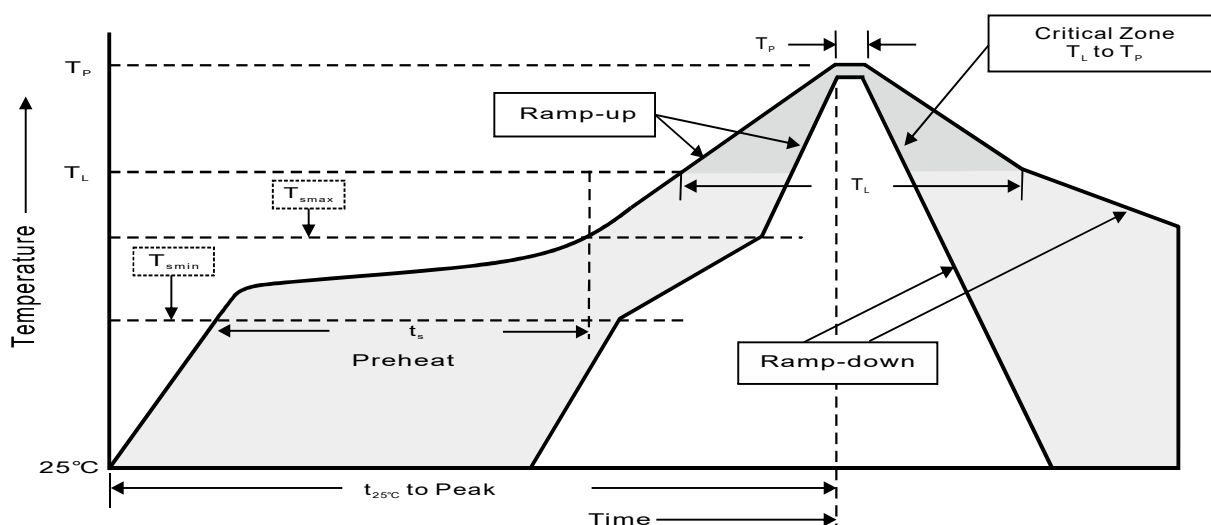
FMOSGTAT42DN06-Q1-H

Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
T5060P8 Dual	13"	5,000	4.0	10,000	335*335*38	330	350*350*360	80,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_p)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_p)	255 °C -0/+5°C
Time with 5°C of actual peak temperature (T_p)	10 ~30 sec
Ramp-down rate	< 6 °C/sec
Time 25°C to peak temperature	< 6 minutes

FMOSGTAT42DN06-Q1-H**High reliability test capabilities**

Item Test	Conditions	Reference
1. MSL Preconditioning	24hr bake@125°C+168hrs@85°C /85%RH+3xIR@260°C+1flux immersion+alcohol+DI H2O rinse	JESD22-A113
2. High Temperature Reverse Bias	$V_{DS}=V_{DS}^{*}80\%$ ($T_J=T_J^{max.}$)Test Duration:1000hrs	JESD22-A108
3. High Temperature Storage Life	$T_a=150^{\circ}\text{C}$ Test Duration:1000hrs	JESD22 A-103
4. Temperature Cycle	$-55^{\circ}\text{C}(15\text{min})$ to $150^{\circ}\text{C}(15\text{min})$ Test Cycles:1000cycles	JESD22 A-104
5. Autoclave	$P=2\text{atm}$ $T_a=121^{\circ}\text{C}$ RH=100% Test Duration:96hrs	JESD22 A-102
6. Solderability	$245\pm 5^{\circ}\text{C}$ for 5sec	J-STD-002
7. Moisture Resistance	$T_a=85^{\circ}\text{C}/85\%$ Relative humidity Test Duration:1000hrs	MIL-STD-750E METHOD 1021.2
8. Resistance To Solder Heat	$260\pm 5^{\circ}\text{C}$ for 10sec	JESD22 B-106
9. High Temperature High Humidity Reverse Bias	$T_a=85^{\circ}\text{C}$, 85%RH, $V_{DS}=80\%$ rated V_{DS} Test Duration: 1000hrs	JESD22-A101