

FMOSGTAC62N10-Q1-H

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FMOSGTAC62N10-Q1-H**62A 100V N-Channel Shield Gate Trench Enhancement Mode Power MOSFET****Features**

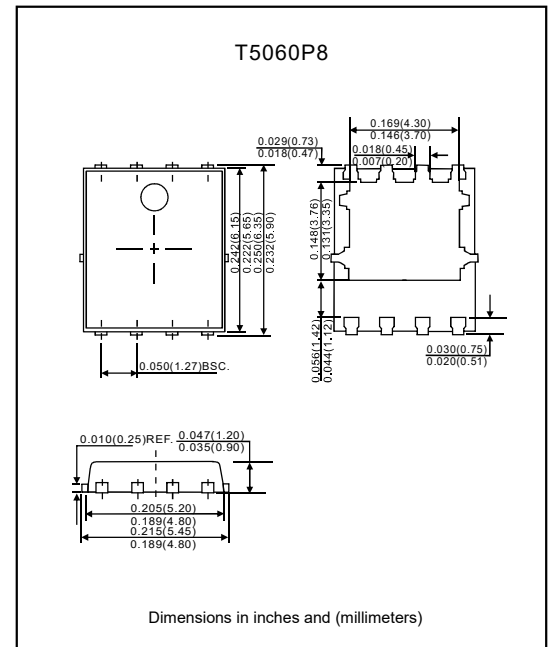
- $V_{DS}=100V$, $I_D=62A$.
- $R_{DS(ON)} \leq 9.0m\Omega$, @ $V_{GS}=10V$, $I_D=30A$.
- $R_{DS(ON)} \leq 11.4m\Omega$, @ $V_{GS}=4.5V$, $I_D=30A$.
- Good stability and uniformity with high E_{AS} .
- High density cell design for ultra-low on-resistance.
- Excellent package for good heat dissipation.
- Battery switch and load switch.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21).

Applications

- SMPS and general purpose applications.
- Uninterruptible power supply.
- Hard switching and high frequency circuit.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic,T5060P8.
- Mounting Position : Any.

Package outline**Maximum ratings** (At $T_J=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($T_c=25^\circ C$) (Note1) ($T_c=100^\circ C$)	I_D	62	A
		44	
Pulsed drain current (Note1,2)	I_{DM}	248	A
Single pulse avalanche energy (Note3)	E_{AS}	220	mJ
Power dissipation (Note1)	P_D	71	W
Thermal resistance, junction to ambient (Note4)	$R_{\theta JA}$	55	$^\circ C/W$
Thermal resistance, junction to case	$R_{\theta JC}$	2.1	$^\circ C/W$
Operating Junction temperature	T_J	+175	$^\circ C$
Storage temperature range	T_{STG}	-55 to +175	$^\circ C$

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Electrical characteristics (At $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	I _D =1mA, V _{GS} =0V	100			V
Drain-source leakage current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _J =25°C			1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =125°C			100	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
On characteristics (Note5)						
Gate threshold voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D =250μA	1.3	1.8	2.5	V
Static drain-source on-resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A		7.2	9.0	mΩ
		V _{GS} =4.5V, I _D =30A		9.1	11.4	
Dynamic parameters						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		2450		pF
Out capacitance	C _{oss}			990		
Reverse transfer capacitance	C _{rss}			47		
Gate resistance	R _g	f=1.0MHz		2		Ω
Switching parameters						
Total gate charge	Q _g	V _{GS} =10V, V _{DD} =50V, I _D =30A		48		nC
Gate to source charge	Q _{gs}			12		
Gate to drain charge	Q _{gd}			11		
Gate plateau voltage	V _{plateau}			2.9		V
Turn-on delay time	t _{d(on)}	V _{DD} =50V, V _{GS} =10V, R _G =2.5Ω, I _D =30A, R _L =1.67Ω		8.5		ns
Rise time	t _r			5.4		
Turn-off delay time	t _{d(off)}			30		
Fall time	t _f			8.0		
Source-drain diode ratings and characteristics						
Drain-source diode forward voltage (Note 5)	V _{SD}	I _S =30A, V _{GS} =0V			1.1	V
Continuous source current (Note 1)	I _S				62	A
Pulsed drain-source diode forward (Note 1,2)	I _{SM}				248	A
Reverse recovery time	t _{rr}	V _R =50V, I _F =30A, di _F /dt=100A/μs		65		ns
Reverse recovery charge	Q _{rr}			75		nC

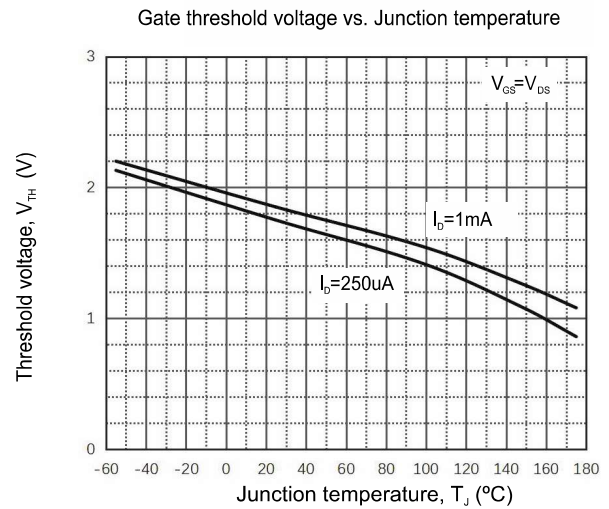
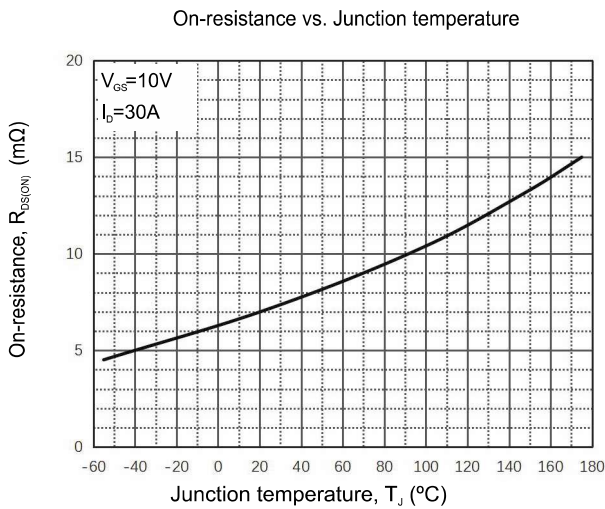
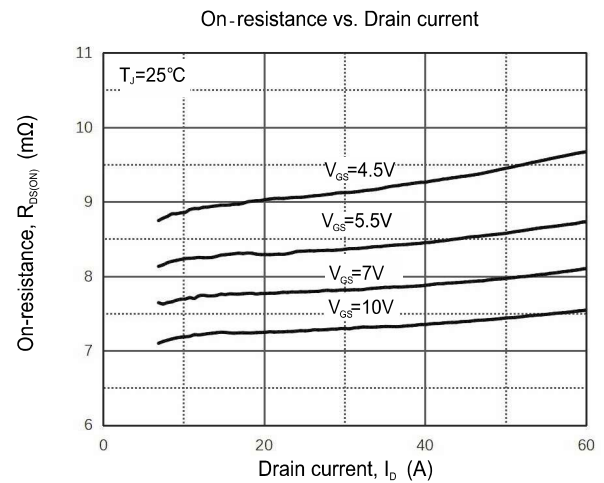
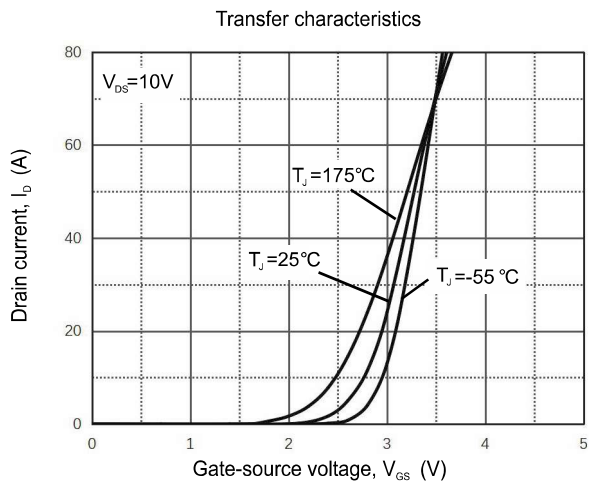
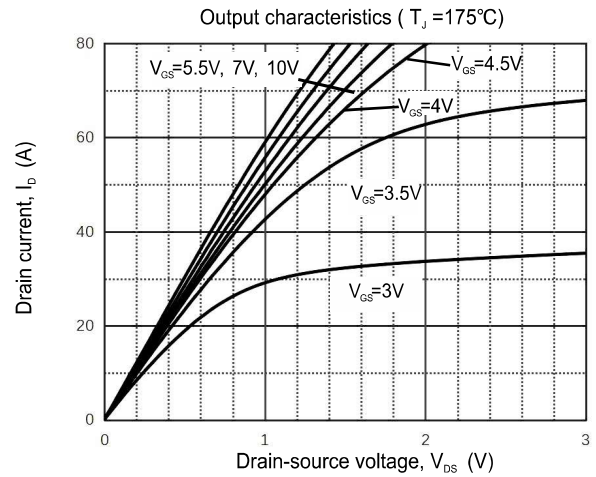
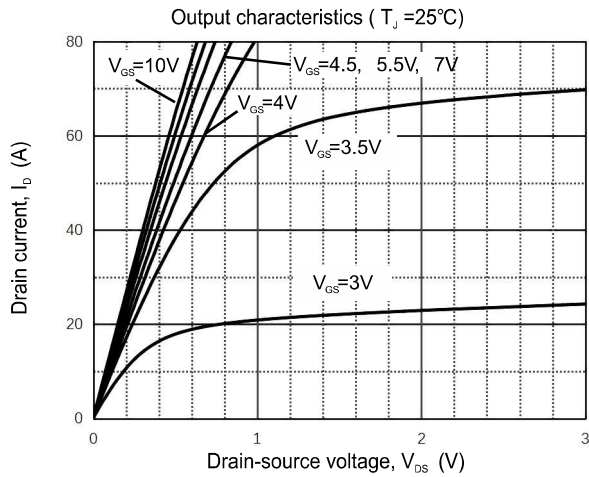
Note : 1. $T_c=25^\circ\text{C}$, $R_{\theta JC}=2.1^\circ\text{C}/\text{W}$.

2. Limited by maximum junction temperature.

3. Test condition: $V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$, starting at $T_J=25^\circ\text{C}$.4. Measured with the device mounted on 1 inch² FR-4 board with 2oz. copper, in a still air environment with $T_A=25^\circ\text{C}$.5. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

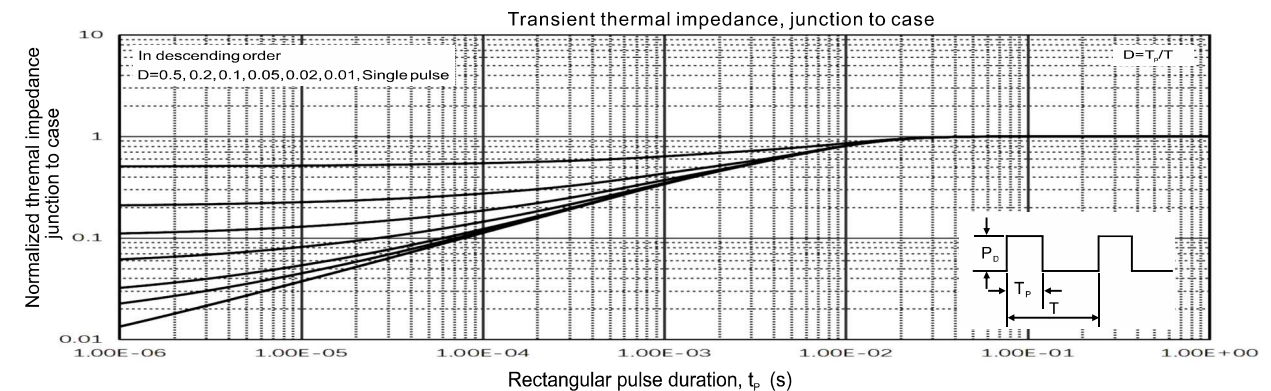
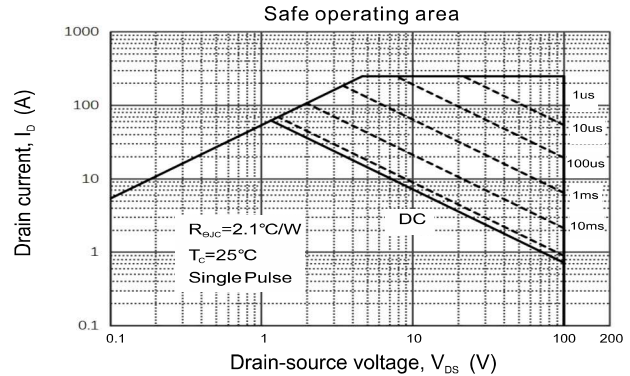
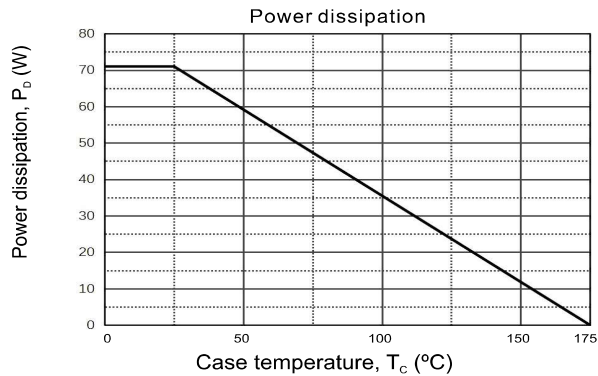
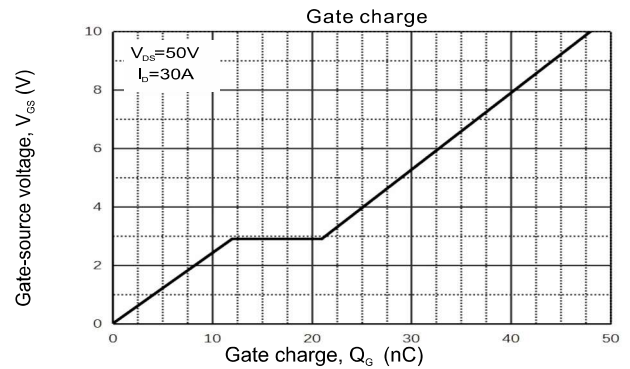
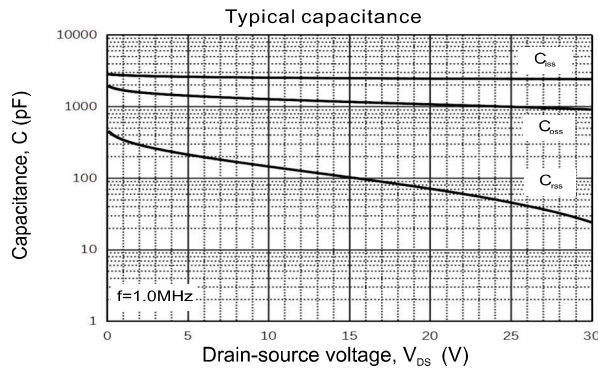
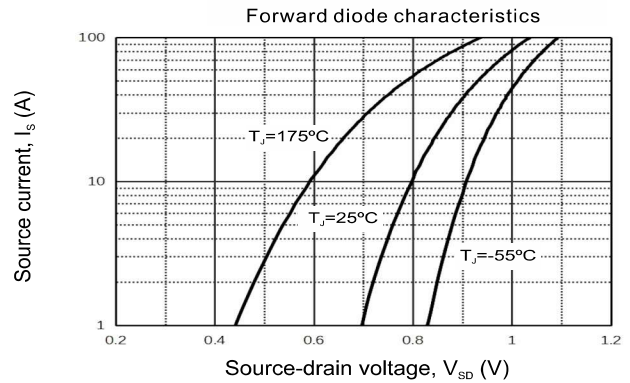
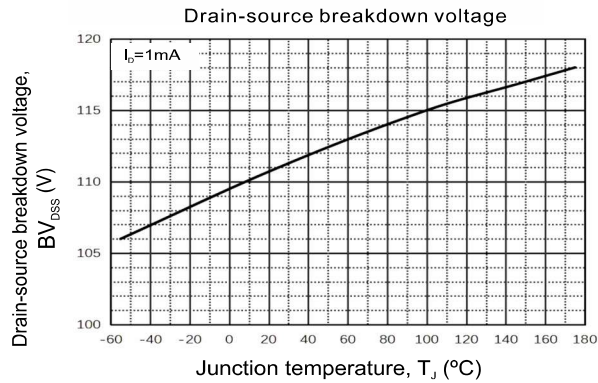
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Rating and characteristic curves



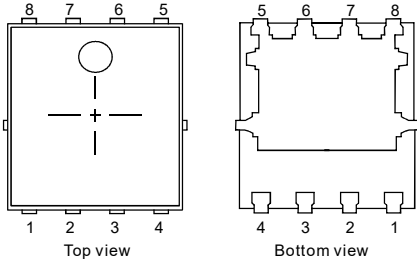
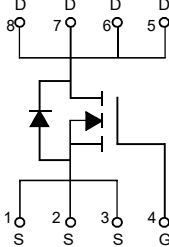
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Rating and characteristic curves



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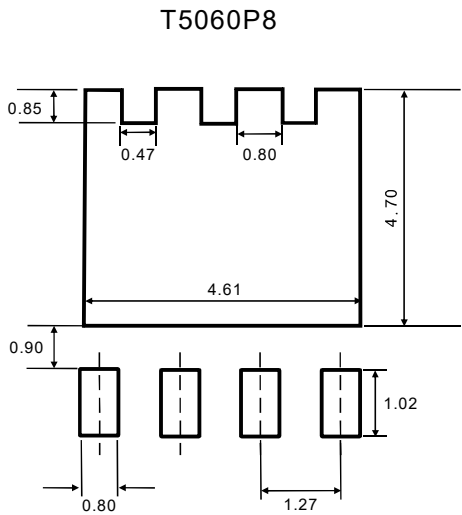
Pinning information

Pin	Simplified outline	Symbol
Pin 1, 2, 3, Source Pin 4 Gate Pin 5, 6, 7, 8 Drain		

Marking

Type number	Marking code
FMOSGTAC62N10-Q1-H	AC62N10

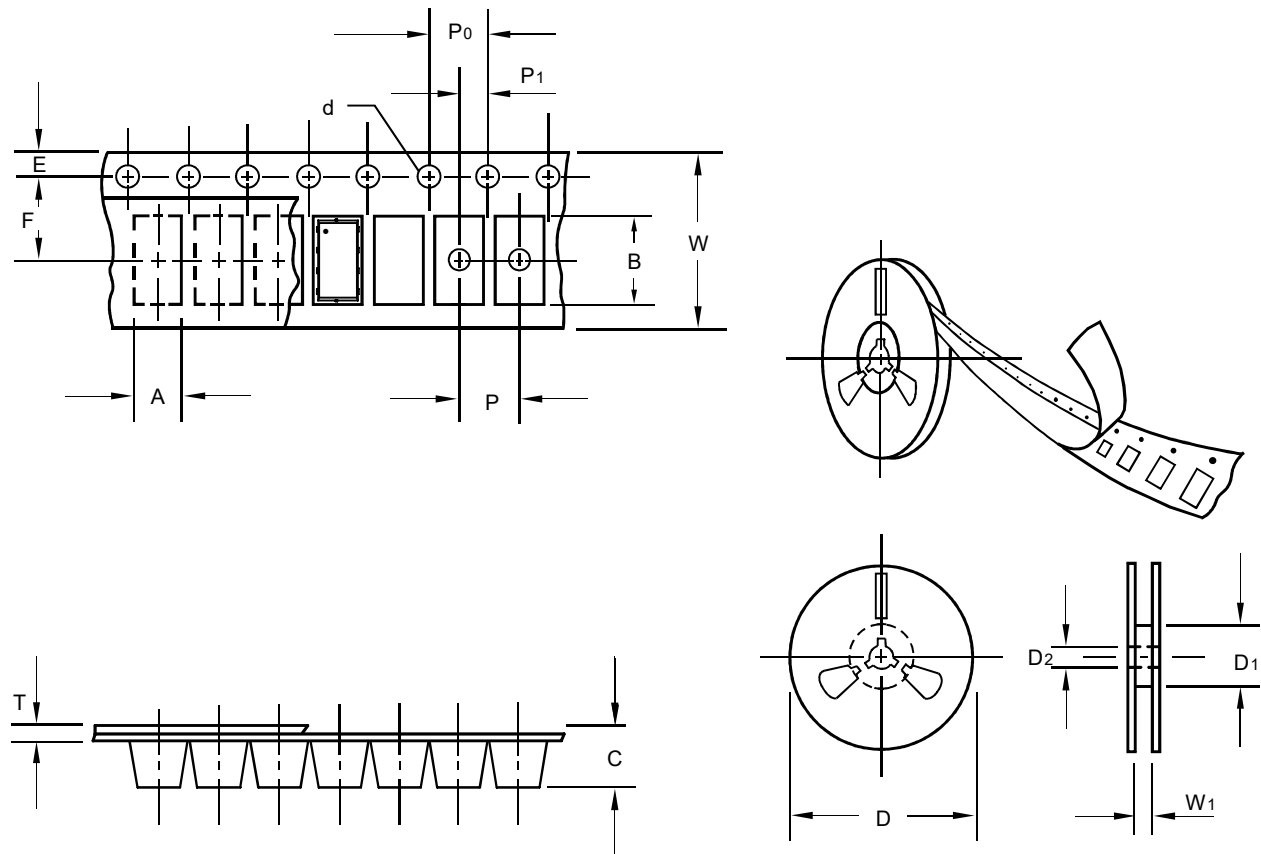
Suggested solder pad layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.1\text{mm}$
3. The pad layout is for reference purposes only.

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Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8
Carrier width	A	0.1	6.30
Carrier length	B	0.1	5.30
Carrier depth	C	0.1	1.10
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D1	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D1	min	-
Feed hole diameter	D2	0.5	13.50
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Tape width	W	0.3	12.00
Reel width	W1	1.0	12.40

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

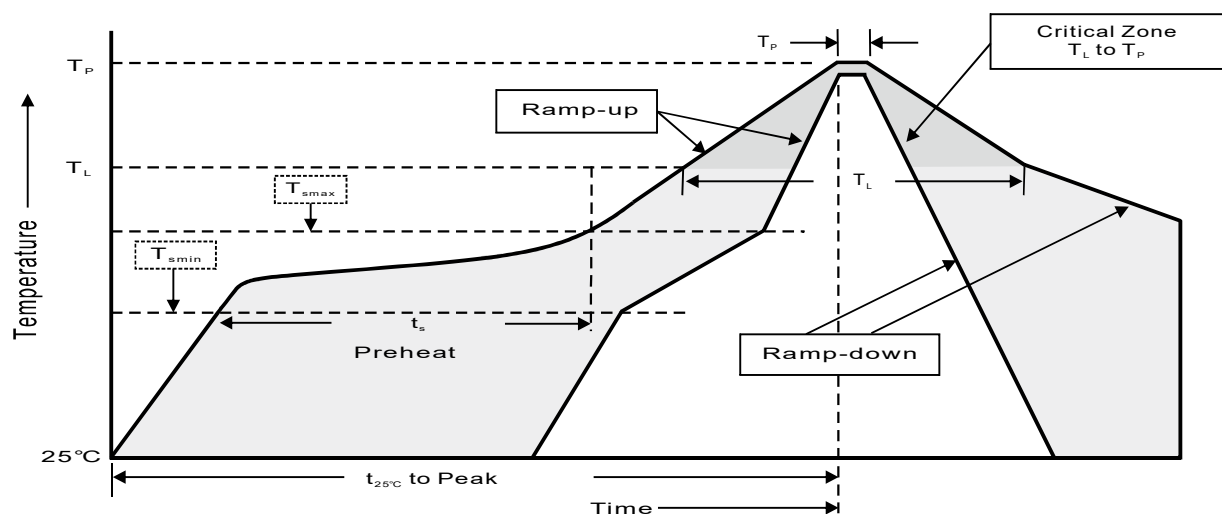
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Reel packing

Device	Outline	Device Package	Reel Size	Reel (pcs)
FMOSGTAC62N10-Q1-H	Taping	T5060P8	13 inch	5,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_p)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_p)	255 °C -0/+5°C
Time with 5°C of actual peak temperature (T_p)	10 ~30 sec
Ramp-down rate	< 6 °C/sec
Time 25°C to peak temperature	< 6 minutes

FMOSGTAC62N10-Q1-H**High reliability test capabilities**

Item Test	Conditions	Reference
1. MSL Preconditioning	24hr bake@125°C+168hrs@85°C /85%RH+3xIR@260°C+1flux immersion+alcohol+DI H2O rinse	JESD22-A113
2. High Temperature Reverse Bias	$V_{DS}=V_{DS}^*80\%$ ($T_J=T_J \text{ max.}$) Test Duration:1000hrs	JESD22-A108
3. High Temperature Storage Life	$T_a=150^\circ\text{C}$ Test Duration:1000hrs	JESD22 A-103
4. Temperature Cycle	-55°C (15min) to 150°C (15min) Test Cycles:1000cycles	JESD22 A-104
5. Autoclave	$P=2\text{atm}$ $T_a=121^\circ\text{C}$ RH=100% Test Duration:96hrs	JESD22 A-102
6. Solderability	$245\pm5^\circ\text{C}$ for 5sec	J-STD-002
7. Moisture Resistance	$T_a=85^\circ\text{C}$ /85% Relative humidity Test Duration:1000hrs	MIL-STD-750E METHOD 1021.2
8. Resistance To Solder Heat	$260\pm5^\circ\text{C}$ for 10sec	JESD22 B-106
9. High Temperature High Humidity Reverse Bias	$T_a=85^\circ\text{C}$, 85%RH, $V_{DS}=80\%$ rated V_{DS} Test Duration: 1000hrs	JESD22-A101