

FMOSGTAC333N04-Q1-H

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FMOSGTAC333N04-Q1-H**333A 40V N-Channel Shield Gate Trench Enhancement Mode Power MOSFET****Features**

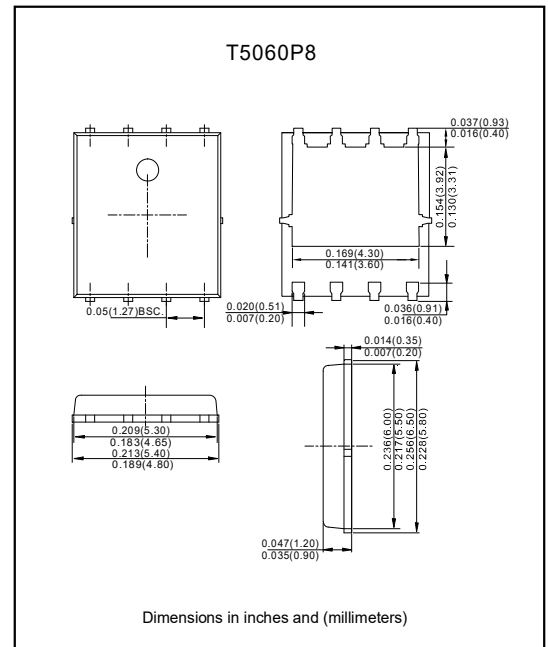
- $V_{DS}=40V$, $I_D=333A$.
- $R_{DS(ON)} \leq 0.85m\Omega$, @ $V_{GS}=10V$, $I_D=20A$.
- 100% ΔV_{DS} and UIS and R_g tested.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21) .

Application

- General automotive applications.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, T5060P8 (DFN5060-8).
- Weight : Approximated 105mg.

Package outline**Maximum ratings** (At $T_c=25^\circ C$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current @ $V_{GS}=10V$ (note 1)	I_D	333	A
		235	
Pulse drain current tested (note 2)	I_{DM}	1331	A
Avalanche current (L=0.3mH)	I_{AS}	55	A
Avalanche energy (note 3)	E_{AS}	1040	mJ
Maximum power dissipation	P_D	158	W
		79	
Thermal resistance, junction to ambient (note 4)	$R_{\theta JA}$	40	$^\circ C/W$
Thermal resistance, junction to case (note 5)	$R_{\theta JC}$	0.95	$^\circ C/W$
Maximum junction temperature	T_J	+175	$^\circ C$
Storage temperature range	T_{STG}	-55 to +175	$^\circ C$

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Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics (Note 6)						
Drain-source breakdown voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-source leakage current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
		V _{DS} =40V, V _{GS} =0V, T _J =125°C			100	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
On characteristics (Note 6)						
Gate threshold voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Static drain-source on-state resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		0.70	0.85	mΩ
Forward transconductance	g _{FS}	V _{DS} =5V, I _D =20A		63		S
Dynamic parameters (Note 7)						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =20V, f=1.0MHz		5912	7686	pF
Out capacitance	C _{oss}			3225	4193	
Reverse transfer capacitance	C _{rss}			111	222	
Gate resistance	R _G	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		2.2		Ω
Switching parameters (Note 7)						
Total gate charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =20A		76	99	nC
Total gate charge		V _{GS} =6V, V _{DS} =20V, I _D =20A		47	61	
Gate to source charge	Q _{gs}	V _{GS} =10V, V _{DS} =20V, I _D =20A		26	39	
Gate to drain charge	Q _{gd}			12.6	19	
Gate plateau voltage	V _{plateau}			4.8		V
Turn-on delay time	t _{d(on)}	V _{DS} =20V, V _{GS} =10V, I _D =20A, R _{GEN} =3Ω		15		ns
Rise time	t _r			25		
Turn-off delay time	t _{d(off)}			46		
Fall time	t _f			23		
Source-drain diode ratings and characteristics						
Drain-source diode forward voltage (Note 6)	V _{SD}	I _S =2.0A, V _{GS} =0V		0.7	1.2	V
Diode continuous current (Note 7)	I _S	T _C =25°C			333	A
Reverse recovery time (Note 7)	t _{rr}	I _F =20A, dI/dt=100A/μs, T _J =25°C		65		ns
Reverse recovery charge (Note 7)	Q _{rr}			104		nC

Note : 1. This current chip limited, which is calculated base on $R_{\theta JC}$.2. This current is calculated on single pulse with $10\mu\text{s}$ pulse and duty cycle=1%.3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^{\circ}\text{C}$, $V_{DS}=20\text{V}$, $V_{GS}=10\text{V}$, $L=1.0\text{mH}$.

4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.

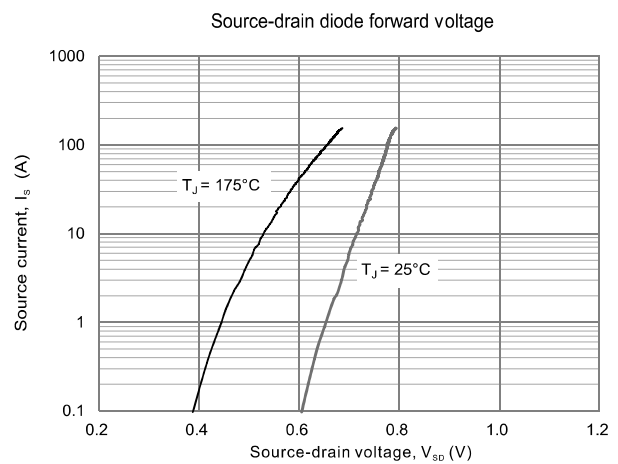
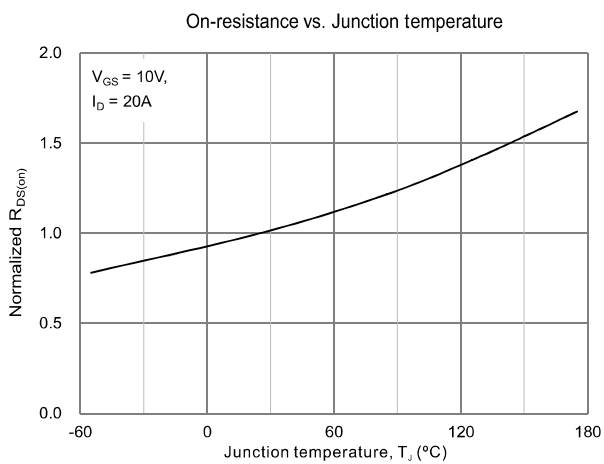
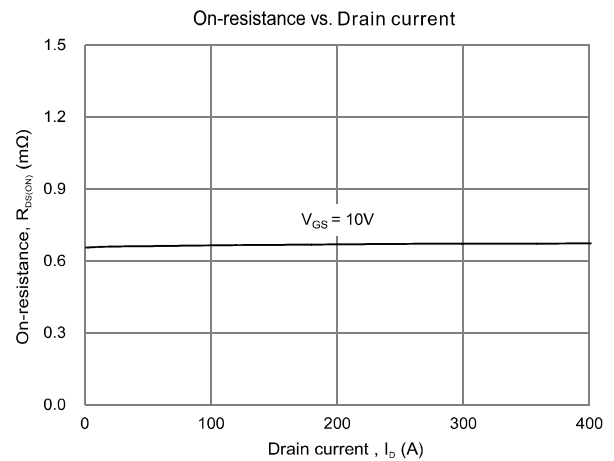
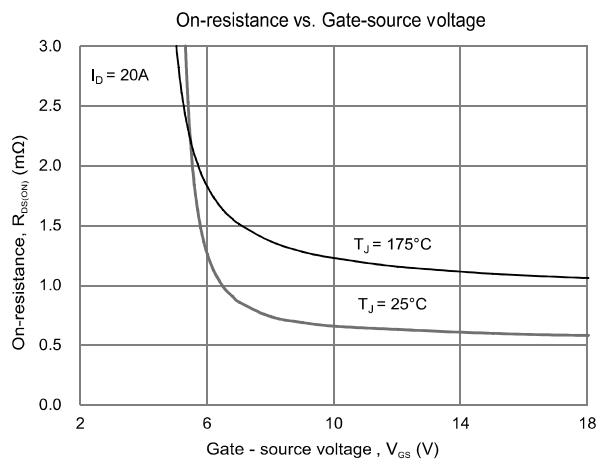
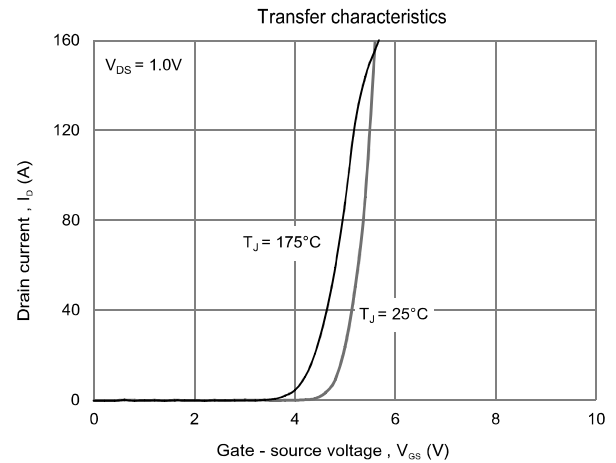
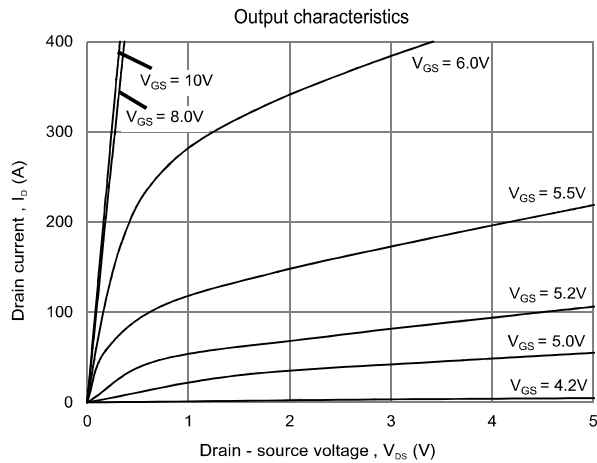
5. Thermal resistance from junction to soldering point (on the exposed drain pad).

6. Short duration pulse test used to minimize self-heating effect.

7. Defined by design, not subject to production.

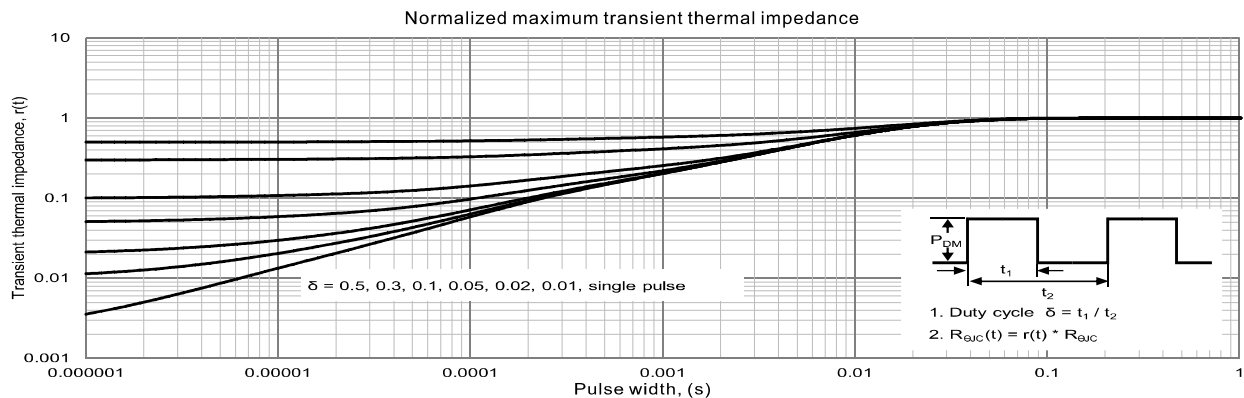
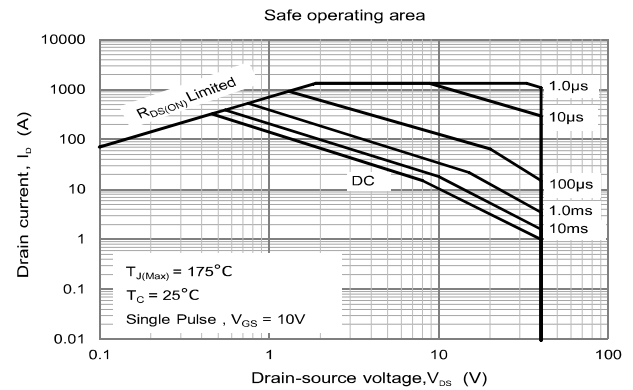
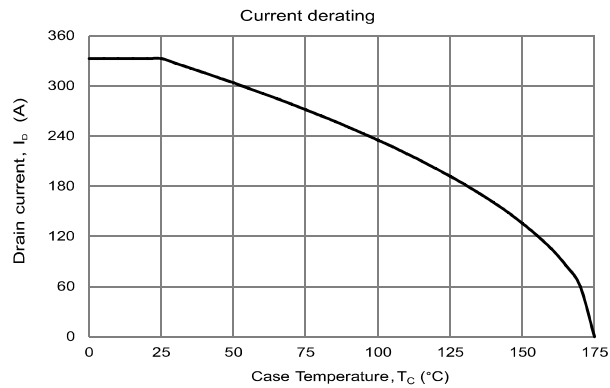
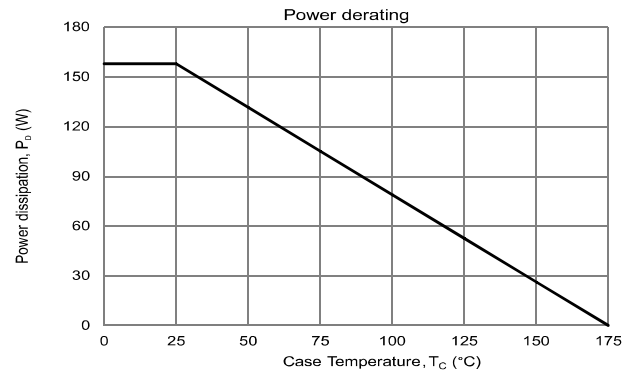
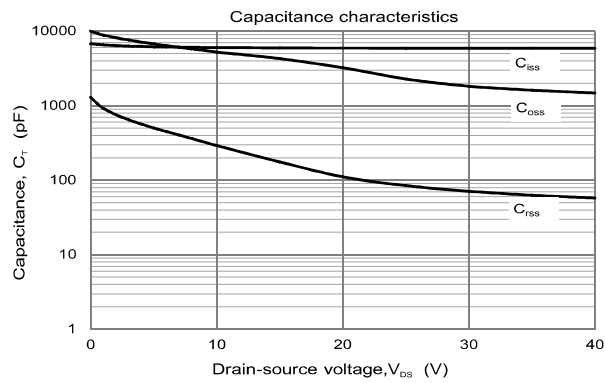
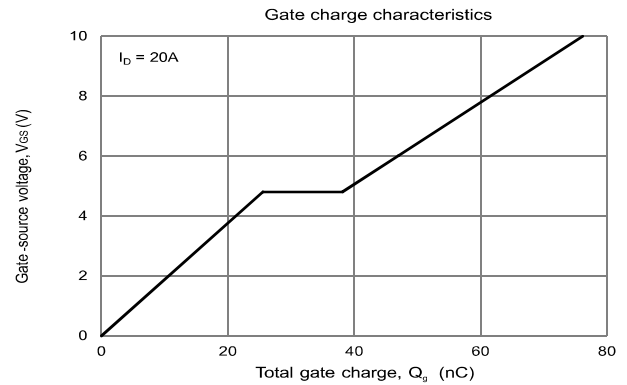
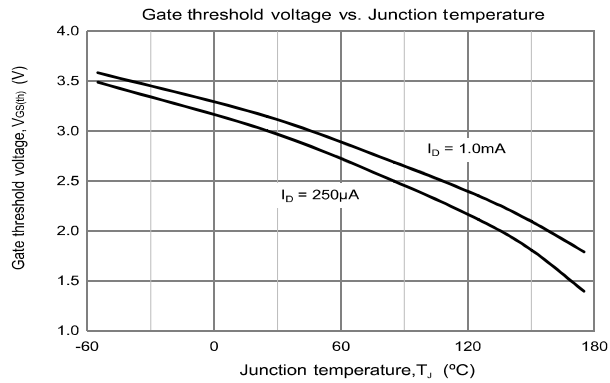
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Rating and characteristic curves



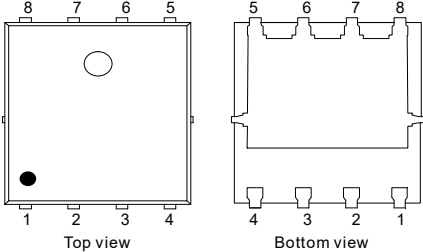
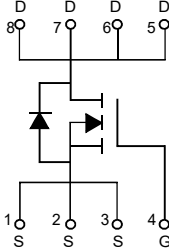
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Rating and characteristic curves



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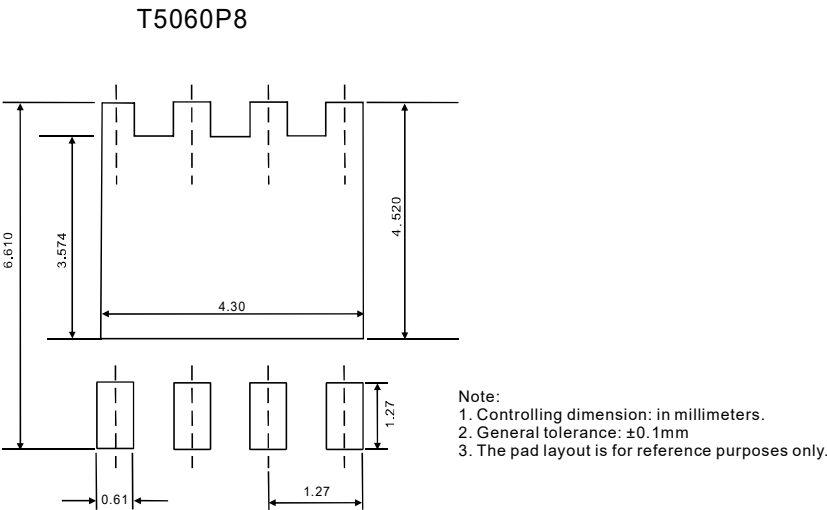
Pinning information

Pin	Simplified outline	Symbol
Pin 1, 2, 3, Source Pin 4 Gate Pin 5, 6, 7, 8 Drain	 Top view Bottom view	

Marking

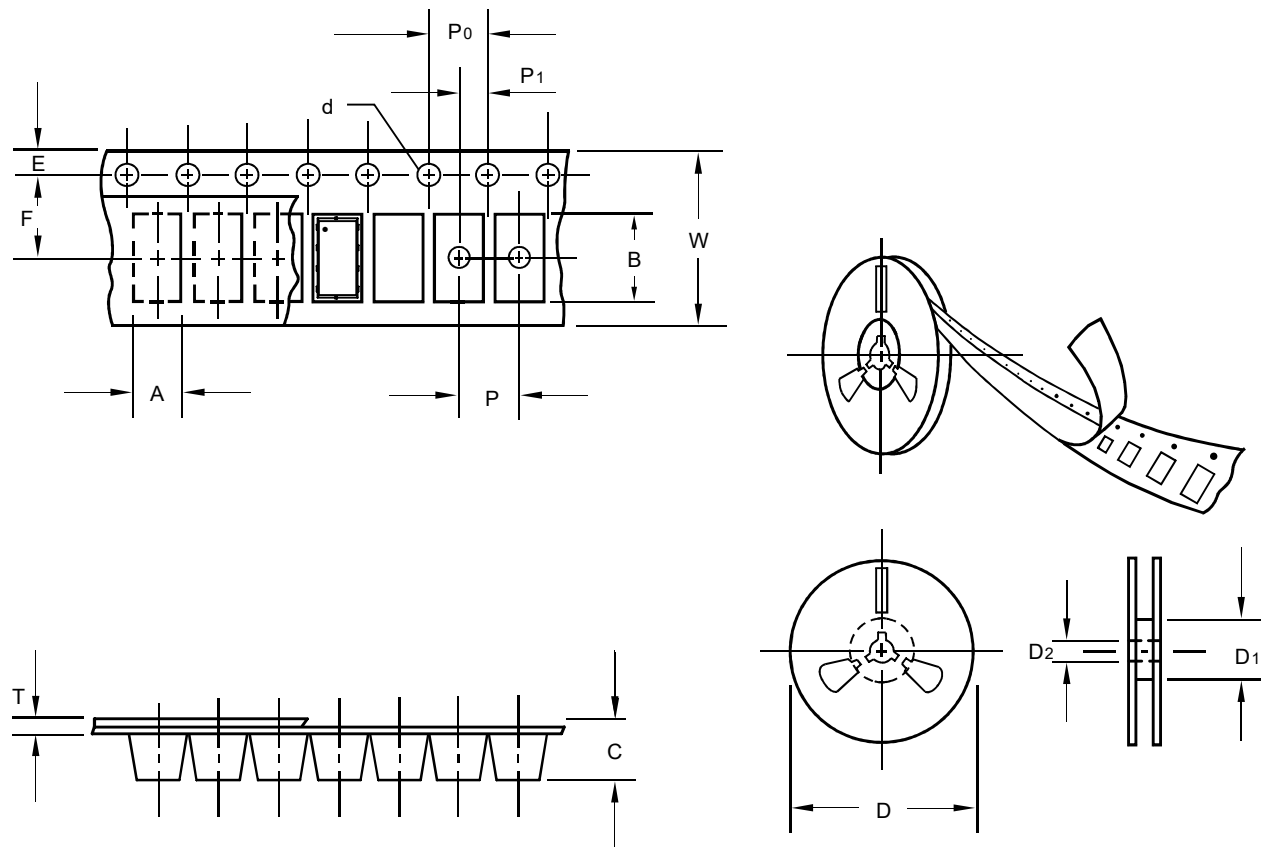
Type number	Marking code
FMOSGTAC333N04-Q1-H	400SAHQ

Suggested solder pad layout



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Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8
Carrier width	A	0.5	6.40
Carrier length	B	0.5	5.40
Carrier depth	C	0.5	1.25
Sprocket hole	d	0.5	1.55
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D ₁	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D ₁	min	-
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.30
Tape width	W	0.5	12.00

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

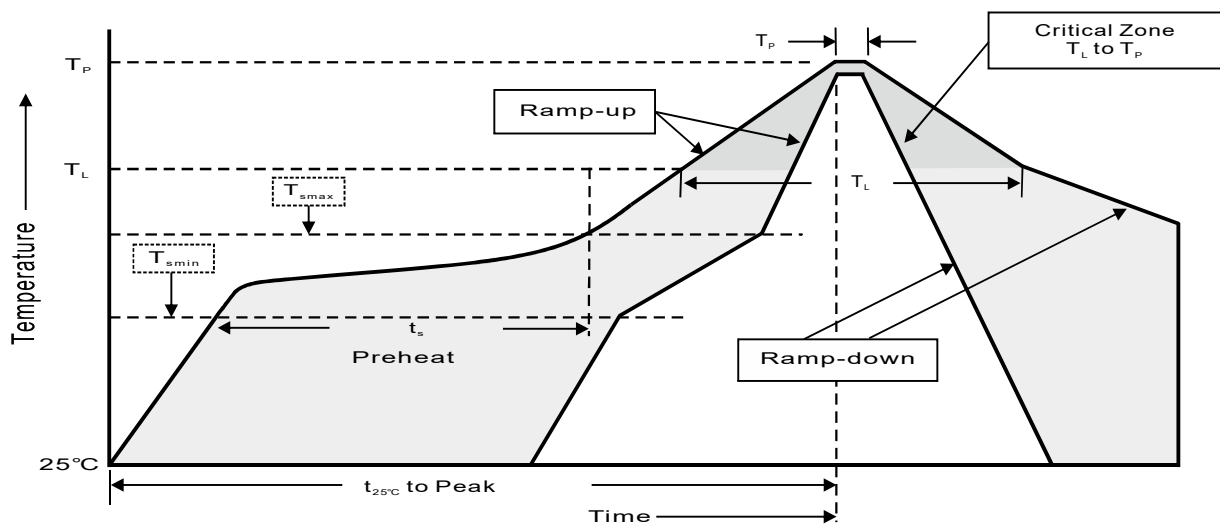
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
T5060P8	13"	5,000	4.0	10,000	335*335*38	330	350*350*360	80,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_p)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_p)	255 °C -0/+5°C
Time with 5°C of actual peak temperature (T_p)	10 ~30 sec
Ramp-down rate	< 6 °C/sec
Time 25°C to peak temperature	< 6 minutes