

FMOSGTAB67N04-Q1-H

List

List.....1

Package outline.....2

Features.....2

Application.....2

Mechanical data.....2

Maximum ratings2

Thermal Performance.....2

Electrical characteristics.....3

Rating and characteristic curves.....4~5

Pinning information.....6

Marking.....6

Suggested solder pad layout.....6

Packing information.....7

Reel Packing.....8

Suggested thermal profiles for soldering processes.....8

High reliability test capabilities.....9

FMOSGTAB67N04-Q1-H

67A 40V N-Channel Shield Gate
Trench Enhancement Mode Power MOSFET

Features

- $V_{DS} = 40V$, $I_D = 67A$.
- $R_{DS(ON)} \leq 4.7\text{ m}\Omega$, @ $V_{GS} = 10V$, $I_D = 20A$.
- $R_{DS(ON)} \leq 7.2\text{ m}\Omega$, @ $V_{GS} = 4.5V$, $I_D = 15A$.
- 100% UIS and R_g tested.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Halogen-free (IEC61249-2-21) .

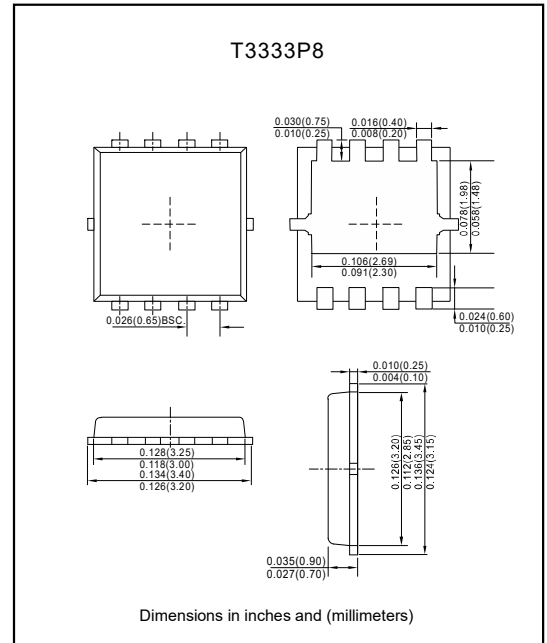
Application

- General automotive application.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, T3333P8.
- Mounting Position : Any.

Package outline

Maximum ratings (At $T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current @ $V_{GS} = 10V$ (note 1)	I_D	67	A
		47	
Pulse drain current tested (note 2)	I_{DM}	223	A
Avalanche current (L=0.1mH)	I_{AS}	27	A
Avalanche energy (note 3)	E_{AS}	102	mJ
Maximum power dissipation	P_D	38	W
		19	
Thermal resistance, junction to ambient (note 4)	$R_{\theta JA}$	63	$^\circ\text{C/W}$
Thermal resistance, junction to case (note 5)	$R_{\theta JC}$	3.9	$^\circ\text{C/W}$
Maximum junction temperature	T_J	+175	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 to +175	$^\circ\text{C}$

FMOSGTAB67N04-Q1-H

Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off characteristics (Note 6)						
Drain-source breakdown voltage	BV_{DS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	40			V
Drain-source leakage current	I_{DSS}	$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$			1	μA
		$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^{\circ}\text{C}$			100	
Gate-source leakage current	I_{GSS}	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$			± 100	nA

On characteristics (Note 6)

Gate threshold voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.2	1.7	2.5	V
Static drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=20\text{A}$		3.9	4.7	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=15\text{A}$		5.7	7.2	
Forward transconductance	g_{FS}	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		25		S

Dynamic parameters (Note 7)

Input capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1.0\text{MHz}$		994	1292	pF
Out capacitance	C_{oss}			602	783	
Reverse transfer capacitance	C_{rss}			23	46	
Gate resistance	R_G	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1.0\text{MHz}$		4.1		Ω

Switching parameters (Note 7)

Total gate charge	Q_g	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=20\text{A}$		14.3	18.6	nC
Total gate charge		$V_{GS}=4.5\text{V}$, $V_{DS}=20\text{V}$, $I_D=20\text{A}$		6.7	8.7	
Gate to source charge	Q_{gs}	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=20\text{A}$		3.1	4.7	
Gate to drain charge	Q_{gd}			1.8	2.7	
Gate plateau voltage	$V_{plateau}$			3.2		V
Turn-on delay time	$t_{d(on)}$	$V_{DS}=20\text{V}$, $V_{GS}=10\text{V}$, $I_D=20\text{A}$, $R_{GEN}=3\Omega$		1.3		ns
Rise time	t_r			12		
Turn-off delay time	$t_{d(off)}$			17		
Fall time	t_f			12		

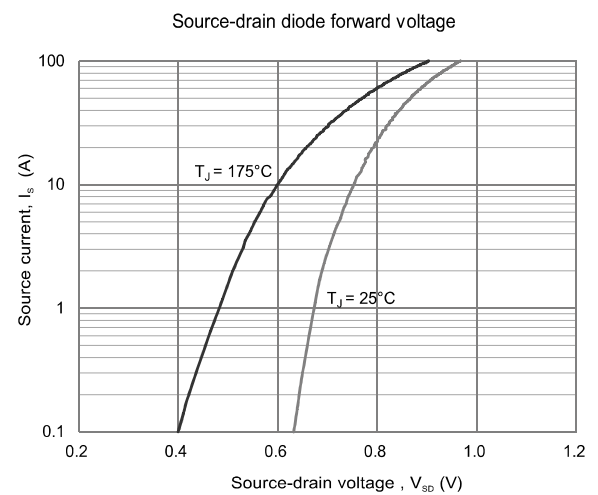
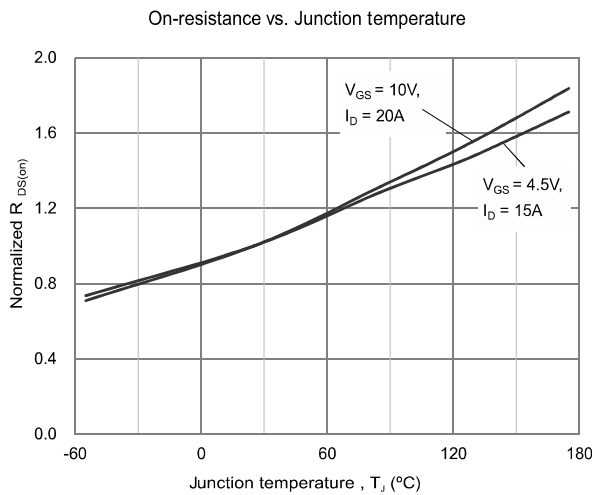
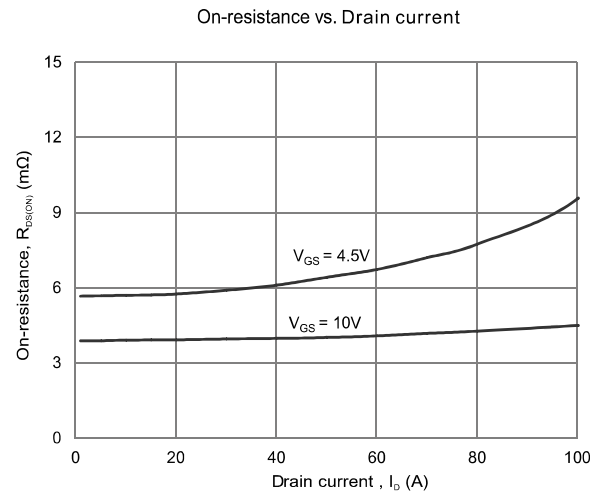
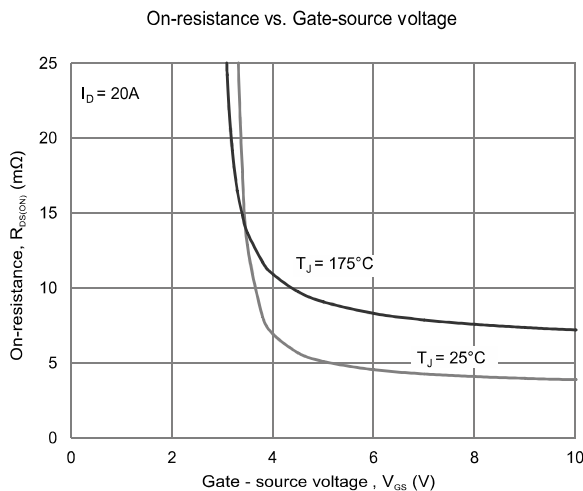
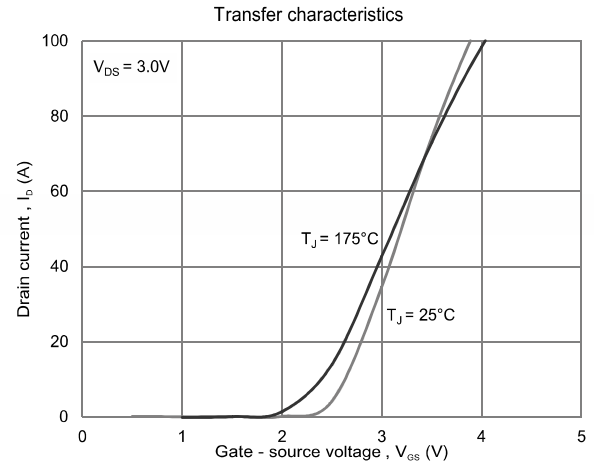
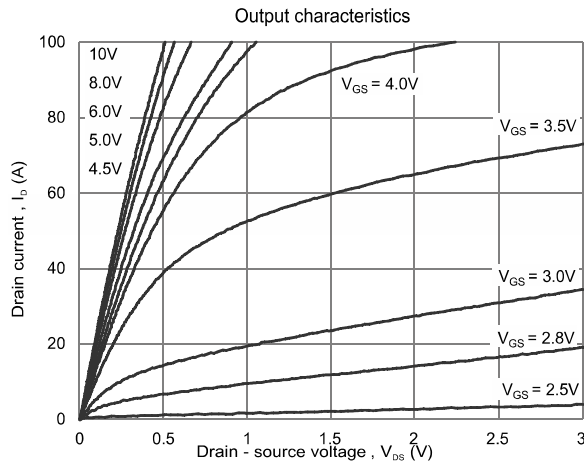
Source-drain diode ratings and characteristics

Drain-source diode forward voltage (Note 6)	V_{SD}	$I_S=2\text{A}$, $V_{GS}=0\text{V}$		0.7	1.2	V
Diode continuous current (Note 7)	I_S	$T_C=25^{\circ}\text{C}$			67	A
Reverse recovery time (Note 7)	t_{rr}	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$, $T_J=25^{\circ}\text{C}$		30		ns
Reverse recovery charge (Note 7)	Q_{rr}			11		nC

- Notes : 1. This current chip limited, which is calculated base on $R_{\theta JC}$.
2. This current is calculated on single pulse with $10\mu\text{s}$ pulse and duty cycle=1%.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^{\circ}\text{C}$, $V_{GS}=20\text{V}$, $V_{DS}=10\text{V}$, $L=1.0\text{mH}$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

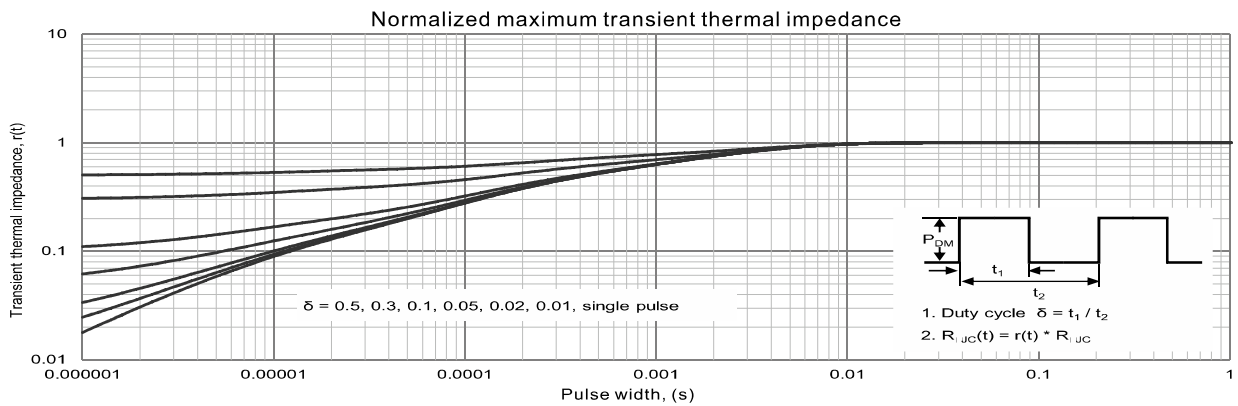
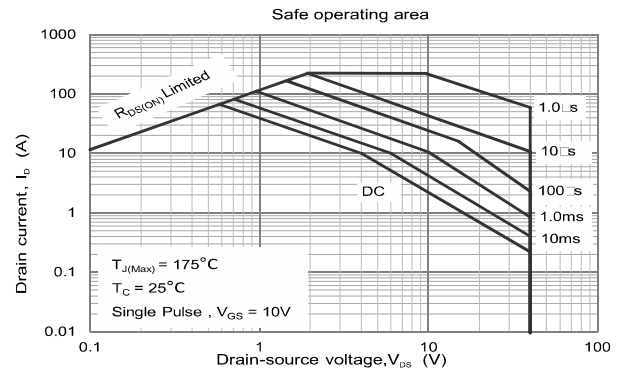
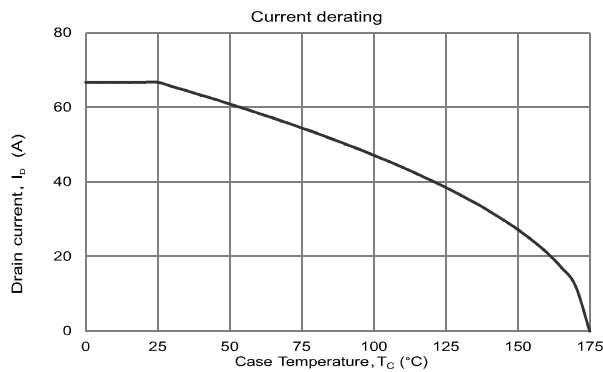
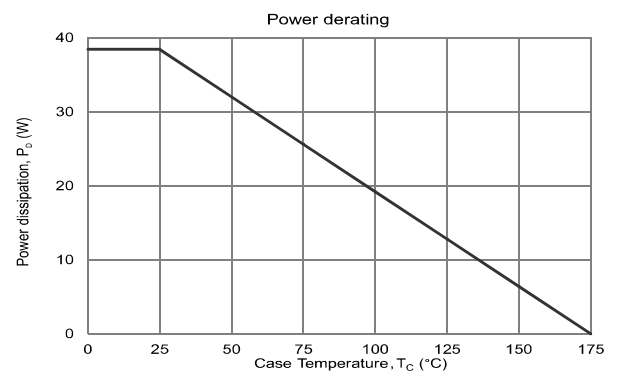
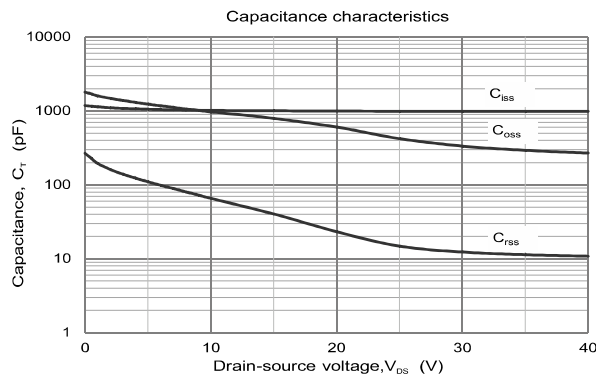
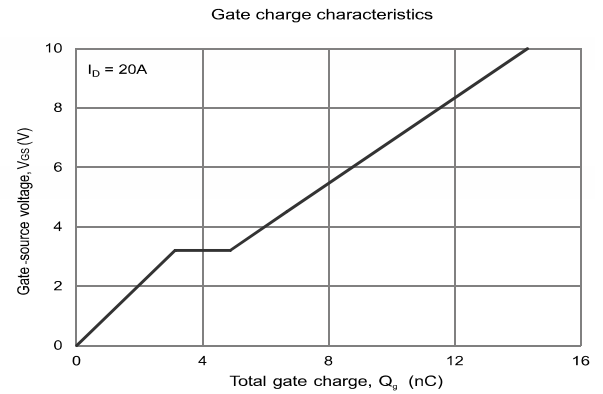
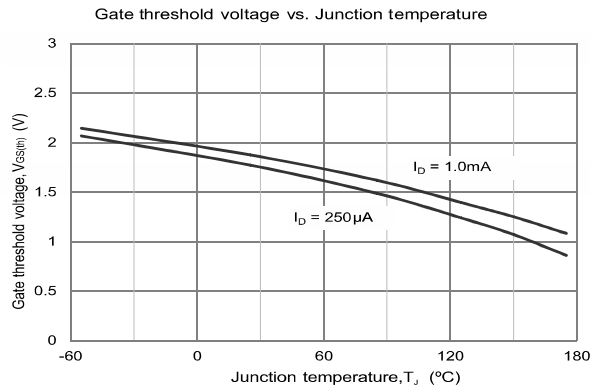
FMOSGTAB67N04-Q1-H

Rating and characteristic curves



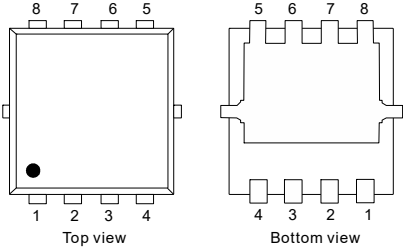
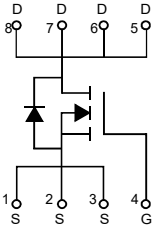
FMOSGTAB67N04-Q1-H

Rating and characteristic curves



FMOSGTAB67N04-Q1-H

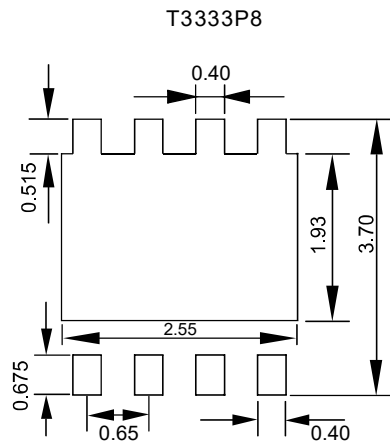
Pinning information

Pin	Simplified outline	Symbol
Pin 1, 2, 3 Source Pin 4 Gate Pin 5, 6, 7, 8 Drain		

Marking

Type number	Marking code
FMOSGTAB67N04-Q1-H	4005CLQ

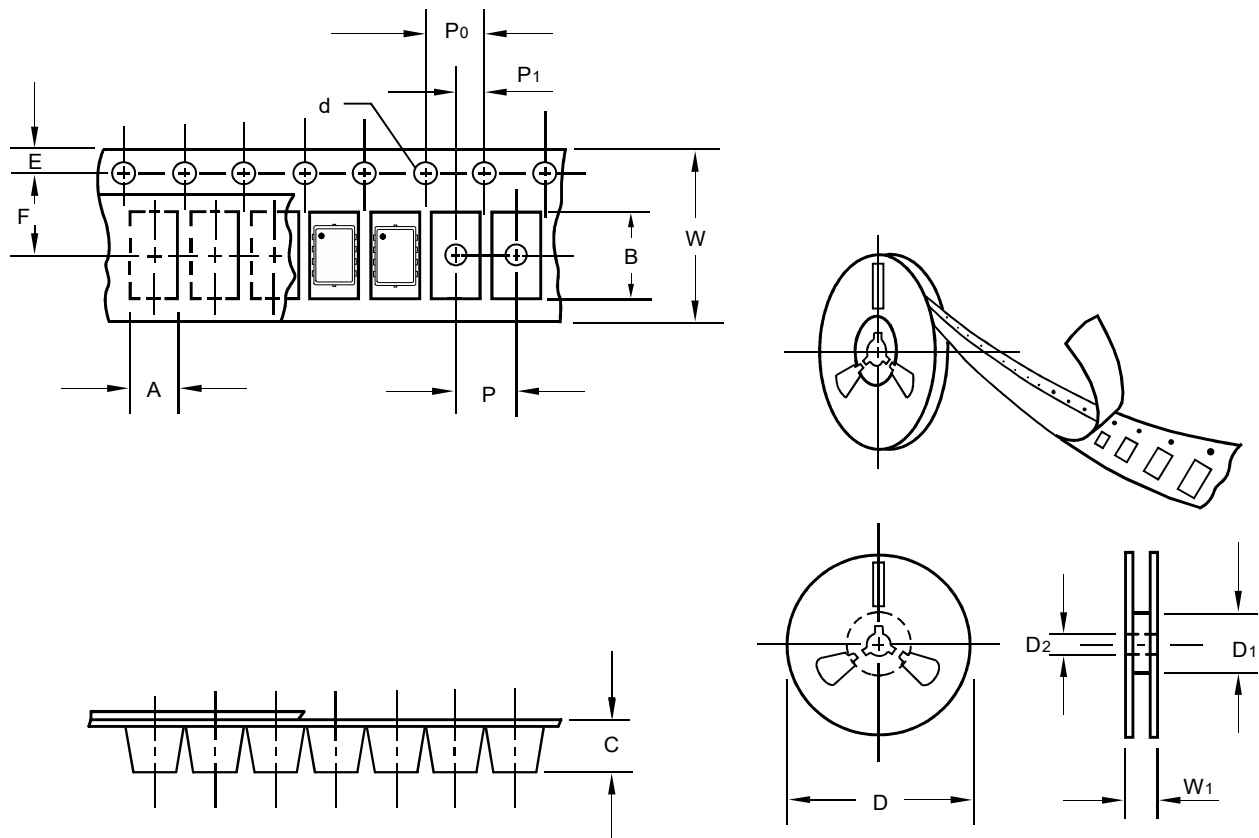
Suggested solder pad layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

FMOSGTAB67N04-Q1-H

Packing information



unit:mm

Item	Symbol	Tolerance	T3333P8
Carrier width	A	0.1	3.55
Carrier length	B	0.1	3.55
Carrier depth	C	0.1	1.10
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D1	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D1	min	-
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Tape width	W	0.3	12.00
Reel width	W1	1.0	17.60

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

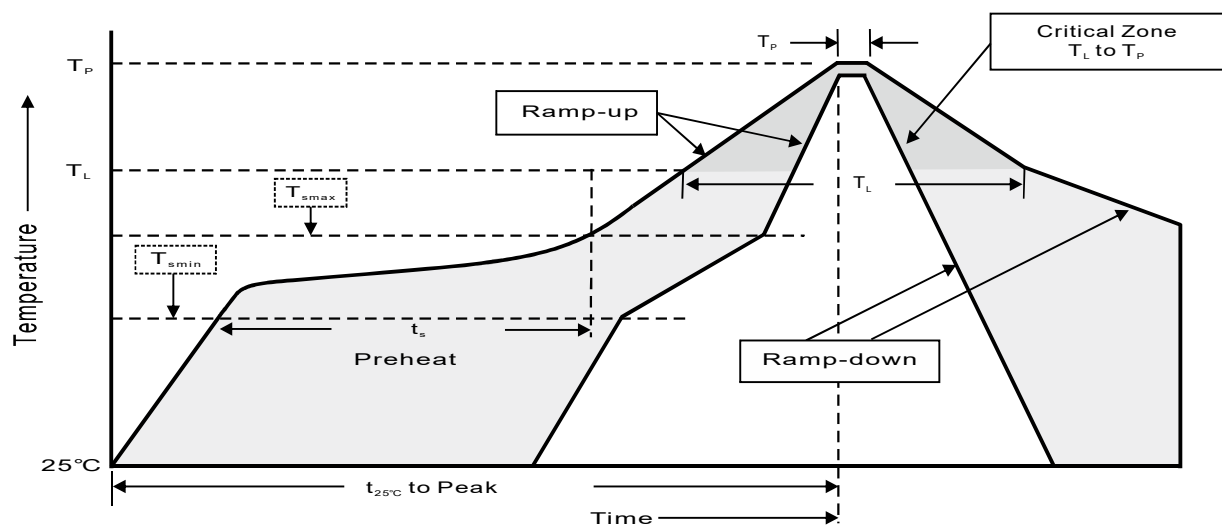
FMOSGTAB67N04-Q1-H

Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
T3333P8	13"	5,000	8.0	10,000	355*335*38	330	350*330*360	80,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_p)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_p)	255 °C -0/+5°C
Time with 5°C of actual peak temperature (T_p)	10 ~30 sec
Ramp-down rate	< 6 °C/sec
Time 25°C to peak temperature	< 6 minutes

FMOSGTAB67N04-Q1-H

High reliability test capabilities

Item Test	Conditions	Reference
1. MSL Preconditioning	24hr bake@125°C+168hrs@85°C /85%RH+3xIR@260°C+1flux immersion+alcohol+DI H2O rinse	JESD22-A113
2. High Temperature Reverse Bias	$V_{DS}=V_{DS} \times 80\%$ ($T_J=T_J \text{ max.}$) Test Duration:1000hrs	JESD22-A108
3. High Temperature Storage Life	$T_a=150^\circ\text{C}$ Test Duration:1000hrs	JESD22 A-103
4. Temperature Cycle	-55°C (15min) to 150°C (15min) Test Cycles:1000cycles	JESD22 A-104
5. Autoclave	$P=2\text{atm}$ $T_a=121^\circ\text{C}$ $\text{RH}=100\%$ Test Duration:96hrs	JESD22 A-102
6. Solderability	$245 \pm 5^\circ\text{C}$ for 5sec	J-STD-002
7. Moisture Resistance	$T_a=85^\circ\text{C}$ / 85% Relative humidity Test Duration:1000hrs	MIL-STD-750E METHOD 1021.2
8. Resistance To Solder Heat	$260 \pm 5^\circ\text{C}$ for 10sec	JESD22 B-106
9. High Temperature High Humidity Reverse Bias	$T_a=85^\circ\text{C}$, 85%RH, $V_{DS}=80\%$ rated V_{DS} Test Duration: 1000hrs	JESD22-A101