

FMOSBSS8402DW-Q1

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FMOSBSS8402DW-Q1

N-Channel And P-Channel Enhancement Mode MOSFET

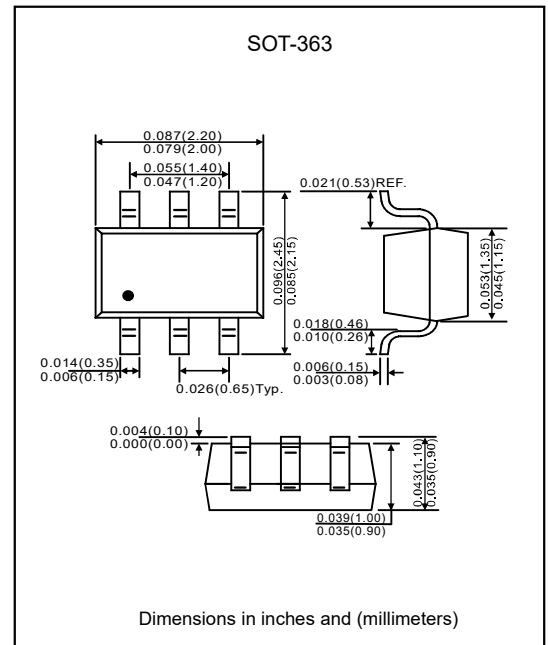
Features

- N-Channel : 60V / 115mA.
 $R_{DS(ON)} \leq 3.0\Omega$, @ $V_{GS}=10V$, $I_D=0.13A$
 $R_{DS(ON)} \leq 3.5\Omega$, @ $V_{GS}=4.5V$, $I_D=0.1A$
- P-Channel : -50V/-130mA.
 $R_{DS(ON)} \leq 10\Omega$, @ $-V_{GS}=5V$, $-I_D=0.1A$.
- Low on-resistance.
- Low gate threshold voltage.
- Fast switching.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen-free part, ex.FMOSBSS8402DW-Q1-H.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, SOT-363.
- Terminals : Solder plated, solder able per MIL-STD-750, Method 2026.
- Mounting Position : Any.

Package outline

Maximum ratings (At $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Ratings		Unit
		N-Channel	P-Channel	
Drain to source voltage	V_{DS}	60	-50	V
Gate-source voltage	V_{GS}	± 20	± 20	V
		± 40	-	
Drain to Gate voltage, ($R_{GS} \leq 1m\Omega$ for N-Ch) ; ($R_{GS} \leq 20K\Omega$ for P-Ch)	V_{DGR}	60	-50	V
Continuous drain current (Note1)	I_D	115	-130	mA
		73	—	
		800	—	
Power dissipation (Note1)	P_D	200		mW
Thermal resistance, junction to ambient	$R_{\theta JA}$	625		$^\circ\text{C/W}$
Junction temperature	T_J	+150		$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 to +150		$^\circ\text{C}$

Note: 1. FR-5 board 1.0x0.75x0.062 inch with minimum recommended pad layout.

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Electrical characteristics (N-Channel) (At $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static parameters (Note2)						
Drain-source breakdown voltage	BV _{DSS}	I _D =10μA, V _{GS} =0V	60	70		V
Drain-source leakage current	I _{DSS}	V _{DS} =60V, V _{GS} =0V, T _C =+25°C			1	μA
		V _{DS} =60V, V _{GS} =0V, T _C =+125°C			500	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
On characteristics (Note2)						
Gate threshold voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
Static drain-source on-state resistance	R _{DS(ON)}	V _{GS} =10V, I _D =0.13A		1.5	3	Ω
		V _{GS} =4.5V, I _D =0.1A		1.8	3.5	
Forward tranconductance	g _{FS}	V _{DS} =10V, I _D =0.2A	80			mS
Dynamic parameters						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		22	50	pF
Out capacitance	C _{oss}			11	25	
Reverse transfer capacitance	C _{rss}			2	5	
Switching parameters						
Turn-on delay time	t _{d(on)}	V _{DS} =30V, I _D =0.2A, R _G =25Ω, R _L =150Ω, V _G =10V		7	20	ns
Turn-off delay time	t _{d(off)}			11	20	ns

Note: 2. Short duration test pulse used to minimize self-heating.

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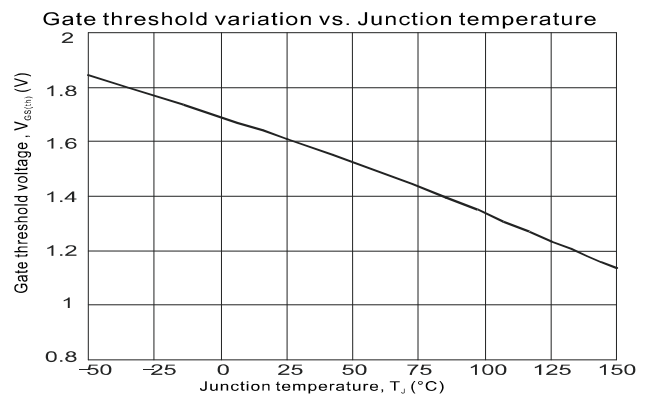
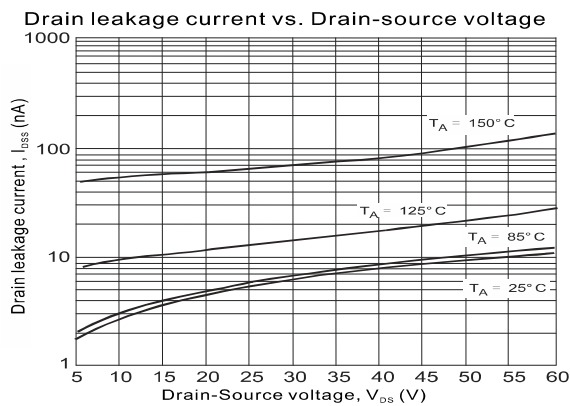
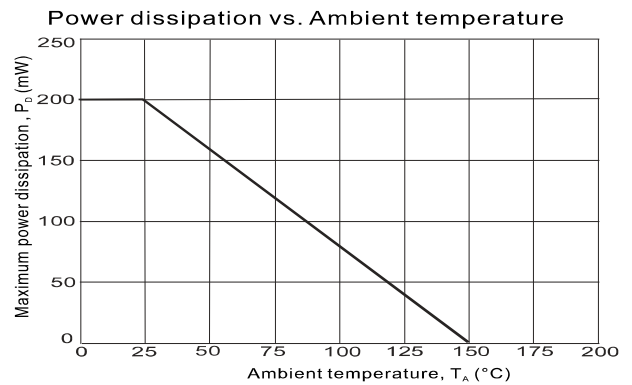
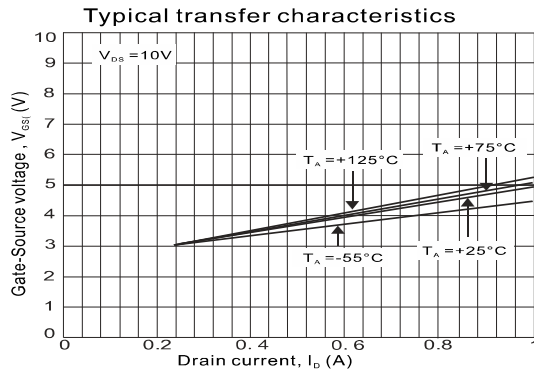
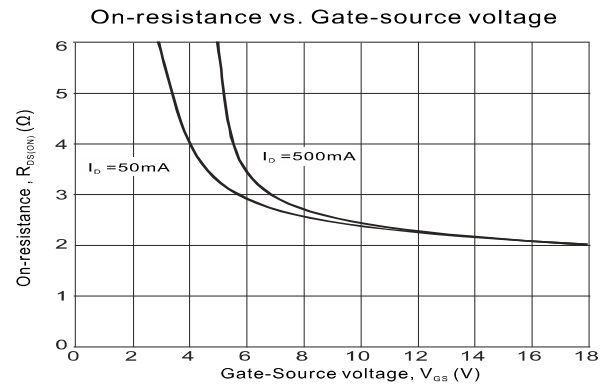
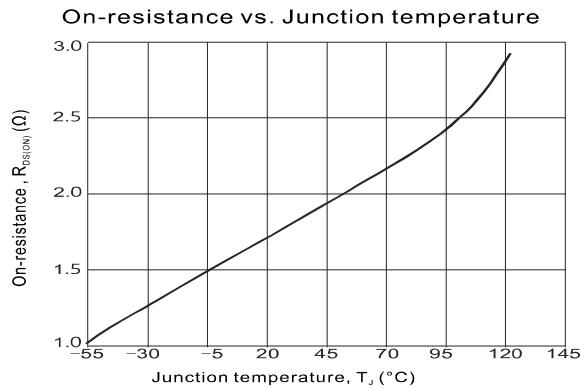
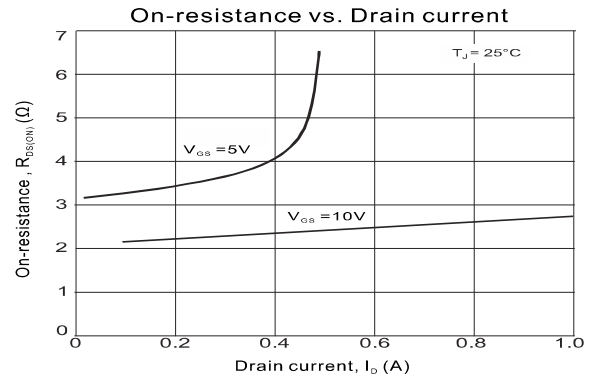
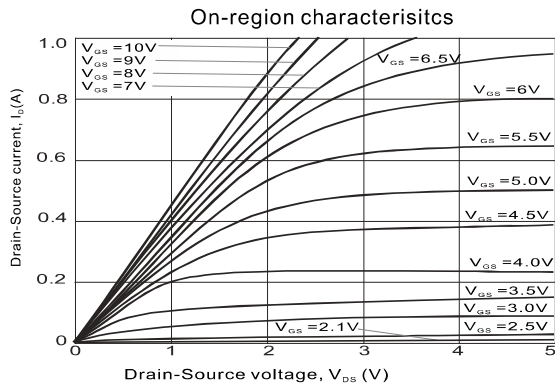
Electrical characteristics (P-Channel) (At $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static parameters (Note2)						
Drain-source breakdown voltage	$-BV_{DSS}$	$-I_D=250\mu A, V_{GS}=0V$	50			V
Drain-source leakage current	$-I_{DSS}$	$-V_{DS}=50V, V_{GS}=0V, T_J=+25^{\circ}C$			1	μA
		$-V_{DS}=50V, V_{GS}=0V, T_J=+125^{\circ}C$			2	
		$-V_{DS}=25V, V_{GS}=0V, T_J=+25^{\circ}C$			100	nA
Gate-source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
On characteristics (Note2)						
Gate threshold voltage	$-V_{GS(TH)}$	$V_{DS}=V_{GS}, -I_D=1mA$	0.8		2	V
Static drain-source on-state resistance	$R_{DS(ON)}$	$-V_{GS}=5V, -I_D=0.1A$			10	Ω
Forward tranconductance	g_{FS}	$-V_{DS}=25V, -I_D=0.1A$	0.05			S
Dynamic parameters						
Input capacitance	C_{iss}	$V_{GS}=0V, -V_{DS}=25V, f=1.0MHz$			45	pF
Out capacitance	C_{oss}				25	
Reverse transfer capacitance	C_{rss}				12	
Switching parameters						
Turn-on delay time	$t_{d(on)}$	$-V_{DS}=30V, -I_D=0.27A, R_G=50\Omega, V_G=-10V$		10		ns
Turn-off delay time	$t_{d(off)}$			18		ns

Note: 2. Short duration test pulse used to minimize self-heating.

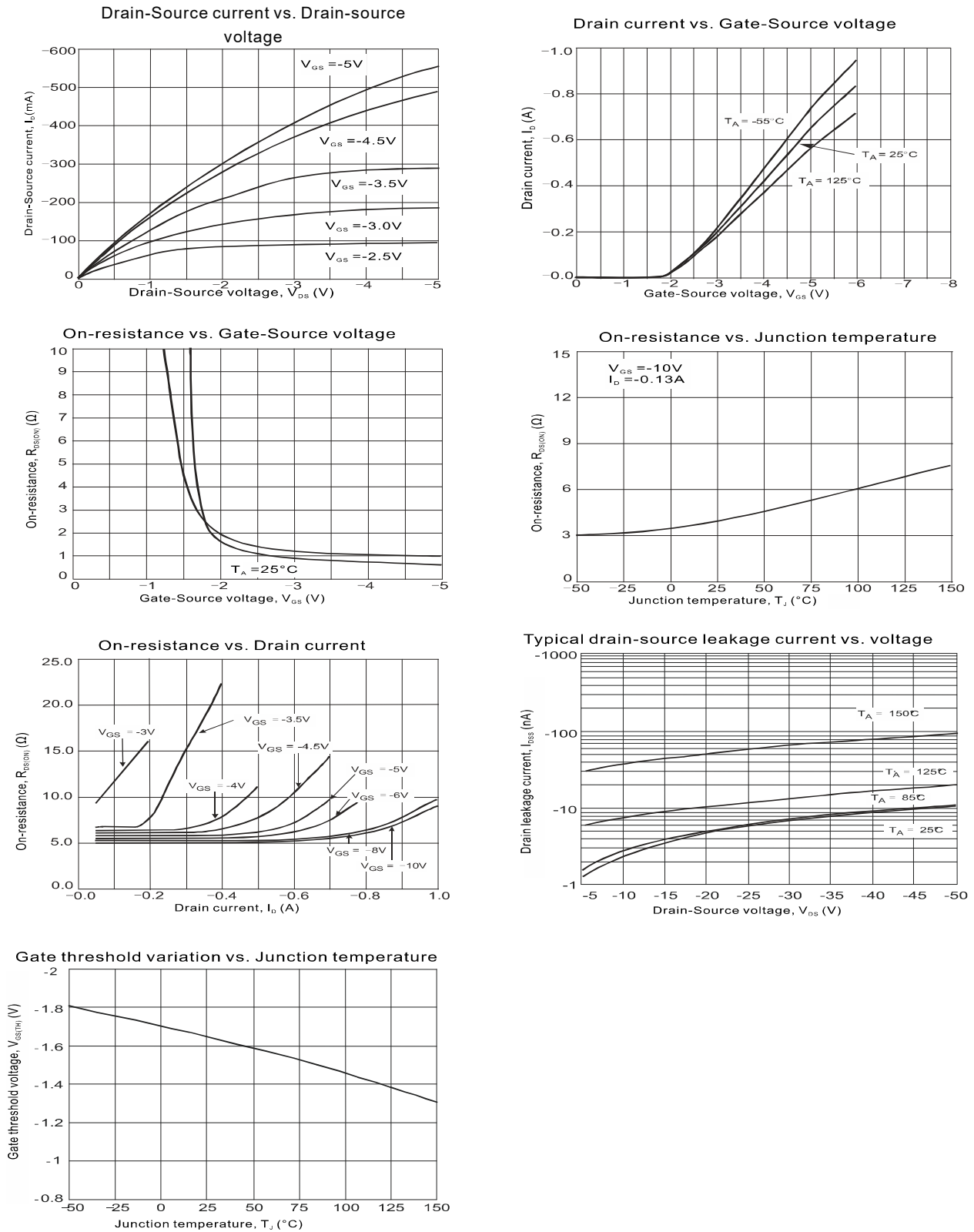
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Rating and characteristic curves (N-Channel)



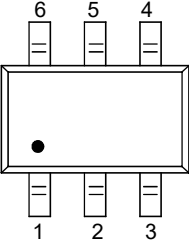
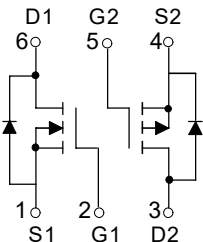
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Rating and characteristic curves (P-Channel)



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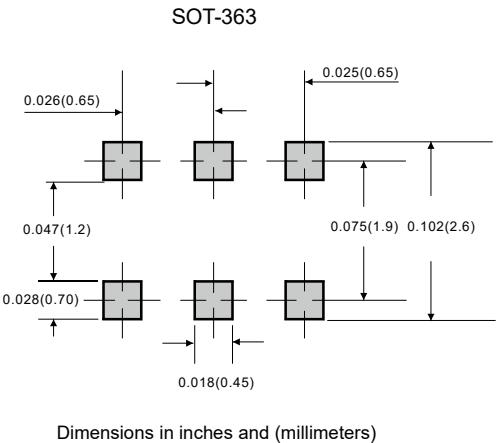
Pinning information

Pin	Simplified outline	Symbol
Pin1 Source1 Pin2 Gate1 Pin3 Drain2 Pin4 Source2 Pin5 Gate2 Pin6 Drain1		

Marking

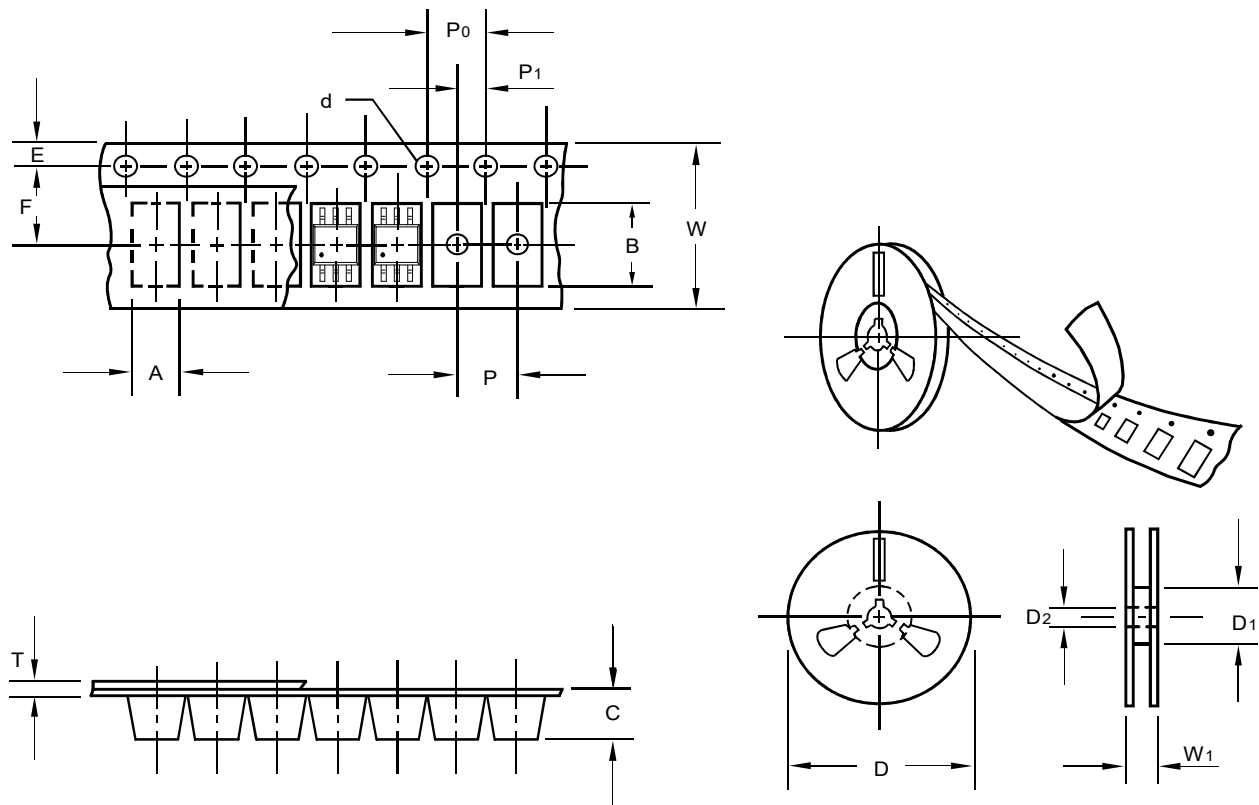
Type number	Marking code
FMOSBSS8402DW-Q1	S82

Suggested solder pad layout



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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-363
Carrier width	A	0.2	2.25
Carrier length	B	0.2	2.55
Carrier depth	C	0.1	1.20
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	62.00
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W1	1.0	11.40

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

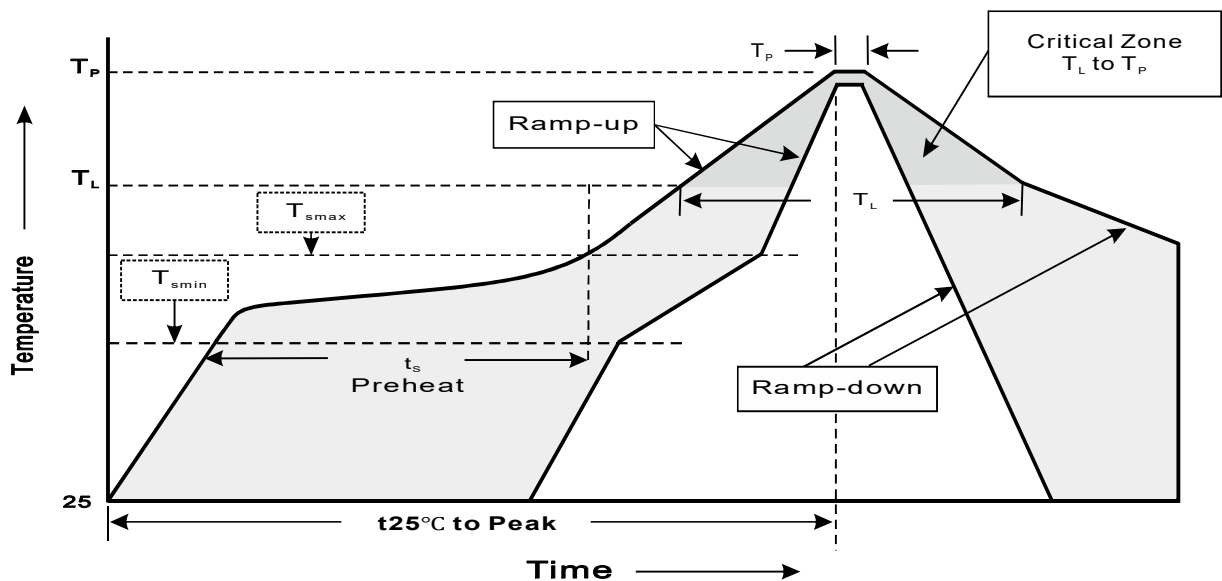
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
SOT-363	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000

Suggested thermal profiles for soldering processes

- 1.Storage environment : Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering Condition
Average ramp-up rate (T_L to T_P)	< 3°C/sec
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (min to max) (t_s)	150°C 200°C 60 ~ 120sec
T_{smax} to T_L -Ramp-up rate	< 3°C/sec
Time maintained above: -Temperature (T_L) -Time(T_L)	217°C 60 ~ 260 sec
Peak Temperature(T_P)	255°C -0/+5°C
Time within 5°C of actual peak Temperature(T_P)	10 ~ 30sec
Ramp-down rate	< 6°C/sec
Time 25°C to peak temperature	< 6 minutes