FMOSB245N10-H

List

List.....1

Package outline.....2

Features.....2

Applications.....2

Mechanical data.....2

Absolute maximum ratings 2

Electrical characteristics.....3

Typical electrical & thermal characteristics.....4~5

Pinning information.....6

Marking.....6

Suggested solder pad layout.....6

Packing information.....7

Reel Information.....8

Suggested thermal profiles for soldering processes.....8

FMOSB245N10-H

245A 100V N-Channel
Enhancement Mode Power MOSFET

Features

- V_{DS}=100(V), I_D=245A.
- $R_{DS(ON)}$ < 3.2mΩ, @V_{GS}=10V, I_D=20A.
- High speed power switching.
- Reliable and Rugged.
- 100% UIS and Rg Tested.
- Lead-free parts meet RoHS requirements.

Applications

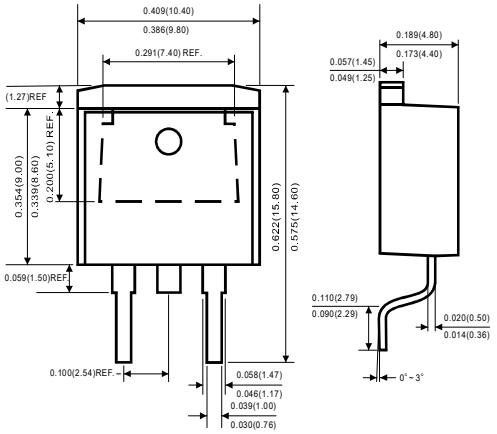
- Synchronous Rectification in SMPS.
- Hard Switching and High Speed Circuit.

Mechanical data

- Case : TO-263, Plastic.
- Terminals : Solder able per MIL-STD-202, Method208.
- Polarity : indicated by cathode band.
- Approx weight : 1.531 grams.

Package outline

D2PAK (TO-263)



Dimensions in inches and (millimeters)

Absolute maximum ratings (At T_C=25°C unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	±20	V
Continuous drain Current (Note 1)	I_D	245	A
Pulsed drain Current	I_{DM}	400	A
Avalanche current, Single pulse (L=0.5mH) (Note 2)	I_{AS}	42	A
Single pulsed avalanche energy (L=0.5mH) (Note 2)	E_{AS}	441	mJ
Power dissipation (Note 4)	P_D	284	W
Operating Junction temperature range	T_J	+175	℃
Storage temperature range	T_{STG}	-55 to +175	℃
Thermal resistance junction to ambient (Note 3)	$R_{\theta JA}$	60	℃/W
Thermal resistance junction to case (Note 3)	$R_{\theta JC}$	0.44	℃/W

FMOSB245N10-H

Electrical characteristics (At T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Drain-source leakage current	I_{DSS}	V_{DS}=80V, V_{GS}=0V			1	μA
Gate-source leakage current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
On characteristics						
Gate threshold voltage	$V_{GS(TH)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	3.0	4.0	V
Static drain-source on-resistance (Note 4)	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		2.7	3.2	mΩ
Forward transconductance	g_{FS}	V_{DS}=5V, I_D=10A		39		S
Dynamic parameters (Note 5)						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=50V, $F_{req.}$=1.0MHz		7424		pF
Out capacitance	C_{oss}			1983		
Reverse transfer capacitance	C_{rss}			59		
Gate resistance	R_G	V_{GS}=0V, V_{DS}=0V, Freq.=1MHz		0.2		Ω
Switching parameters						
Total gate charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=20A		123.6		nC
Gate to source charge	Q_{gs}			34.7		
Gate to drain charge	Q_{gd}			27.6		
Turn-on delay time	$t_{d(on)}$	V_{DD}=25V, V_{GS}=10V, R_{GEN}=1Ω, I_D=1.0A		22.5		ns
Rise time	t_r			6.5		
Turn-off delay time	$t_{d(off)}$			61.5		
Fall time	t_f			119.2		
Source-drain diode ratings and characteristics (Note 4)						
Maximum continuous drain to source forward current	I_S				200	A
Reverse recovery charge	Q_{rr}	I_F=10A, V_R=50V, dI_F/dt=100A/μs		186.5		nC
Reverse recovery time	t_{rr}			84.9		ns
Drain-source diode forward voltage (Note 4)	V_{SD}	I_{SD}=10A, V_{GS}=0V		0.75	1.1	V

Note :
1. Max. Current is limited by junction temperature
2. UIS tested and pulse width are limited by maximum junction temperature 150°C.
3. Surface Mounted on 1in2 FR-4 board with 1oz.
4. Pulse test (pulse width≤300us, duty cycle ≤ 2%).
5. Guaranteed by design, not subject to production testing.

FMOSB245N10-H

Typical electrical & thermal characteristics

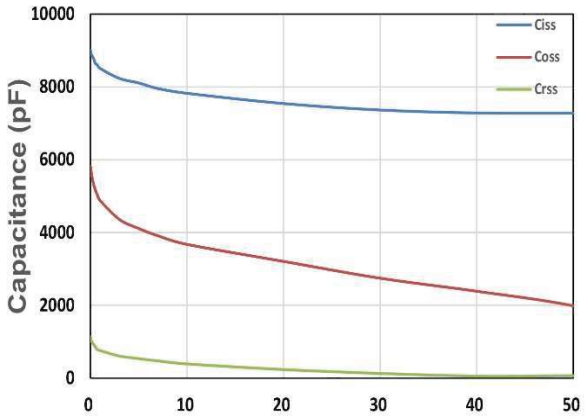


Figure 7. Capacitance

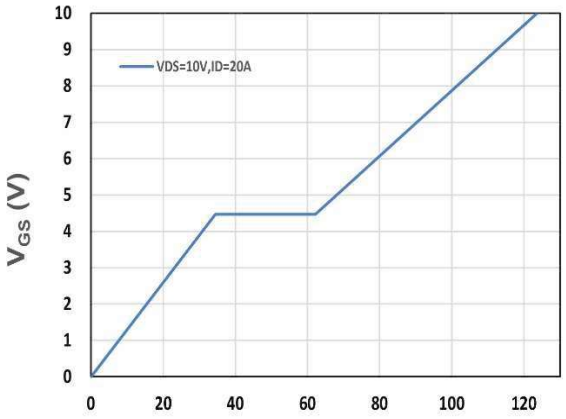


Figure 8. Gate Charge Characteristics

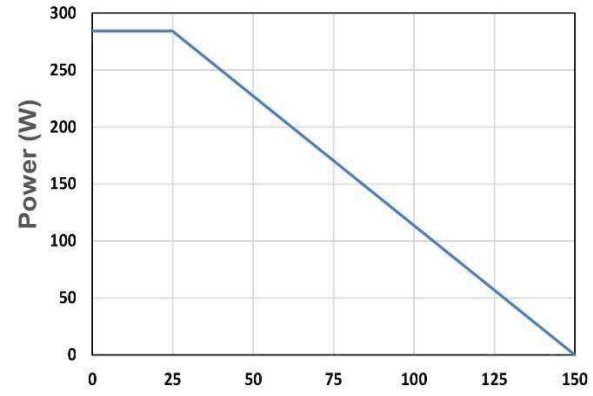


Figure 9. Power Dissipation

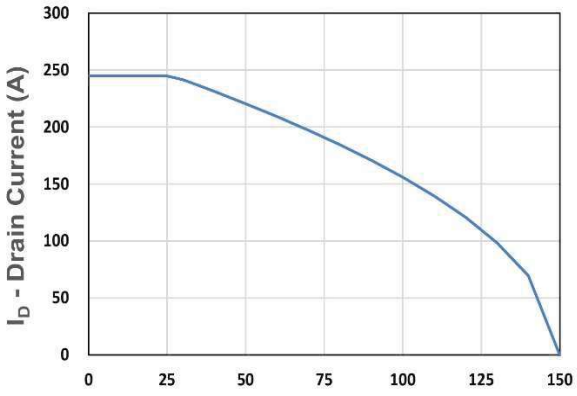


Figure 10. Drain Current

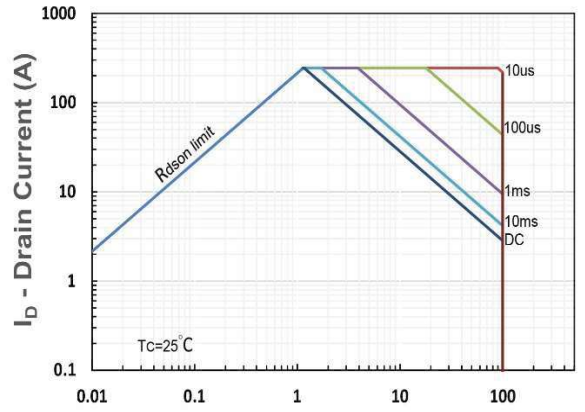


Figure 11. Safe Operating Area

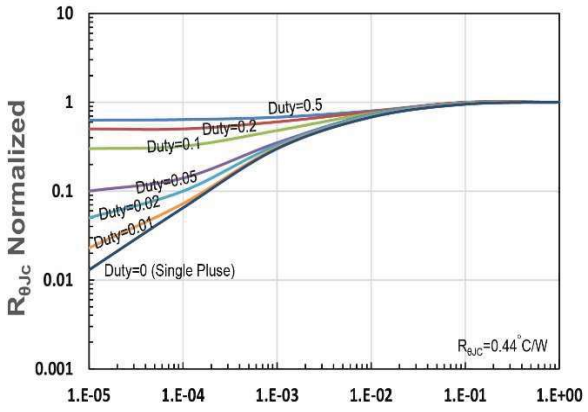


Figure 12. RθJc Transient Thermal Impedance

FMOSB245N10-H

Typical electrical & thermal characteristics

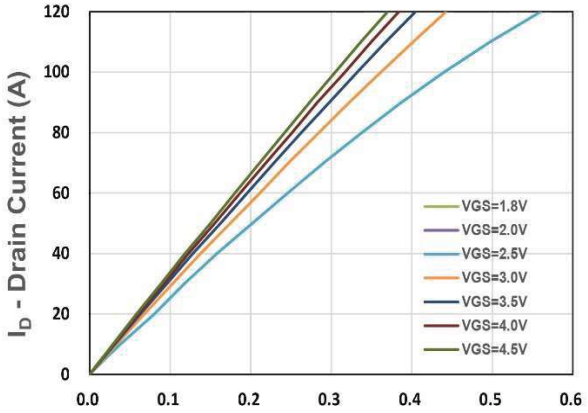


Figure 1. Output Characteristics

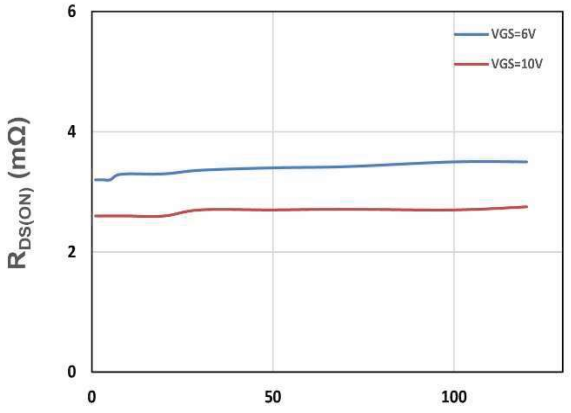


Figure 2. On-Resistance vs. ID

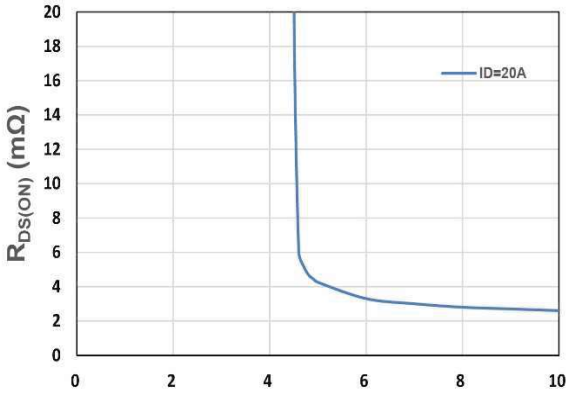


Figure 3. On-Resistance vs. VGS

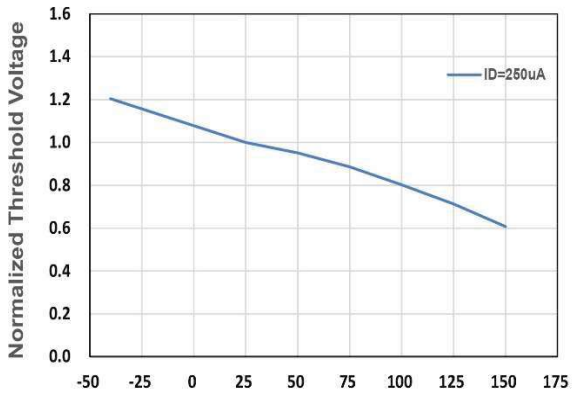


Figure 4. Gate Threshold Voltage

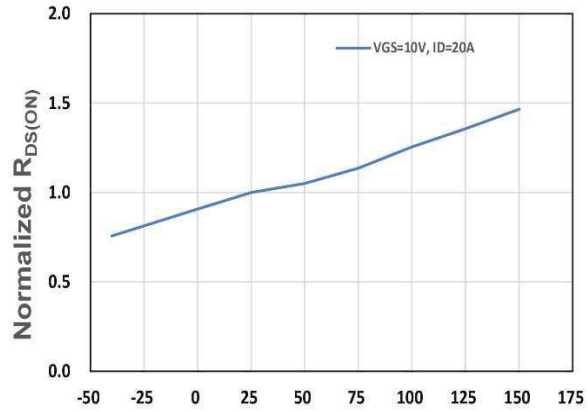


Figure 5. Drain-Source On Resistance

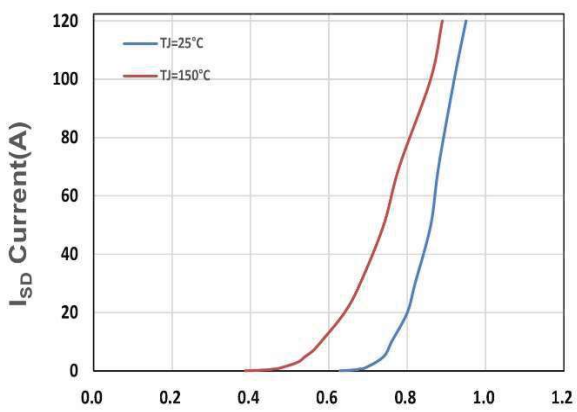
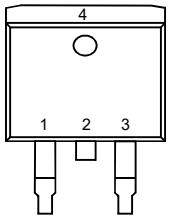
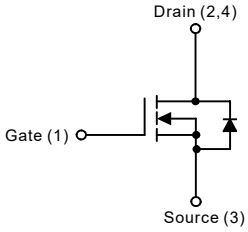


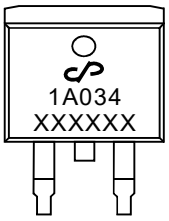
Figure 6. Source-Drain Diode Forward

FMOSB245N10-H

Pinning information

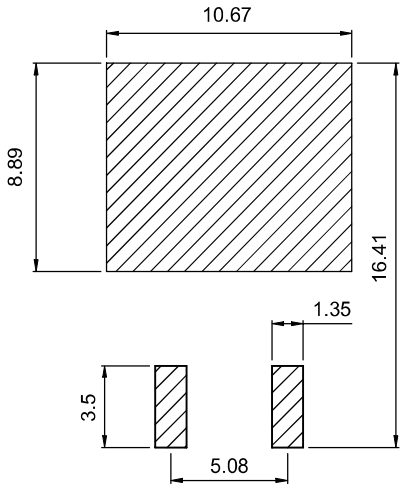
Pin	Simplified outline	Symbol
Pin 1 Gate Pin 2, 4 Drain Pin 3 Source		

Marking



Date Code : XXXXXX

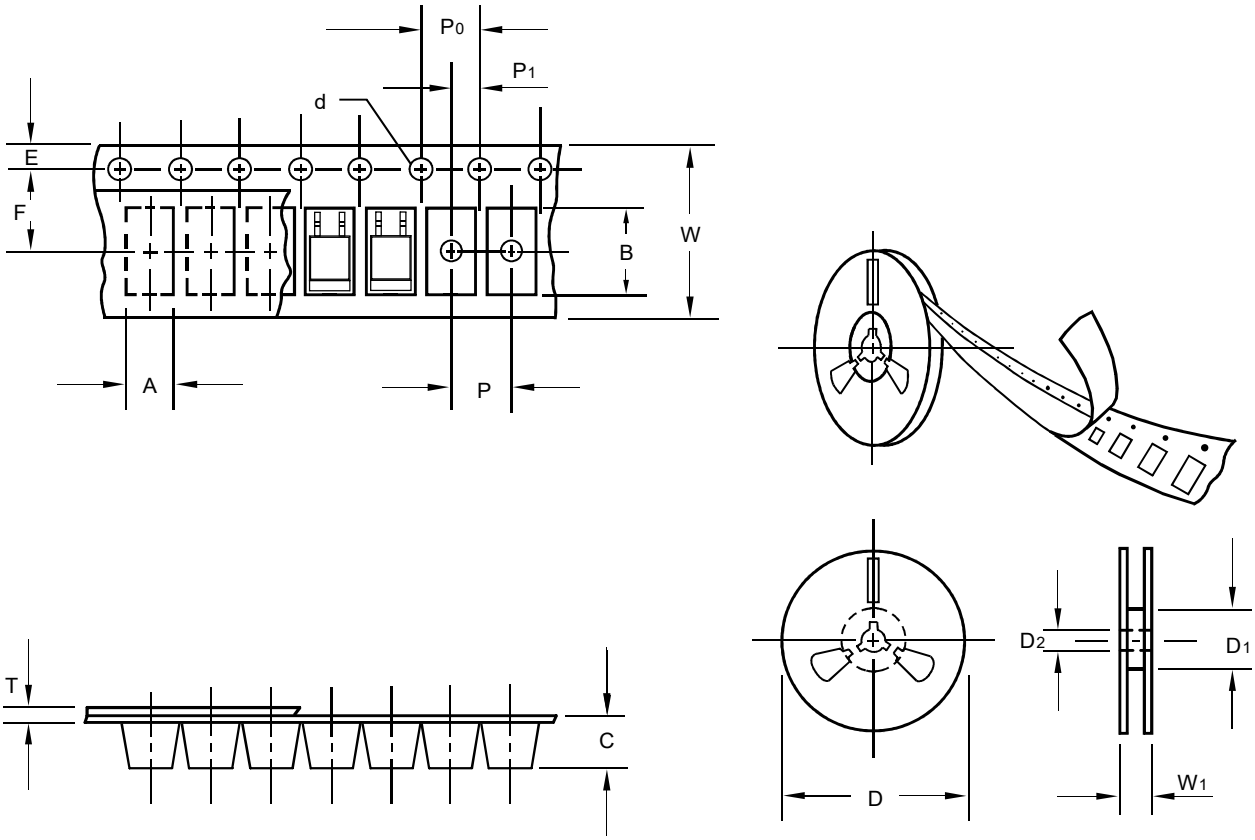
Suggested solder pad layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.1 mm.
3.The pad layout is for reference purposes only.

FMOSB245N10-H

Packing information



unit:mm

Item	Symbol	Tolerance	D2PAK
Carrier width	A	0.1	10.70
Carrier length	B	0.1	16.30
Carrier depth	C	0.1	5.10
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D_1	min	50.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D_1	min	-
Feed hole diameter	D_2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	11.50
Punch hole pitch	P	0.1	16.00
Sprocket hole pitch	P_0	0.1	4.00
Embossment center	P_1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	24.00
Reel width	W_1	1.0	30.00

Note:Devices are packed in accor dance with EIA standar RS-481-A and specifications listed above.

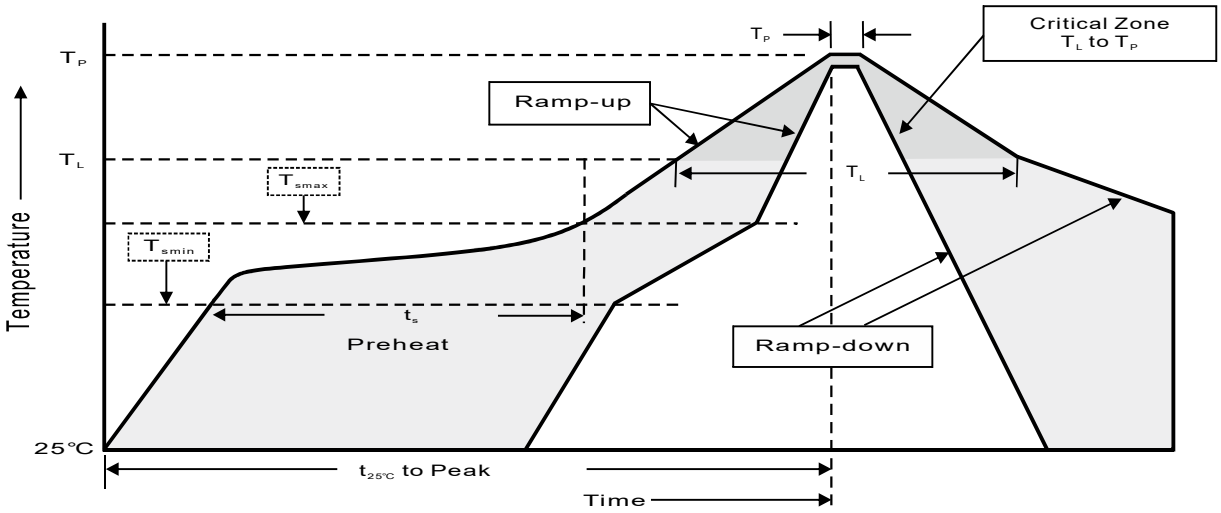
FMOSB245N10-H

Packing information

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
D2PAK/TO-263	13"	800	16.0	800	335*335*38	330	350*330*360	6,400	15.0

Suggested thermal profiles for soldering processes

1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%
2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_P)	< 3 ℃/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	 150℃ 200℃ 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	 < 3 ℃/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	 217℃ 60 ~ 260 sec
Peak temperature (T_P)	255 ℃ -0/+5℃
Time with 5℃ of actual peak temperature (T_P)	10 ~30 sec
Ramp-down rate	< 6 ℃/sec
Time 25℃ to peak temperature	< 6 minutes