

FMOSAC70N03A

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FMOSAC70N03A

70A 30V N-Channel Enhancement Mode Power MOSFET

Features

- $V_{DS} = 30V$, $I_D = 70A$.
- $R_{DS(ON)} \leq 4\text{ m}\Omega$, @ $V_{GS} = 10V$, $I_D = 20A$.
- $R_{DS(ON)} \leq 6\text{ m}\Omega$, @ $V_{GS} = 4.5V$, $I_D = 10V$.
- 100% UIS and R_g tested.
- Reliable and rugged.
- Low gate charge and gate-drain charge for high-speed switching.
- Low on-resistance to minimize conduction losses.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates halogen free part, ex: FMOSAC70N03A-H.

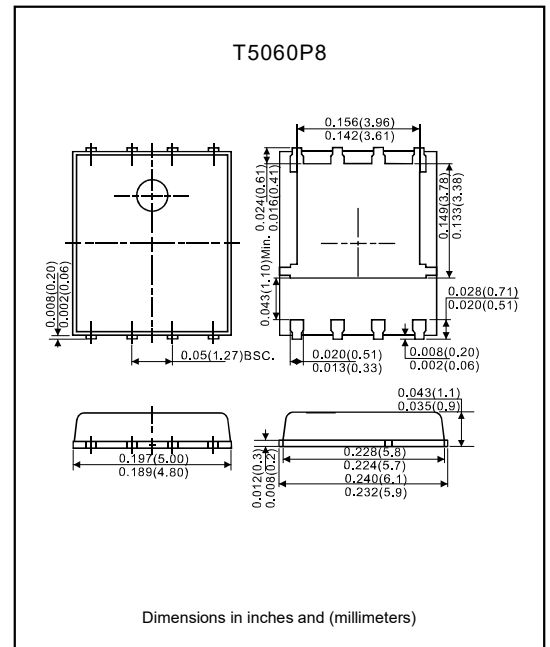
Application

- Power management in DC/DC converters.
- Power load switch.
- Notebook battery management.

Mechanical data

- Epoxy: UL94-V0 rated flame retardant.
- Case : Molded plastic, T5060P8 (DFN5060-8) .
- Mounting Position : Any.

Package outline



Maximum ratings (At $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain Current (Note 2)	I_D	($T_c = 25^\circ\text{C}$) 70	A
		($T_c = 100^\circ\text{C}$) 50	
Pulsed drain current tested (Note 1)	I_{DM}	($T_c = 25^\circ\text{C}$) 70	A
Avalanche current, single pulse (Note 3)	I_{AS}	($L = 0.1\text{mH}$) 31	A
Avalanche energy, single pulse (Note 3)	E_{AS}	($L = 0.1\text{mH}$) 48	mJ
Power dissipation (Note 2)	P_D	($T_c = 25^\circ\text{C}$) 46	W
		($T_c = 100^\circ\text{C}$) 18	
Thermal resistance junction to ambient (Note 3) (Steady state)	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal resistance Junction to case (Steady state)	$R_{\theta JC}$	2.7	$^\circ\text{C/W}$
Operating Junction temperature	T_J	+150	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^\circ\text{C}$

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Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	BV_{DSS}	30			V
Drain-source leakage current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$	I_{DSS}			1	μA
Gate-source leakage current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	I_{GSS}			± 100	nA

On characteristics

Gate threshold voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	$V_{GS(TH)}$	1	1.5	2	V
Static drain-source on-resistance (Note 4)	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	$R_{DS(ON)}$		3.4	4	m Ω
	$V_{GS}=4.5\text{V}$, $I_D=10\text{A}$			4.5	6	
Forward trans conductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$	g_{FS}		25.2		S

Dynamic parameters (Note 5)

Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1.0\text{MHz}$	R_G		1		Ω
Input capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1.0\text{MHz}$	C_{iss}		2435		pF
Out capacitance		C_{oss}		308		
Reverse transfer capacitance		C_{rss}		259		

Switching parameters

Total gate charge	$V_{GS}=4.5\text{V}$, $V_{DS}=15\text{V}$, $I_D=20\text{A}$	Q_g		33		nC
				62		
Gate to source charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=20\text{A}$	Q_{gs}		10.19		
Gate to drain charge		Q_{gd}		16.01		
Turn-on delay time	$V_{DS}=15\text{V}$, $V_{GS}=10\text{V}$, $R_G=3\Omega$, $I_D=1\text{A}$	$t_{d(on)}$		10.3		ns
Rise time		t_r		17.6		
Turn-off delay time		$t_{d(off)}$		43.2		
Fall time		t_f		31.7		

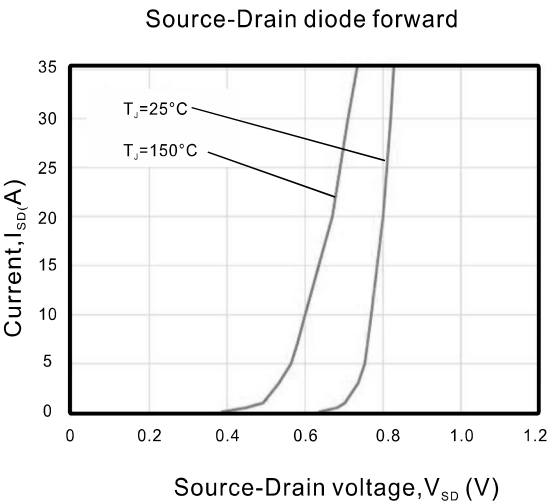
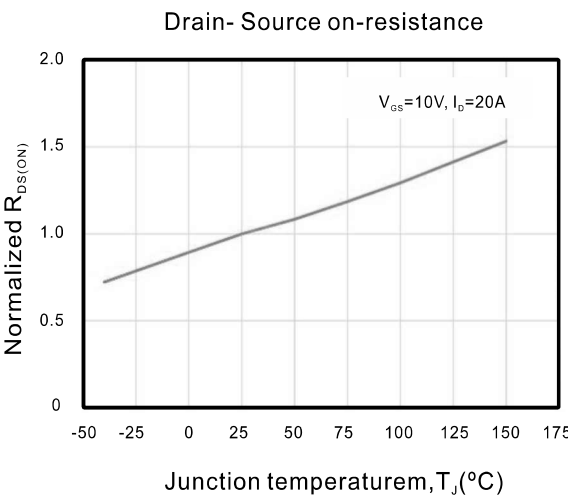
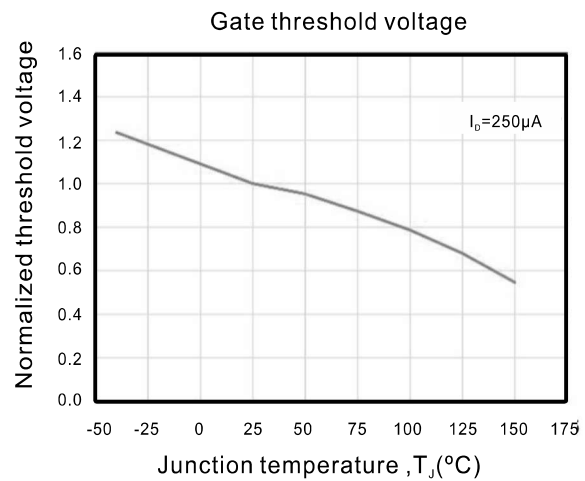
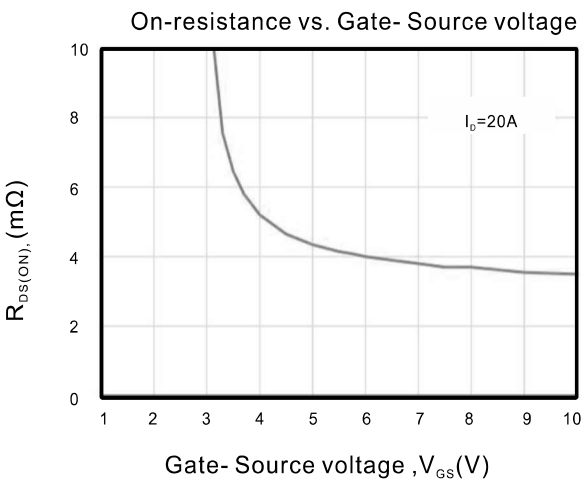
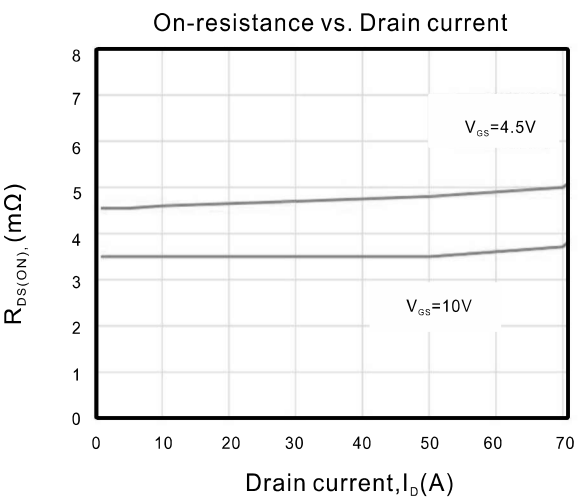
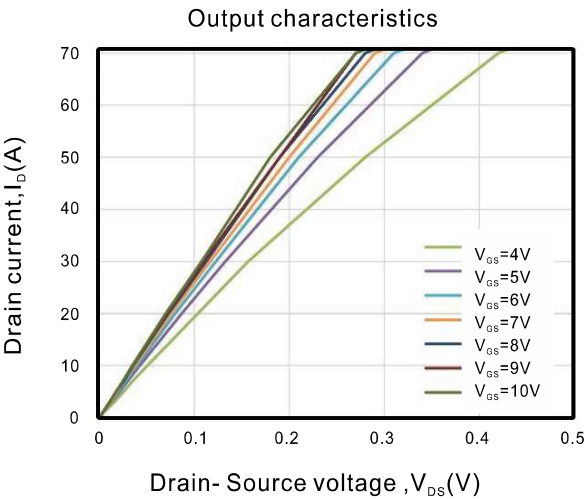
Source-drain diode ratings and characteristics

Drain-source diode forward voltage (Note 4)	$I_S=1\text{A}$, $V_{GS}=0\text{V}$	V_{SD}		0.7	1.1	V
Body diode reverse recovery time	$V_{GS}=0\text{V}$, $I_F=1\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$	t_{rr}		20		ns
Body diode reverse recovery charge		Q_{rr}		12		nC

- Note : 1. Max.current is limited by bonding wire.
 2. UIS tested and pulse width are limited by maximum junction temperature 150°C .
 3. Surface mounted on 1in² FR-4 board with 1oz.
 4. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
 5. Guaranteed by design, not subject to production testing.

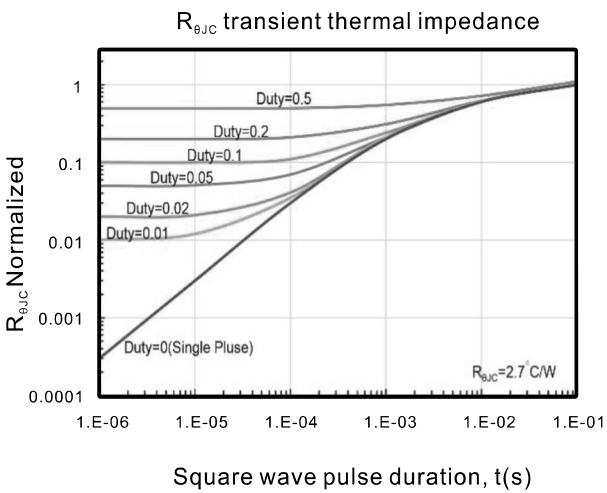
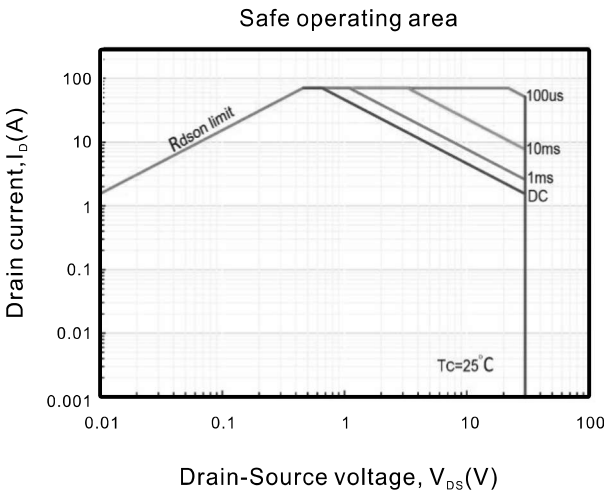
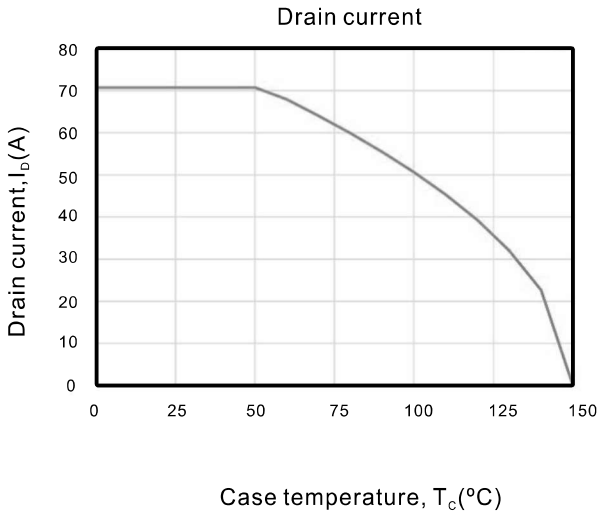
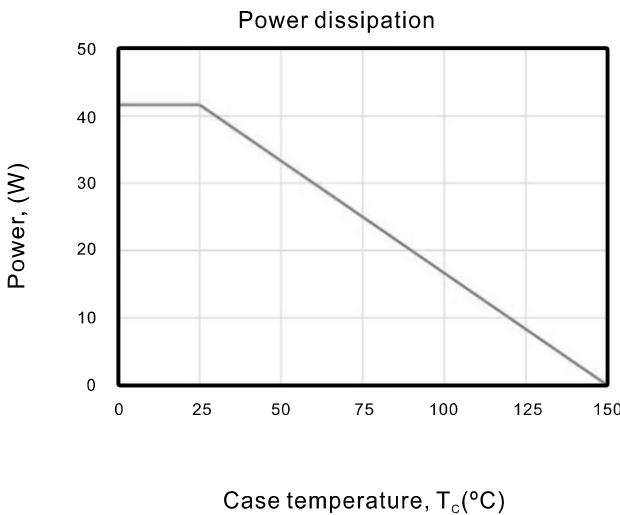
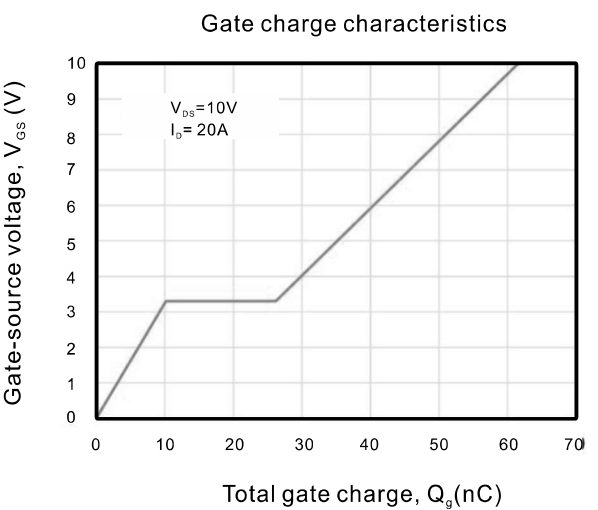
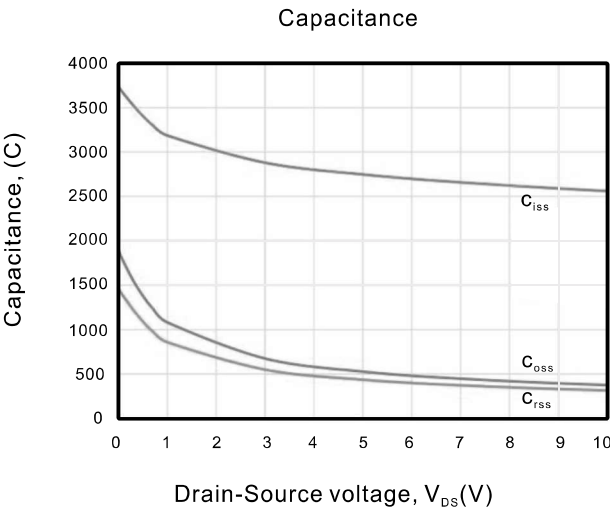
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Rating and characteristic curves



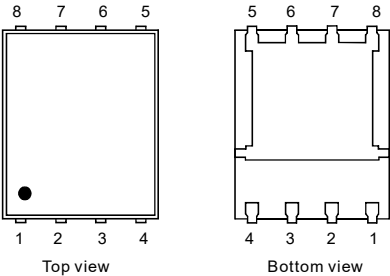
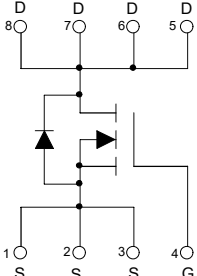
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Rating and characteristic curves

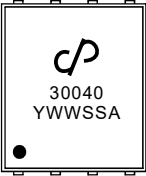


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Pinning information

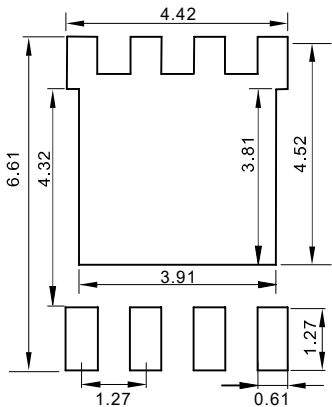
Pin	Simplified outline	Symbol
Pin1 Source Pin2 Source Pin3 Source Pin4 Gate Pin5 Drain Pin6 Drain Pin7 Drain Pin8 Drain	 Top view Bottom view	

Marking

Type number	Marking code
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* YWW: Wafer lot code
Y: Year
W: Week
SS: Sequence
A: Assy. code

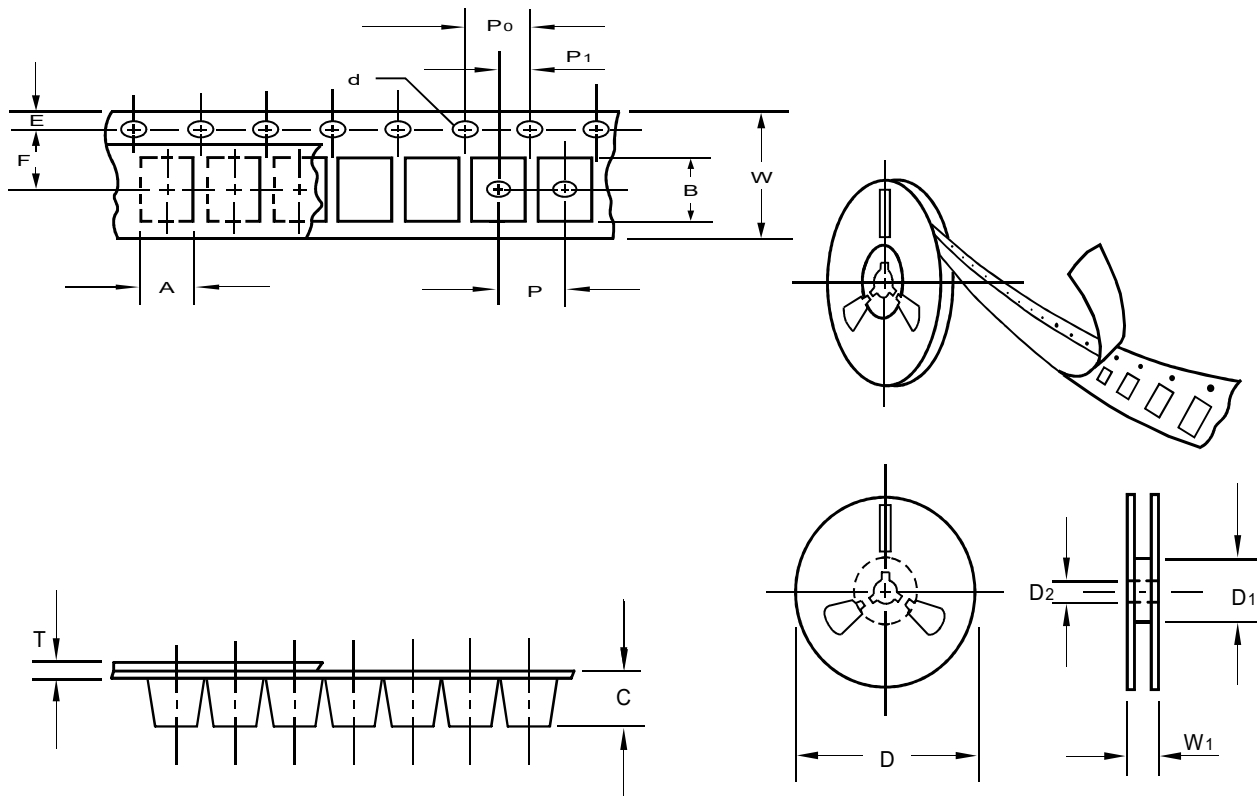
Suggested solder pad layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only.

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Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8
Carrier width	A	0.1	6.40
Carrier length	B	0.1	5.40
Carrier depth	C	0.1	1.25
Sprocket hole	d	0.1	1.55
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D1	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D1	min	-
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.30
Tape width	W	0.3	12.00
Reel width	W1	1.0	17.60

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

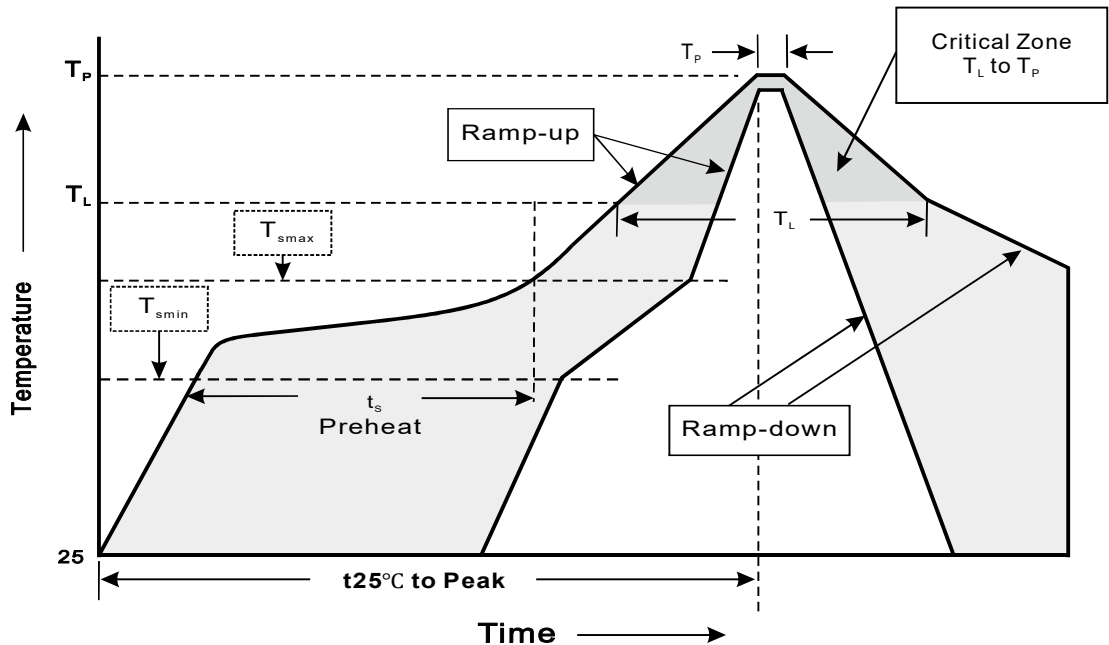
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Reel packing

Device	Outline	Device Package	Reel Size	Reel (pcs)
FMOSAC70N03A	Taping	T5060P8	13 inch	5,000

Suggested thermal profiles for soldering processes

- 1.Storage environment : Temperature=5°C~40°C Humidity=55%±25%
2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering Condition
Average ramp-up rate (T_L to T_p)	< 3°C/sec
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (min to max) (t_s)	150°C 200°C 60 ~ 120sec
T_{smax} to T_L -Ramp-up rate	< 3°C/sec
Time maintained above: -Temperature (T_L) -Time(T_L)	217°C 60 ~ 260 sec
Peak Temperature(T_p)	255°C -0/+5°C
Time within 5°C of actual peak Temperature(T_p)	10 ~ 30sec
Ramp-down rate	< 6°C/sec
Time 25°C to peak temperature	< 6 minutes