

FMOSAC52N06-Q1

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FMOSAC52N06-Q1

52A 60V N-Channel Enhancement
Mode Power MOSFET

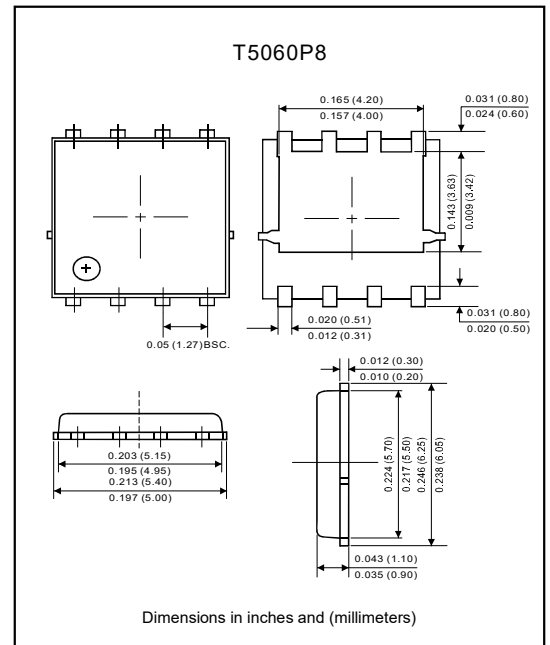
Features

- $V_{DS}=60V$, $I_D=52A$.
- $R_{DS(ON)} \leq 12m\Omega$ @ $V_{GS}=10V$, $I_D=20A$.
- $R_{DS(ON)} \leq 16m\Omega$ @ $V_{GS}=4.5V$, $I_D=15A$.
- Low on-resistance and low gate charge.
- 100% UIS and R_g tested.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen-free part, ex.FMOSAC52N06-Q1-H.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, T5060P8.
- Mounting Position : Any.

Package outline

Maximum ratings (At $T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain Current (Note 1)	I_D	52	A
		37	
Pulsed drain current (Note 2)	I_{DM}	207	A
Single pulse avalanche current (Note 3)	I_{AS}	20	A
Single pulse avalanche energy (Note 3)	E_{AS}	20	mJ
Power dissipation (Note 4)	P_D	53	W
		31	
Thermal resistance Junction to ambient	$R_{\theta JA}$	72	$^\circ C/W$
Thermal resistance Junction to case	$R_{\theta JC}$	2.8	$^\circ C/W$
Operating Junction temperature	T_J	+175	$^\circ C$
Storage temperature range	T_{STG}	-55 to +175	$^\circ C$

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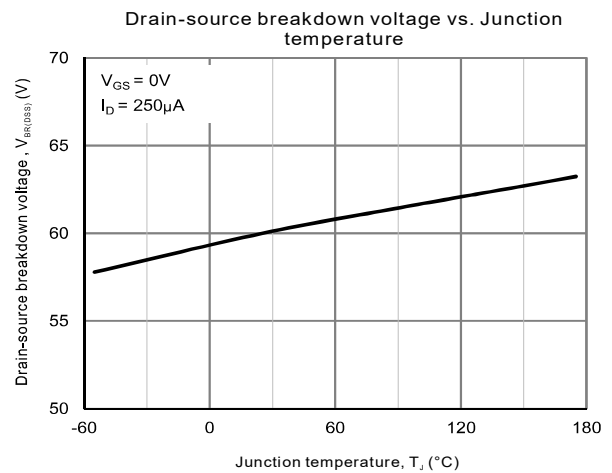
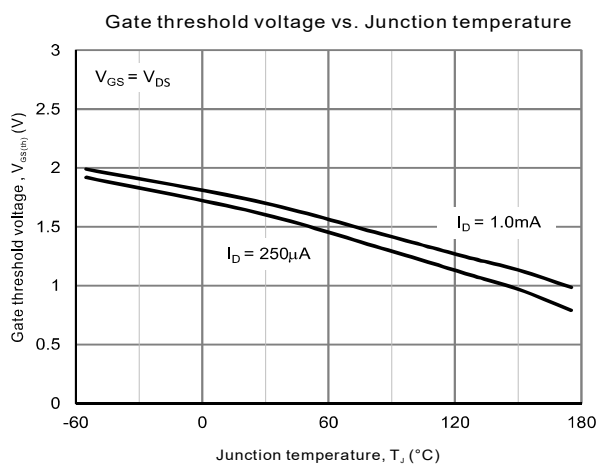
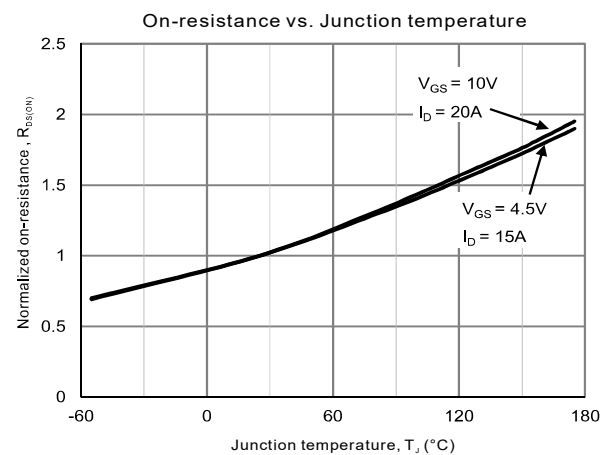
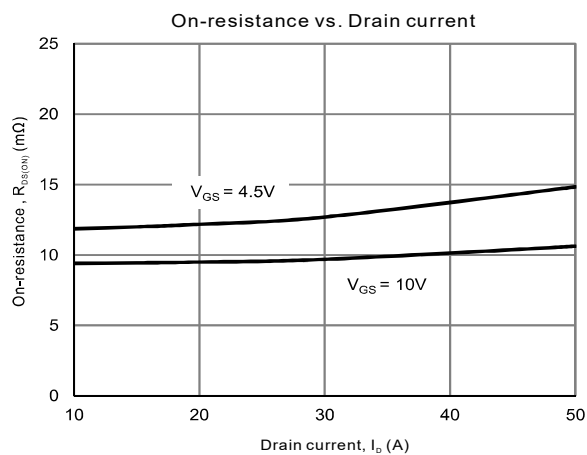
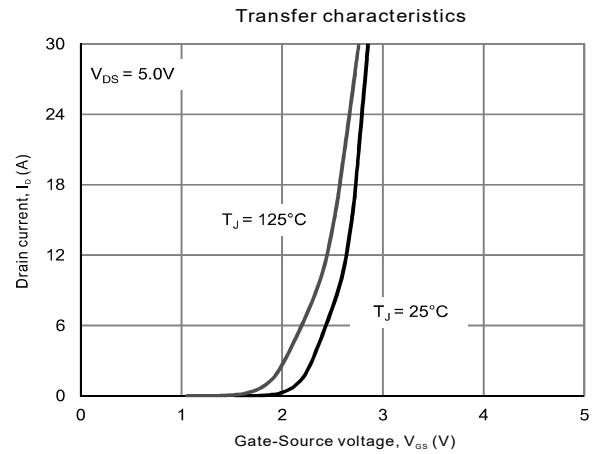
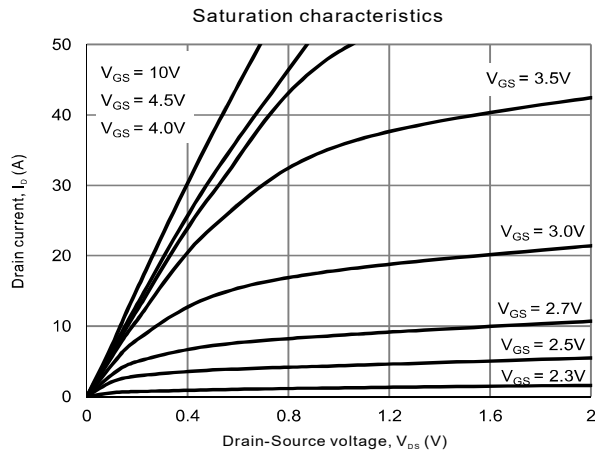
Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	60			V
Drain-source leakage current	I _{DSS}	V _{DS} =48V, V _{GS} =0V			1	μA
		V _{DS} =48V, V _{GS} =0V, T _J =55°C			5	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
On characteristics						
Gate threshold voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D =250μA	1.2	1.6	2.5	V
Static drain-source on-resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		9.5	12	mΩ
		V _{GS} =4.5V, I _D =15A		12	16	
Forward transconductance	g _{FS}	V _{DS} =5V, I _D =20A		81		S
Dynamic parameters						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =30V, f=1.0MHz		731		pF
Out capacitance	C _{oss}			224		
Reverse transfer capacitance	C _{rss}			7.4		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		1.7		Ω
Switching parameters						
Total gate charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =20A		13.9		nC
		V _{GS} =4.5V, V _{DS} =30V, I _D =20A		7		
Gate to source charge	Q _{gs}	V _{GS} =0 to 10V, V _{DS} =30V, I _D =20A		1.6		
Gate to drain charge	Q _{gd}	V _{GS} =0 to 10V, V _{DS} =30V, I _D =20A		3.1		
Turn-on delay time	t _{d(on)}	V _{DS} =30V, V _{GS} =10V, R _L =1.5Ω, R _G =6Ω		3.7		ns
Rise time	t _r			4.3		
Turn-off delay time	t _{d(off)}			16.2		
Fall time	t _f			6.5		
Source-drain diode ratings and characteristics						
Drain-source diode forward voltage	V _{SD}	I _S =1A, V _{GS} =0V		0.65	1	V
Diode continuous current	I _S	T _C =25°C			52	A
Body diode reverse recovery time	t _{rr}	I _F =15A, dI _F /dt=100A/μs		24		ns
Body diode reverse recovery charge	Q _{rr}				9.3	

- Notes : 1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under $T_{J_Max}=175^{\circ}\text{C}$.
3. This single-pulse measurement was taken under the following condition [$L=100\mu\text{H}$, $V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$] while its value is limited by $T_{J_Max}=175^{\circ}\text{C}$.
4. The power dissipation P_D is based on $T_{J_Max}=175^{\circ}\text{C}$.
5. This value is guaranteed by design hence it is not included in the production test.

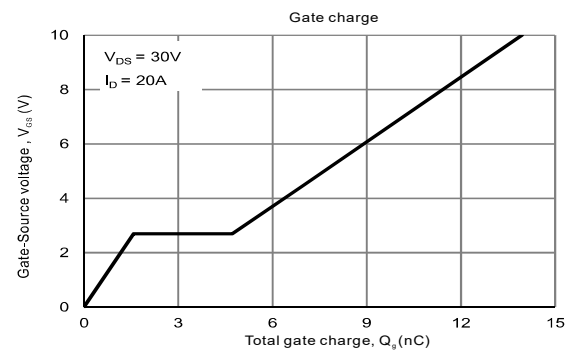
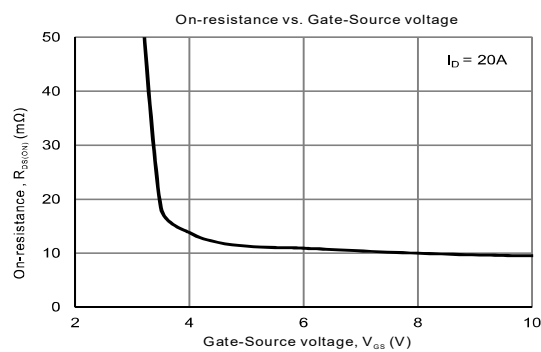
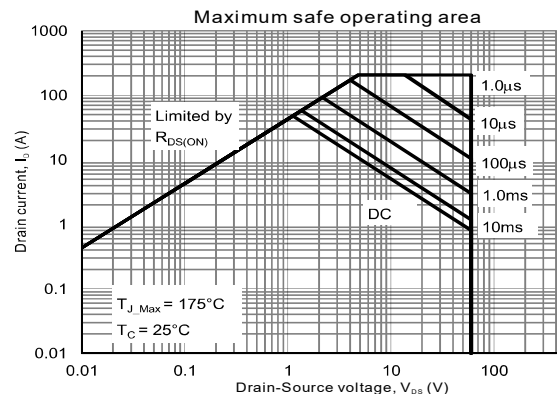
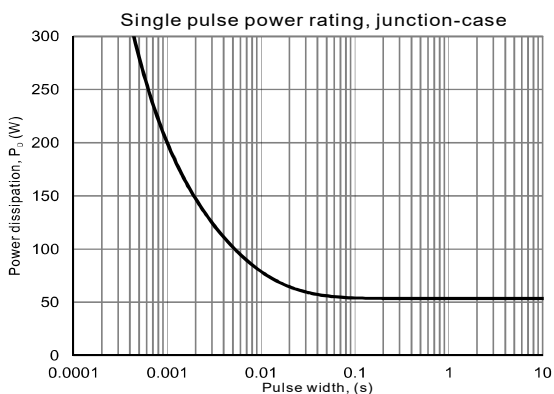
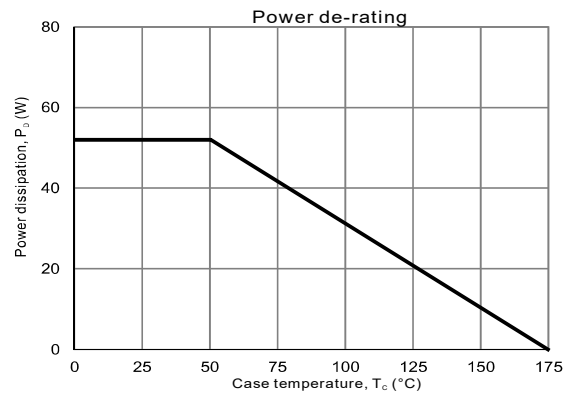
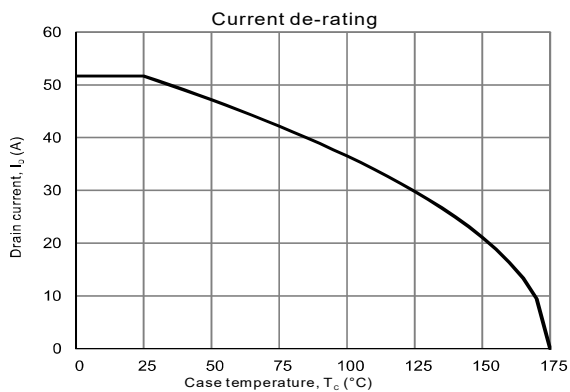
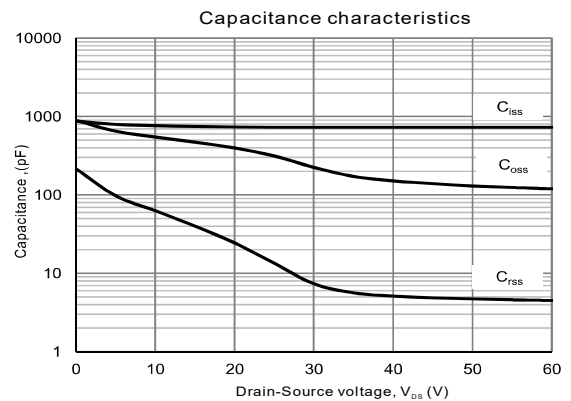
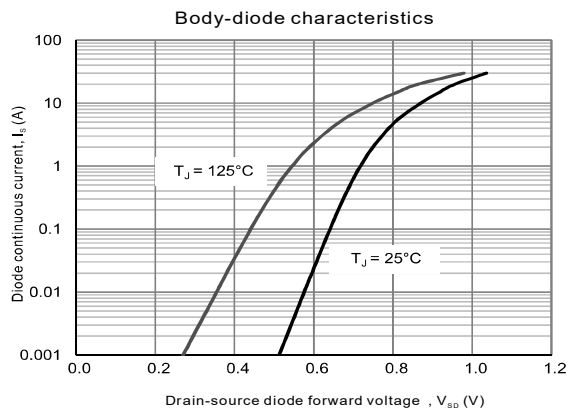
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Rating and characteristic curves



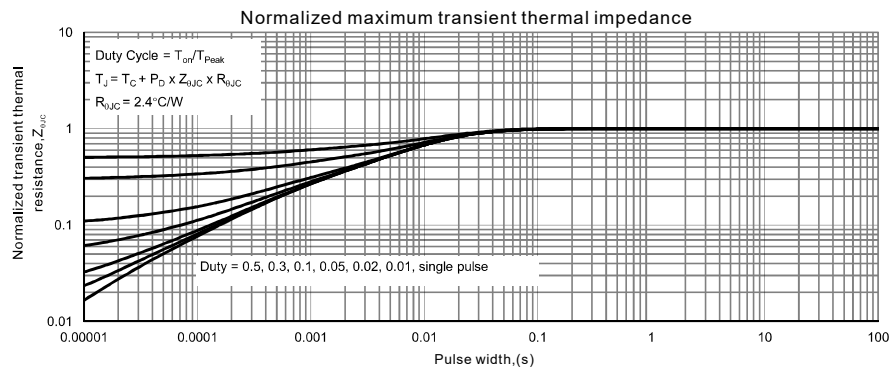
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Rating and characteristic curves



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Rating and characteristic curves



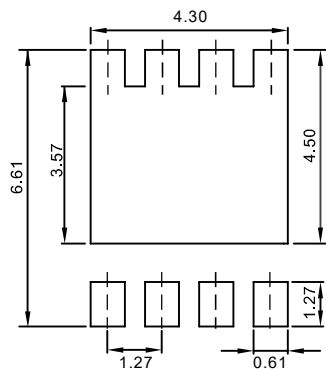
Pinning information

Pin	Simplified outline	Symbol
Pin 1, 2, 3 Source Pin 4 Gate Pin 5, 6, 7, 8 Drain		

Marking

Type number	Marking code
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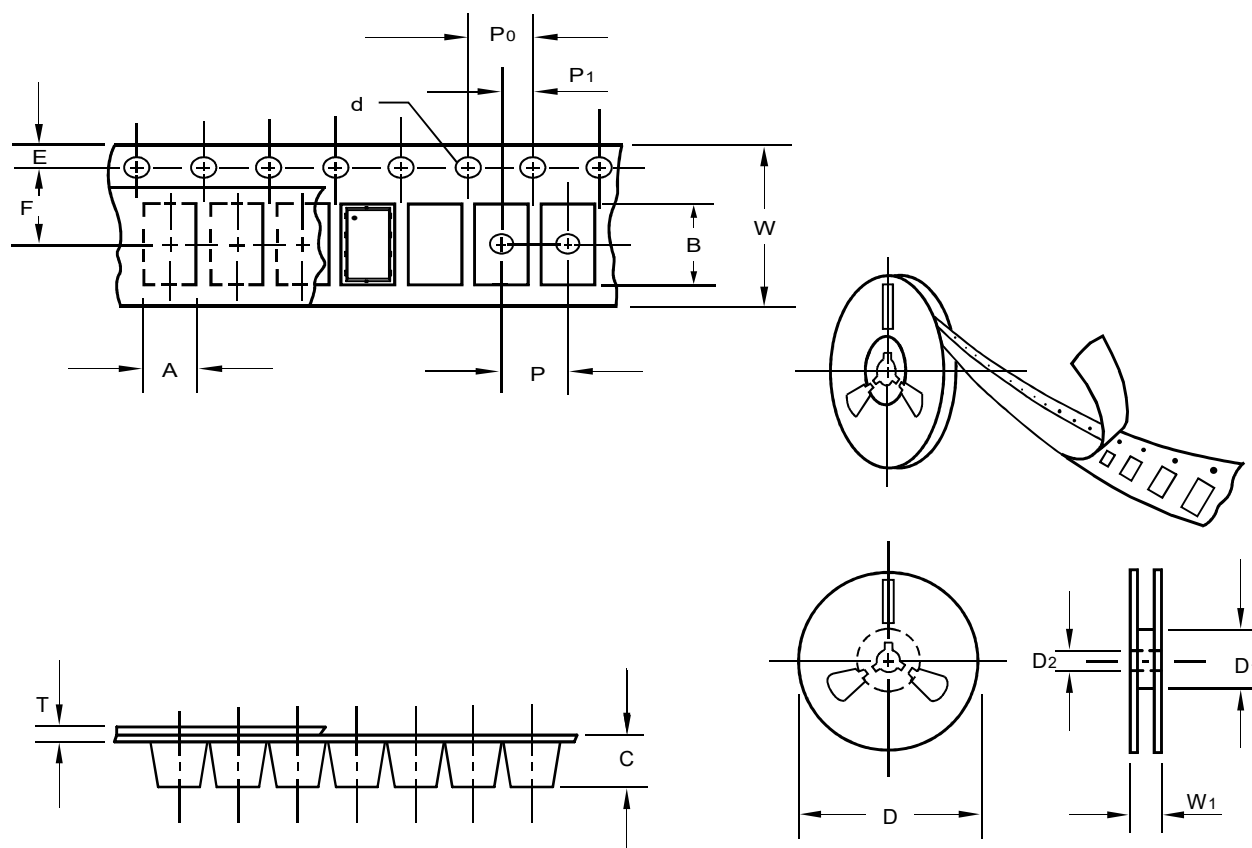
Suggested solder pad layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only.

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Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8
Carrier width	A	0.1	6.40
Carrier length	B	0.1	5.40
Carrier depth	C	0.1	1.25
Sprocket hole	d	0.1	1.55
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D1	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D1	min	-
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.30
Tape width	W	0.3	12.00
Reel width	W1	1.0	17.60

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

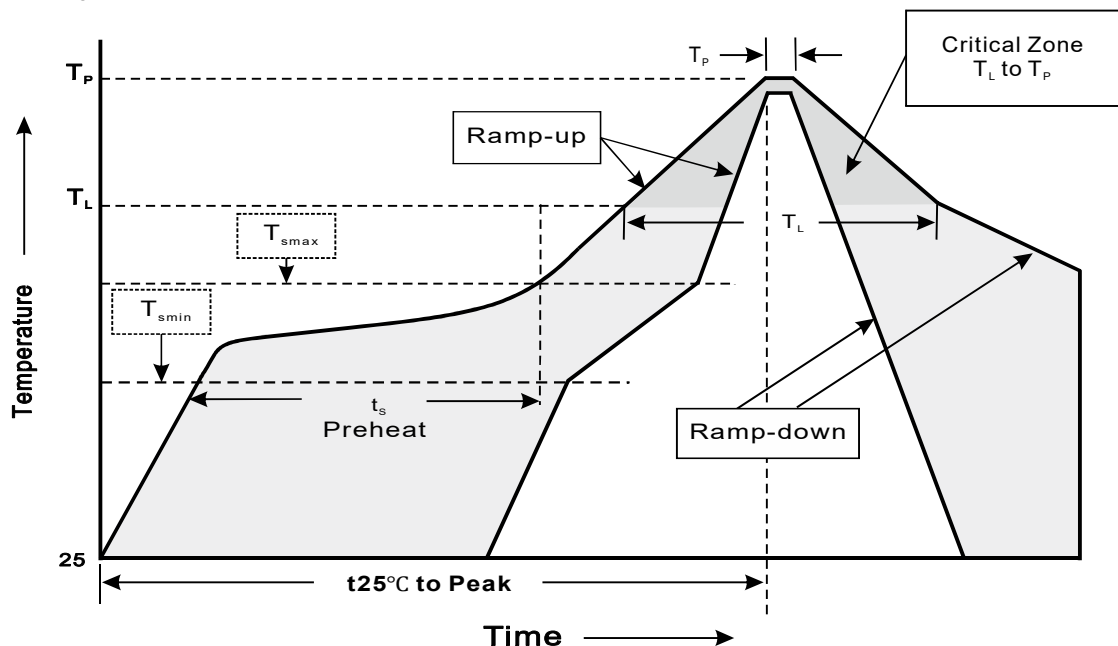
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Reel packing

Device	Outline	Package	Reel Size	Reel (PCS)
FMOSAC52N06-Q1	TAPING	T5060P8	13inch	5,000

Suggested thermal profiles for soldering processes

- 1.Storage environment : Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering Condition
Average ramp-up rate (T_L to T_p)	$< 3^\circ\text{C/sec}$
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (min to max) (t_s)	150°C 200°C 60 ~ 120sec
T_{smax} to T_L -Ramp-up rate	$< 3^\circ\text{C/sec}$
Time maintained above: -Temperature (T_L) -Time(T_L)	217°C 60 ~ 260 sec
Peak Temperature(T_p)	255°C -0/+5°C
Time within 5°C of actual peak Temperature(T_p)	10 ~ 30sec
Ramp-down rate	$< 6^\circ\text{C/sec}$
Time 25°C to peak temperature	< 6 minutes