

FMOSAC43N06-H

List

List.....	1
Package outline.....	2
Features.....	2
Mechanical data.....	2
Maximum ratings	2
Electrical characteristics.....	3
Rating and characteristic curves.....	4~6
Pinning information.....	6
Marking.....	6
Suggested solder pad layout.....	6
Packing information.....	7
Reel packing.....	8
Suggested thermal profiles for soldering processes.....	8

FMOSAC43N06-H

43A 60V N-Channel Power MOSFET

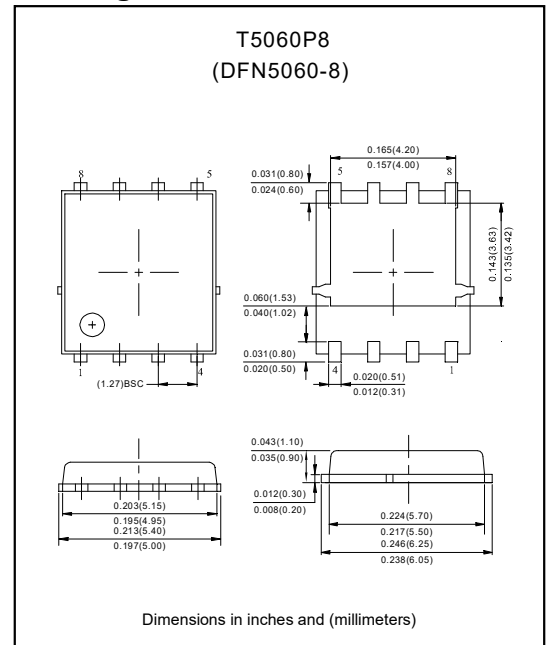
Features

- $V_{DS} = 60V$, $I_D = 43A$.
- $R_{DS(ON)} \leq 9.4m\Omega @ V_{GS} = 10V$, $I_D = 20A$.
 $R_{DS(ON)} \leq 12m\Omega @ V_{GS} = 4.5V$, $I_D = 15A$.
- Ultra-low on-resistance, $R_{DS(ON)}$.
- Low gate charge Q_g .
- 100% UIS and R_g Tested.
- Lead-free parts meet RoHS requirements.

Mechanical data

- Epoxy: UL94-V0 rated flame retardant.
- Case : Molded plastic, T5060P8 (DFN5060-8).
- Weight : Approximated 69mg.

Package outline

Maximum ratings (At $T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain Current (Note 1)	I_D	43	A
		27	
Pulsed drain current (Note 2)	I_{DM}	156	A
Avalanche current (Note 3)	I_{AS}	26	A
Single pulse avalanche energy (Note 3)	E_{AS}	34	mJ
Power dissipation (Note 4)	P_D	31	W
		12.5	
Operating Junction temperature	T_J	+175	$^\circ C$
Storage temperature range	T_{STG}	-55 to +175	$^\circ C$
Thermal resistance, Junction to ambient	$R_{\theta JA}$	55	$^\circ C/W$
Thermal resistance Junction to case	$R_{\theta JC}$	4	$^\circ C/W$

FMOSAC43N06-H

Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise noted)

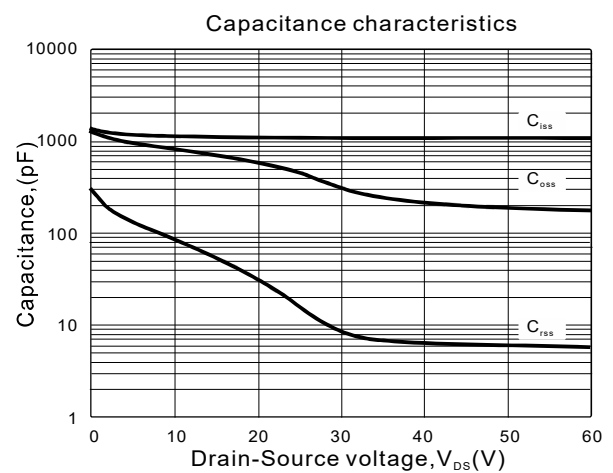
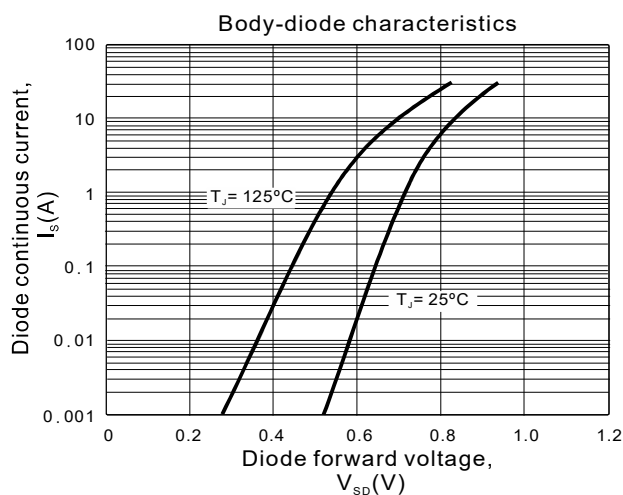
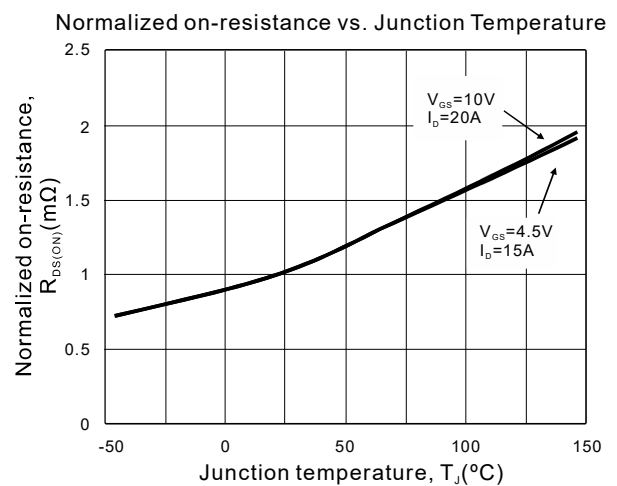
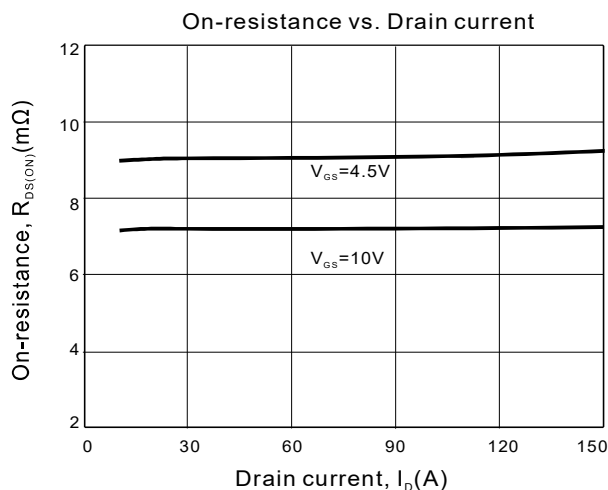
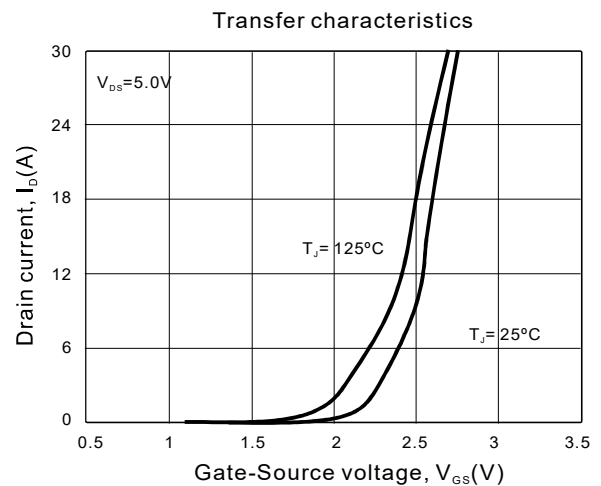
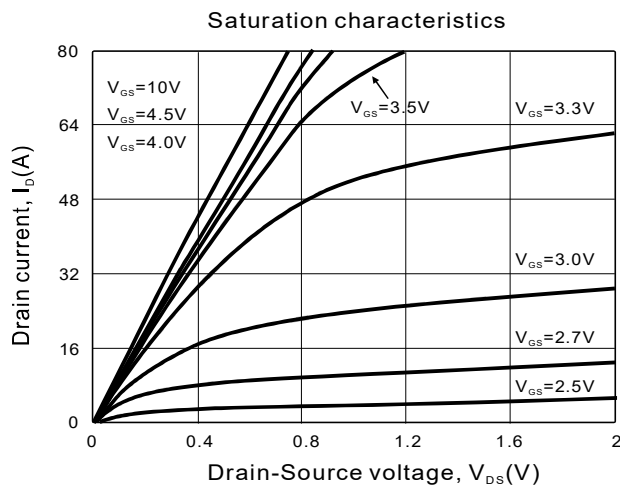
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	60			V
Drain-source leakage current	I _{DSS}	V _{DS} =48V, V _{GS} =0V			1	μA
		V _{DS} =48V, V _{GS} =0V, T _J =55°C			5	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
On characteristics						
Gate threshold voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D =250μA	1.2	1.5	2.5	V
Static drain-source on-resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		7.2	9.4	mΩ
		V _{GS} =4.5V, I _D =15A		9	12	
Forward transconductance	g _{FS}	V _{DS} =5V, I _D =20A		85		S
Dynamic parameters (Note 5)						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =30V, f=1.0MHz		1087		pF
Out capacitance	C _{oss}			309		
Reverse transfer capacitance	C _{rss}			8.5		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		1.6		Ω
Switching parameters (Note 5)						
Total gate charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =20A		16.6		nC
		V _{GS} =4.5V, V _{DS} =30V, I _D =20A		8.3		
Gate to source charge	Q _{gs}	V _{GS} =10V, V _{DS} =30V, I _D =20A		2.6		
Gate to drain charge	Q _{gd}			2.7		
Turn-on delay time	t _{d(on)}	V _{DS} =30V, V _{GS} =10V, R _L =1.5Ω, R _G =6Ω		4.7		ns
Rise time	t _r			7.6		
Turn-off delay time	t _{d(off)}			24		
Fall time	t _f			8.9		
Source-drain diode ratings and characteristics						
Maximum body-diode continuous current	I _S	T _C =25°C			31	A
Drain-source diode forward voltage	V _{SD}	I _S =1A, V _{GS} =0V		0.69	1	V
Body diode reverse recovery time	t _{rr}	I _F =15A, dI _F /dt=100A/μs		26		ns
Body diode reverse recovery charge	Q _{rr}			13.4		nC

Notes :

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under $T_{J_Max} = 150^{\circ}\text{C}$
3. This single-pulse measurement was taken under the following condition [$L = 100\mu\text{H}$, $V_{GS} = 10\text{V}$, $V_{DS} = 30\text{V}$] while its value is limited by $T_{J_Max} = 150^{\circ}\text{C}$.
4. The power dissipation P_D is based on $T_{J_Max} = 150^{\circ}\text{C}$
5. This value is guaranteed by design hence it is not included in the production test.

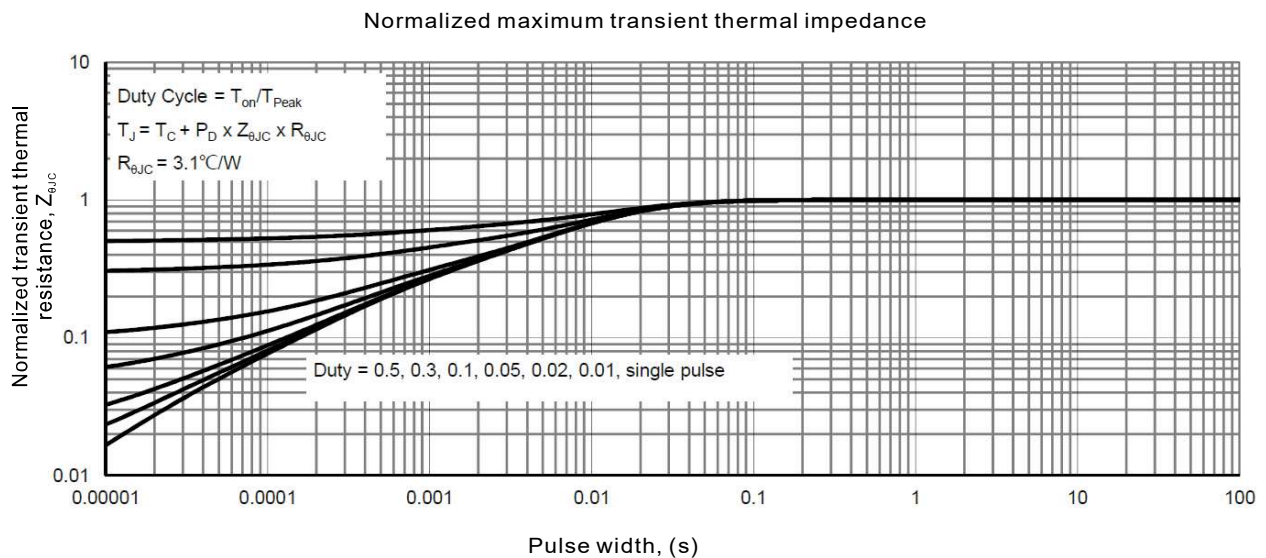
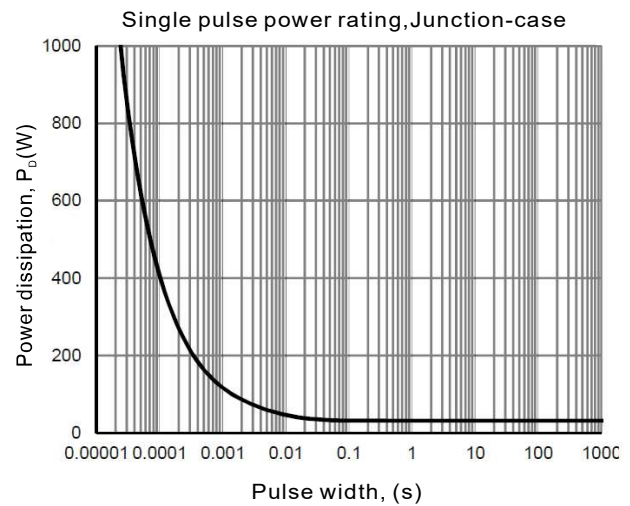
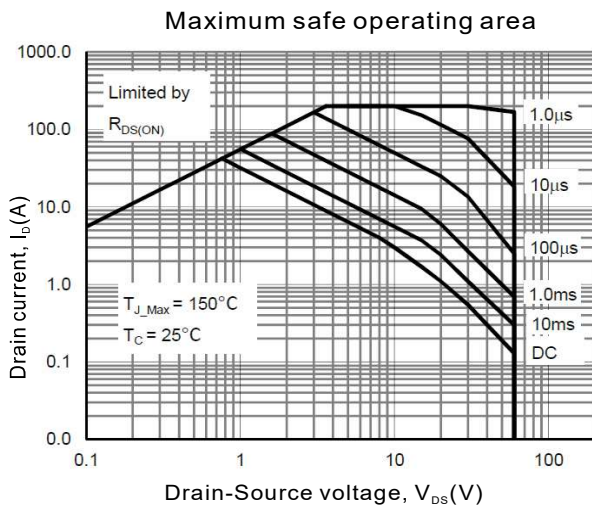
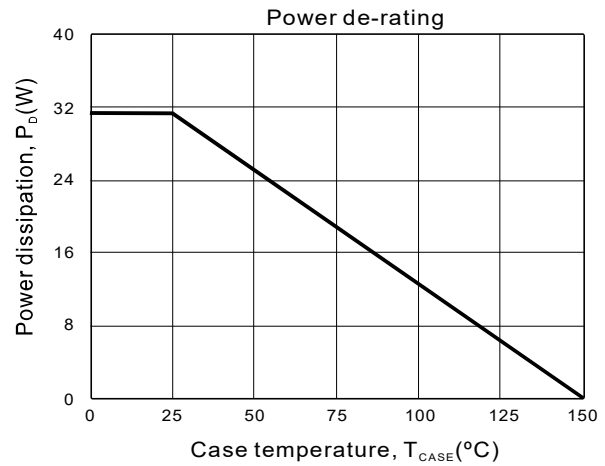
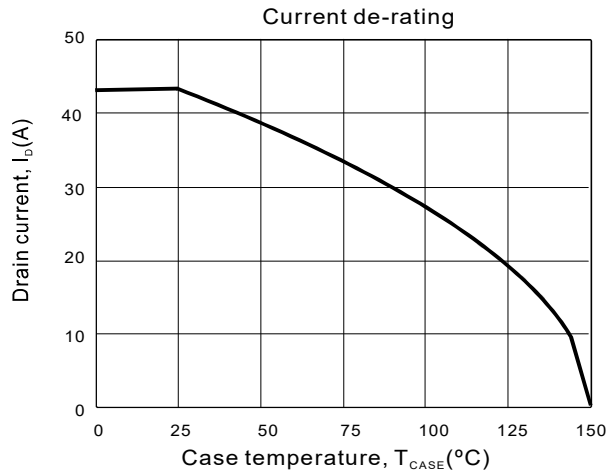
FMOSAC43N06-H

Rating and characteristic curves



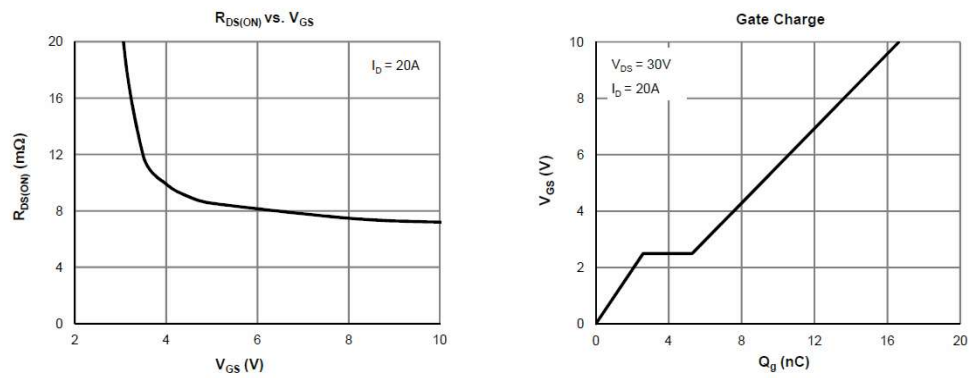
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Rating and characteristic curves



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Rating and characteristic curves



Pinning information

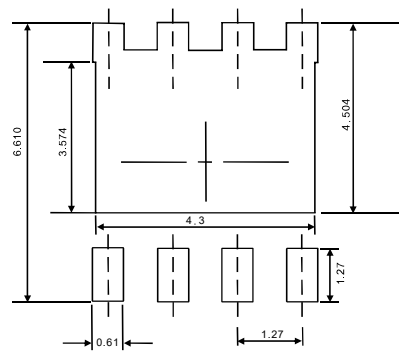
Pin	Simplified outline	Symbol
Pin 1, 2, 3 Source Pin 4 Gate Pin 5, 6, 7, 8 Drain		

Marking

Type number	Marking code
FMOSAC43N06-H	

Suggested solder pad layout

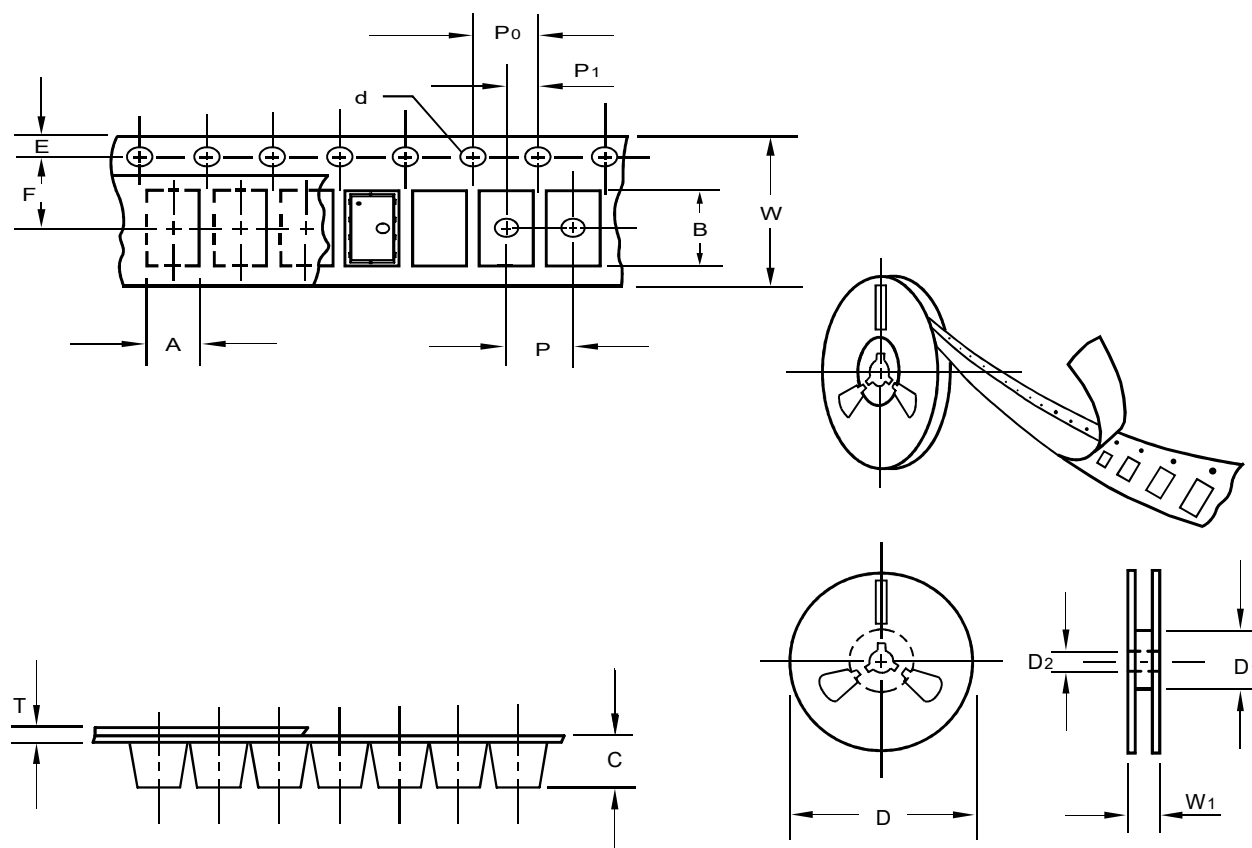
T5060P8



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.1mm$
3. The pad layout is for reference purposes only.

FMOSAC43N06-H

Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8 (DFN5060-8)
Carrier width	A	0.1	6.40
Carrier length	B	0.1	5.40
Carrier depth	C	0.1	1.25
Sprocket hole	d	0.1	1.55
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D1	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D1	min	-
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.30
Tape width	W	0.3	12.00
Reel width	W1	1.0	17.60

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

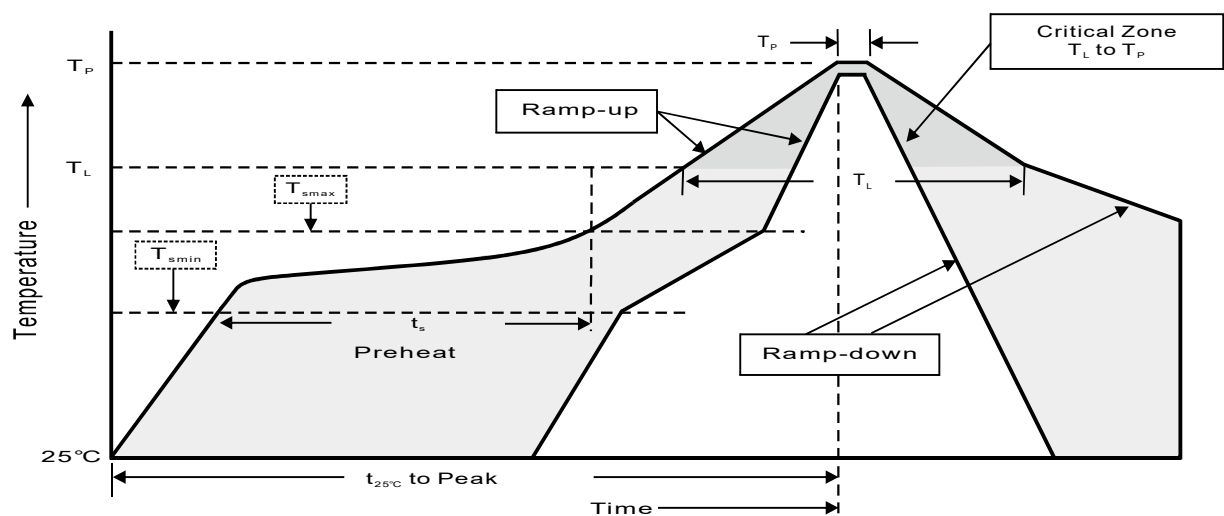
FMOSAC43N06-H

Reel packing

Device	Outline	Device Package	Reel Size	Reel (pcs)
FMOSAC43N06-H	Taping	T5060P8	13 inch	5000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature = 5°C ~ 40°C Humidity = 55%, ±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_p)	< 3 °C/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150°C 200°C 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 °C/sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217°C 60 ~ 260 sec
Peak temperature (T_p)	255 °C -0/+5°C
Time with 5°C of actual peak temperature (T_p)	10 ~30 sec
Ramp-down rate	< 6 °C/sec
Time 25°C to peak temperature	< 6 minutes