FMOSAC4064

List

FMOSAC4064

85A 40V N-Channel Enhancement Mode Power MOSFET

Features

- V_{DS}=40V, I_D=85A.
- $R_{DS(ON)}$ ≤ 2.8mΩ, @ V_{GS}=10V, I_D=15A.
- $R_{DS(ON)}$ ≤ 4.0mΩ, @ V_{GS}=4.5V,I_D=15A.
- 100% E_{AS} guaranteed.
- Low on-resistance.
- Advanced trench MOS technology.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen-free part, ex.FMOSAC4064-H.

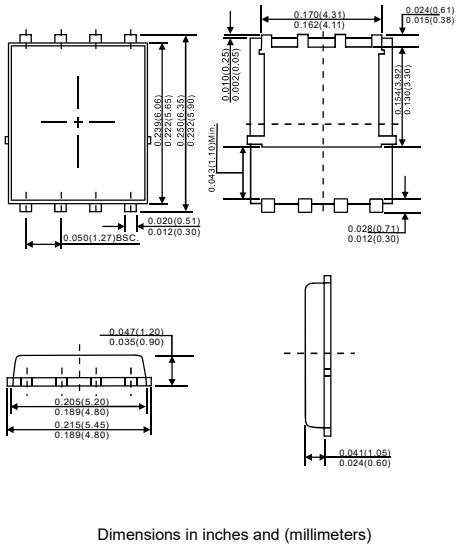
Applications

- SMPS synchronous rectification.
- DC/DC converters.
- Or-ing.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic,T5060P8.
- Mounting Position : Any.

Package outline



Dimensions in inches and (millimeters)

Maximum ratings (At T_C=25°C unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	±20	V
Continuous drain current ,V_{GS}@10V (Note1,6) (T_C=25°C)	I_D	85	A
Continuous drain current ,V_{GS}@10V (Note1,6) (T_C=100°C)	I_D	67	A
Pulsed drain current (Note2)	I_{DM}	250	A
Avalanche current	I_{AS}	32	A
Single pulse avalanche energy (Note3)	E_{AS}	256	mJ
Power dissipation (Note4) T_C=25°C	P_D	48	W
Thermal resistance Junction to ambient (Note1)	$R_{\theta JA}$	50	°C/W
Thermal resistance Junction to case (Note1)	$R_{\theta JC}$	2.6	°C/W
Operating Junction temperature	T_J	+150	°C
Storage temperature range	T_{STG}	-55 to +150	°C

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Electrical characteristics (At T_C=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off characteristics						
Drain-source breakdown voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	40			V
Drain-source leakage current	I_{DSS}	V_{DS}=32V, V_{GS}=0V, T_J=25°C			1	μA
		V_{DS}=32V, V_{GS}=0V, T_J=55°C			5	
Gate-source leakage current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
On characteristics						
Gate threshold voltage	$V_{GS(TH)}$	V_{GS}=V_{DS}, I_D=250μA	1.2	1.6	2.2	V
Static drain-source on-resistance (Note 2)	$R_{DS(ON)}$	V_{GS}=10V, I_D=15A		1.9	2.8	mΩ
		V_{GS}=4.5V,I_D=15A		2.8	4.0	
Dynamic parameters						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=20V, f=1.0MHz		2894		pF
Out capacitance	C_{oss}			1309		
Reverse transfer capacitance	C_{rss}			145		
Gate resistance	R_g	V_{DS}=0V, V_{GS}=0V, f=1.0MHz		0.8		Ω
Switching parameters						
Total gate charge	Q_g	V_{GS}=4.5V, V_{DS}=15V, I_D=15A		28.6		nC
Gate to source charge	Q_{gs}			7.5		
Gate to drain charge	Q_{gd}			11.9		
Turn-on delay time	$t_{d(on)}$	V_{DD}=15V, V_{GS}=10V, R_G=3.3Ω, I_D=15A		12		ns
Rise time	t_r			7		
Turn-off delay time	$t_{d(off)}$			35		
Fall time	t_f			6		
Source-drain diode ratings and characteristics						
Drain-source diode forward voltage (Note 2)	V_{SD}	I_S=1A, V_{GS}=0V, T_J=25°C			1.2	V
Continuous source current (Note 1, 6)	I_S	V_G=V_D=0V, Force current			85	A

Note: 1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
3.The E_{AS} data shows maximum rating . The test condition is V_{DD}=25V, V_{GS}=10V, L=0.5mH, I_{AS}=32A .
4.The power dissipation is limited by 150°C junction temperature.
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
6.Package limitation current is 85A.

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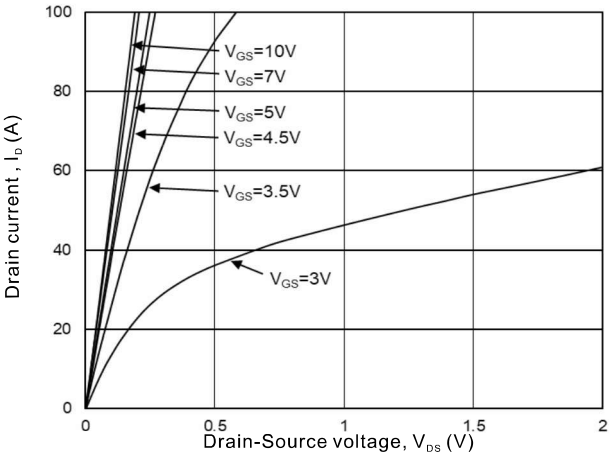
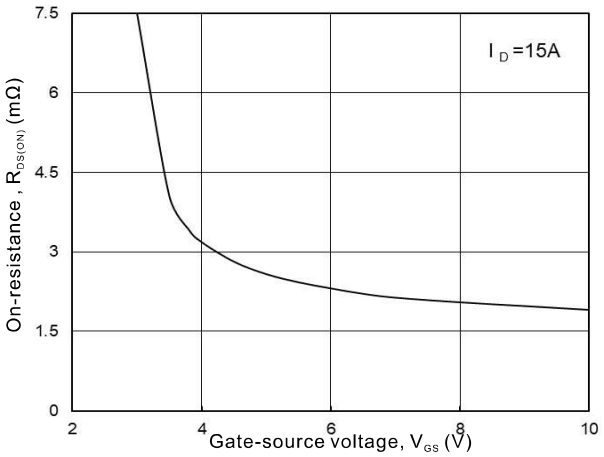
Rating and characteristic curves

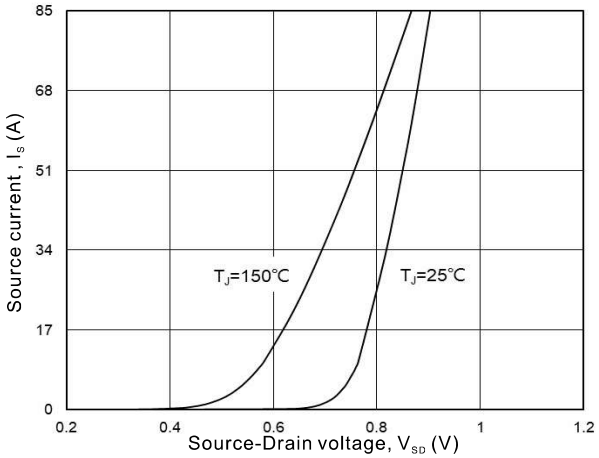
Typical output characteristics



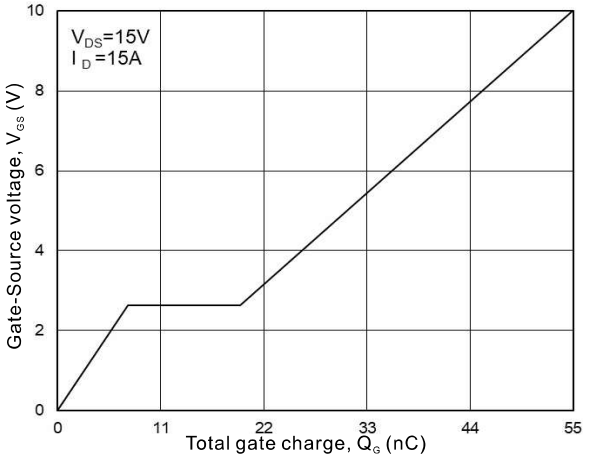
On-resistance vs. Gate-Source voltage



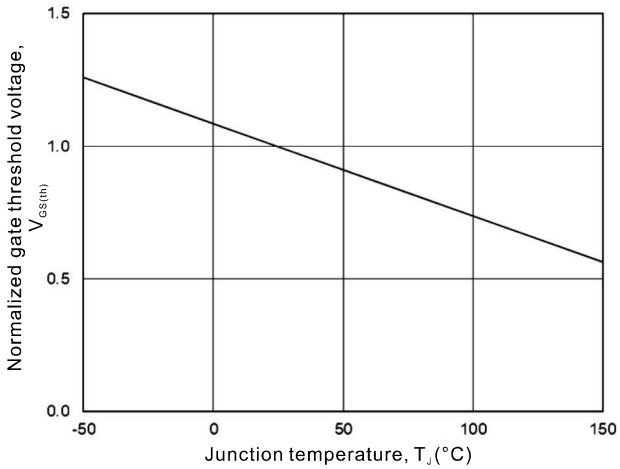
Source current vs. Source-Drain voltage characteristics



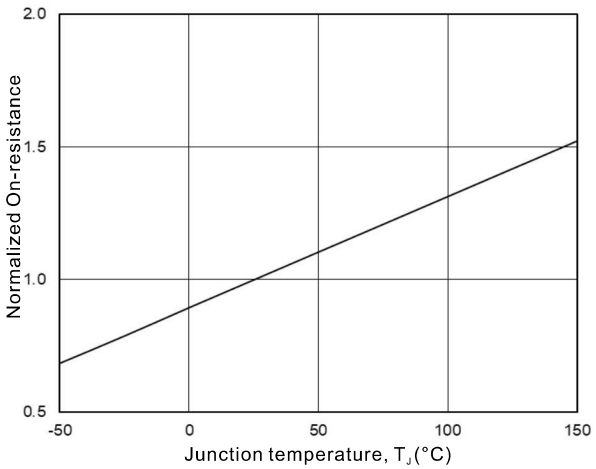
Gate charge characteristics



Normalized $V_{GS(th)}$ vs. Junction temperature



Normalized $R_{DS(ON)}$ vs. Junction temperature



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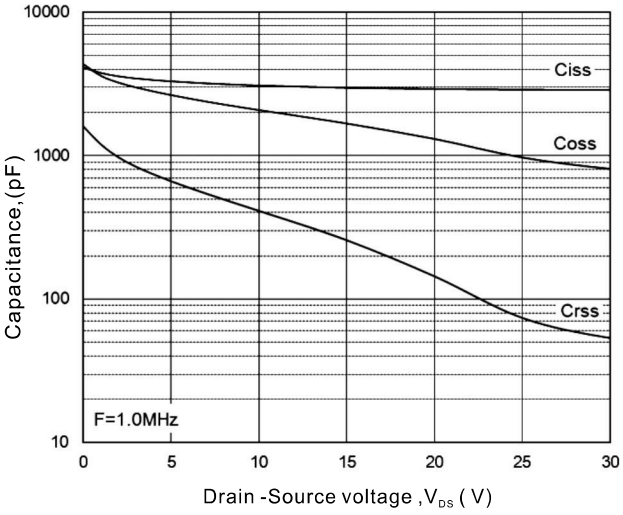
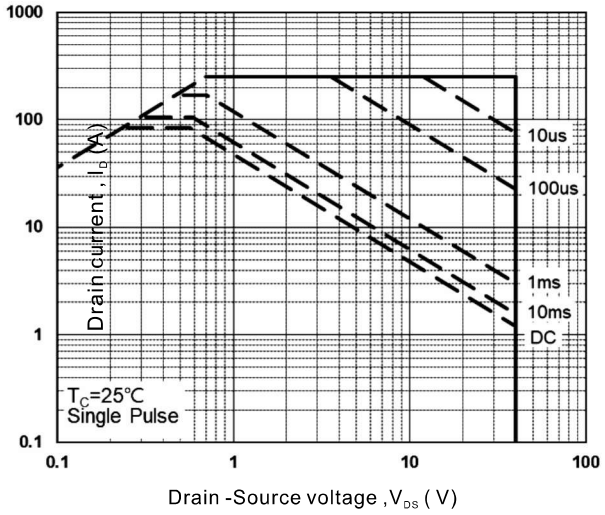
Rating and characteristic curves

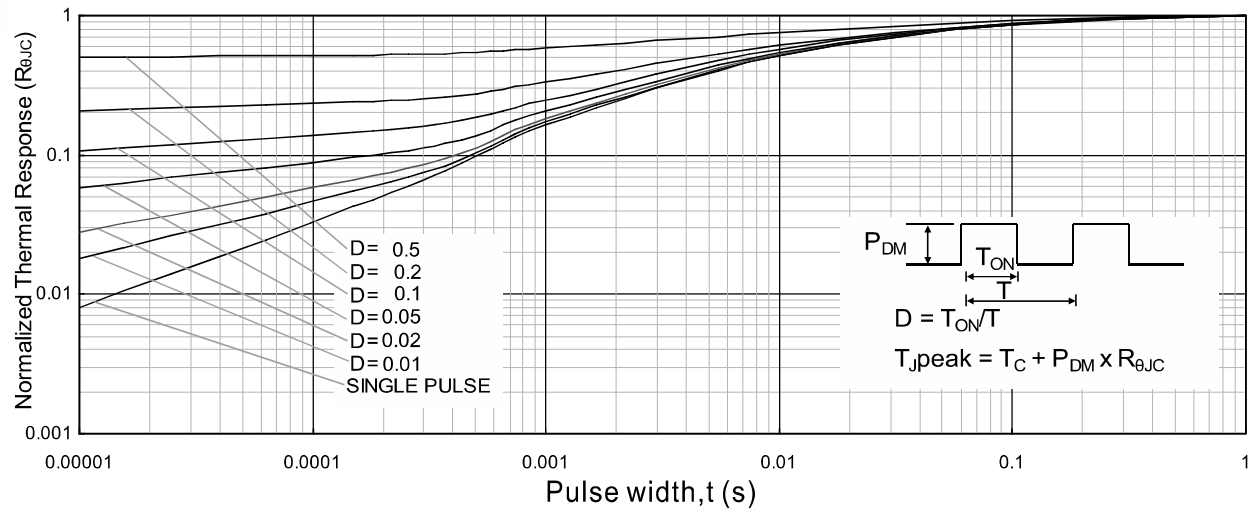
Capacitance



Safe operating area



Normalized maximum transient thermal impedance



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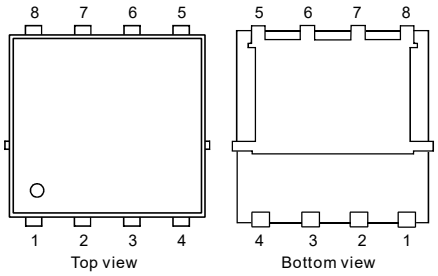
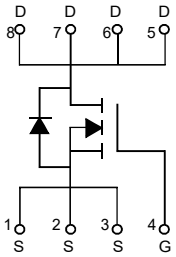
Pinning information

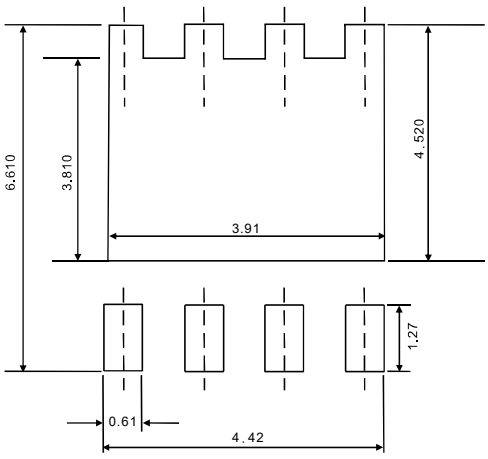
Pin	Simplified outline	Symbol
Pin 1, 2, 3, Source Pin 4 Gate Pin 5, 6, 7, 8 Drain		

Marking

Type number	Marking code
FMOSAC4064	AC4064

Suggested solder pad layout

T5060P8



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ±0.1mm
3. The pad layout is for reference purposes only.

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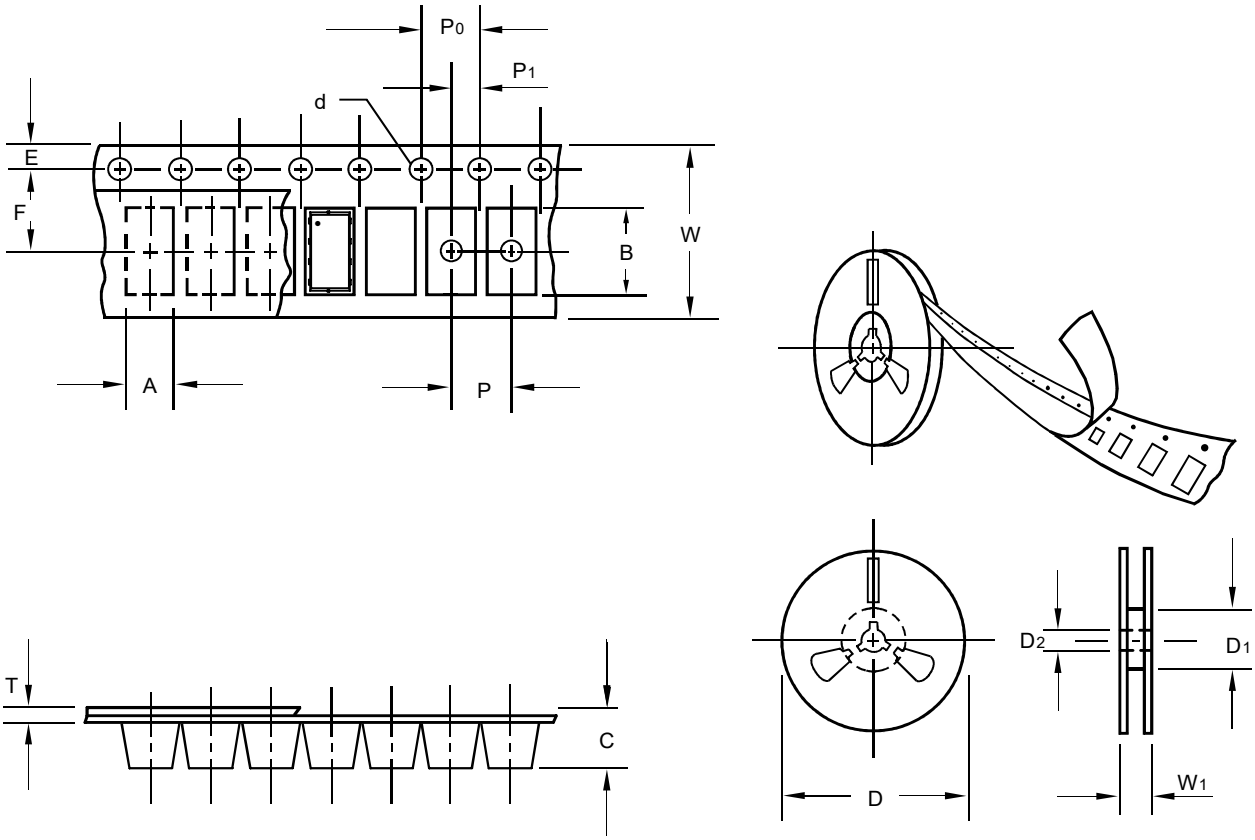
Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8
Carrier width	A	0.1	6.50
Carrier length	B	0.1	5.30
Carrier depth	C	0.1	1.40
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D_1	min	176.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D_1	min	-
Feed hole diameter	D_2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P_0	0.1	4.00
Embossment center	P_1	0.1	2.00
Overall tape thickness	T	0.1	0.30
Tape width	W	0.3	12.00
Reel width	W_1	1.0	18.40

Note:Devices are packed in accor dance with EIA standar RS-481-A and specifications listed above.

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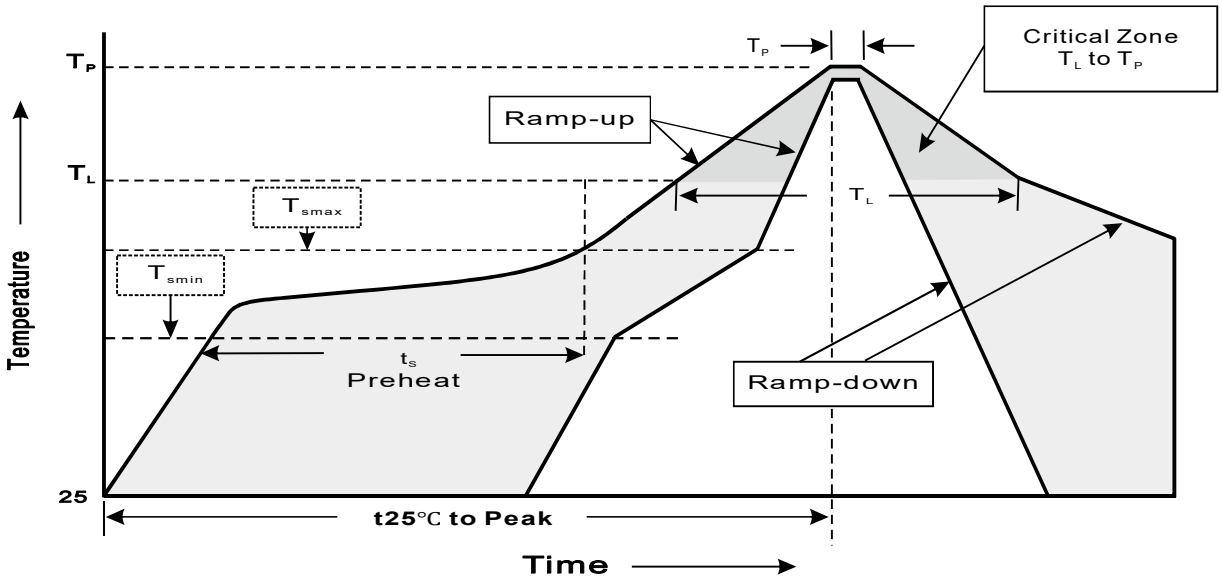
Reel packing

Device	Outline	Device Package	Reel Size	Reel (pcs)
FMOSAC4064	Taping	T5060P8	13 inch	3,000

Suggested thermal profiles for soldering processes

1.Storage environment : Temperature=5℃~40℃ Humidity=55%±25%
2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering Condition
Average ramp-up rate (T_L to T_P)	< 3℃/sec
Prehaeat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (min to max) (t_S)	 150℃ 200℃ 60 ~120sec
T_{smax} to T_L -Ramp-up rate	< 3℃/sec
Time maintained above: -Temperature (T_L) -Time(T_L)	 217℃ 60 ~ 260 sec
Peak Temperature(T_P)	255℃ -0/+5℃
Time within 5℃ of actual peak Temperature(T_P)	10 ~ 30sec
Ramp-down rate	< 6℃/sec
Time 25℃ to peak temperature	< 6 minutes