

FMOSAC112N06-Q1

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FMOSAC112N06-Q1

112A 60V N-Channel Enhancement Mode Power MOSFET

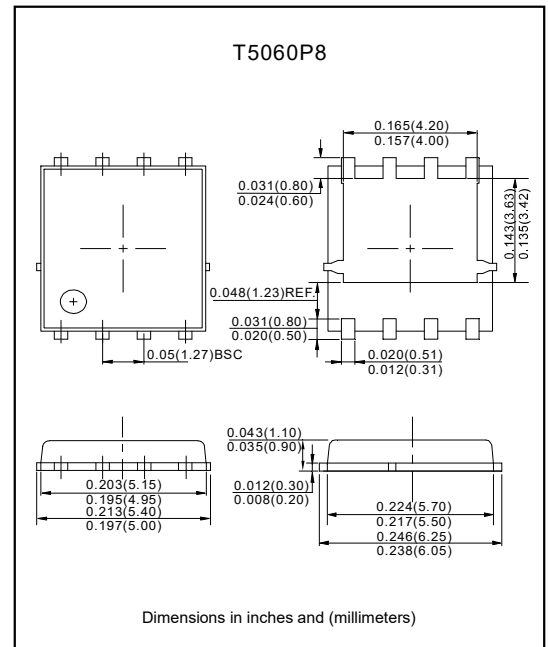
Features

- $V_{DS}=60V$, $I_D=112A$.
- $R_{DS(ON)} \leq 4.5m\Omega$, @ $V_{GS}=10V$, $I_D=20A$.
- $R_{DS(ON)} \leq 5.9m\Omega$, @ $V_{GS}=4.5V$, $I_D=15A$.
- Ultra-low on-resistance.
- Low gate charge.
- 100% UIS and 100% R_g tested.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen-free part, ex.FMOSAC112N06-Q1-H.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, T5060P8.
- Mounting Position : Any.

Package outline



Maximum ratings (At $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current (Note 1)	I_D	$T_c=25^\circ C$ 112	A
		$T_c=100^\circ C$ 79	
Pulsed drain current (Note 2)	I_{DM}	449	A
Avalanche current (Note 3)	I_{AS}	25	A
Single pulse avalanche energy (Note 3)	E_{AS}	94	mJ
Power dissipation (Note 4)	P_D	$T_c=25^\circ C$ 100	W
		$T_c=100^\circ C$ 50	
Thermal resistance, Junction to ambient	$R_{\theta JA}$	62	$^\circ C/W$
Thermal resistance Junction to case	$R_{\theta JC}$	1.7	$^\circ C/W$
Operating Junction temperature	T_J	+175	$^\circ C$
Storage temperature range	T_{STG}	-55 to +175	$^\circ C$

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Electrical characteristics (At $T_J=25^{\circ}\text{C}$ unless otherwise noted)

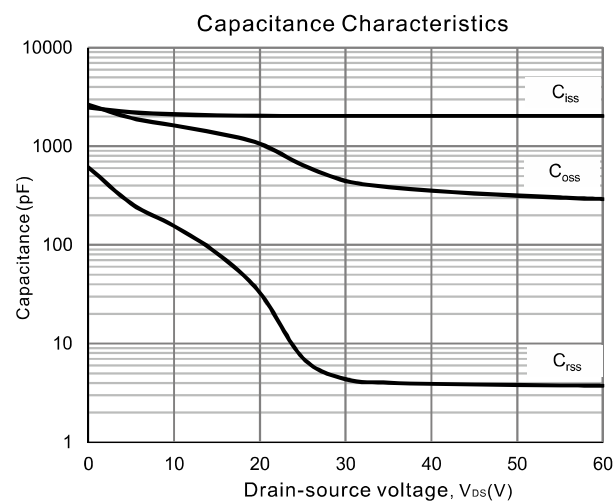
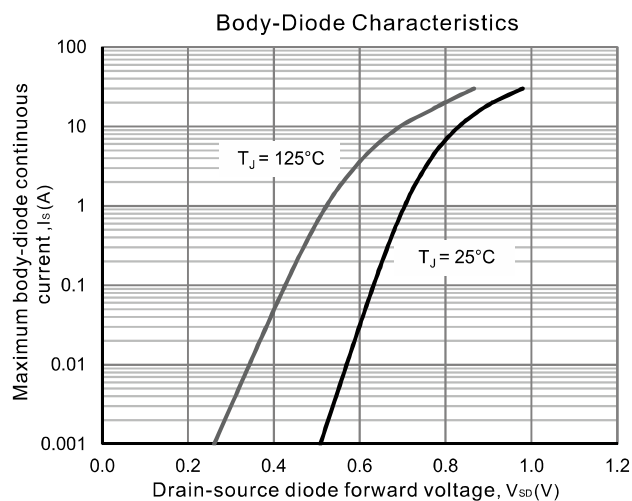
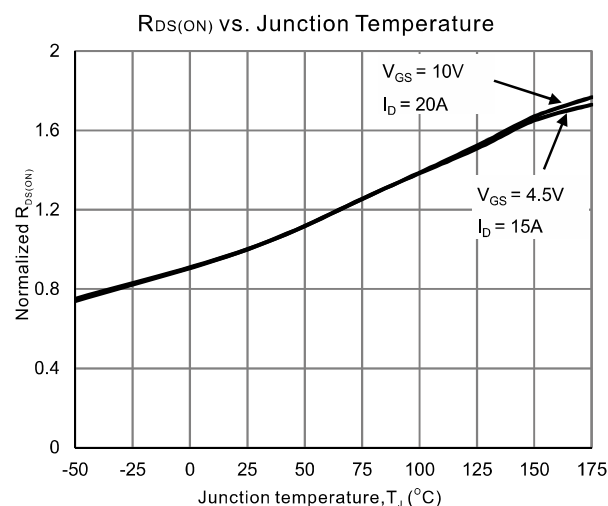
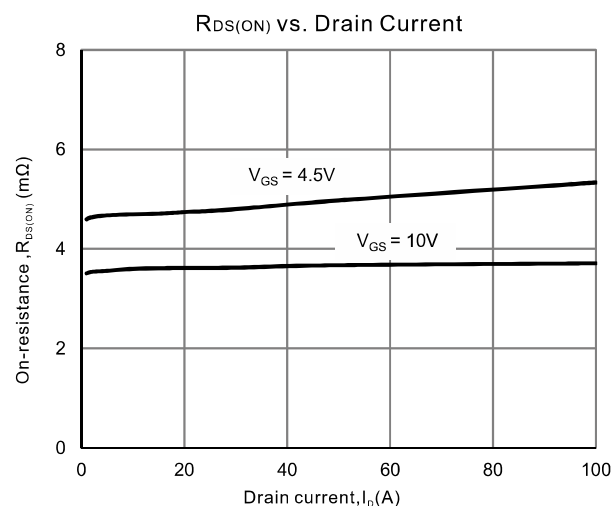
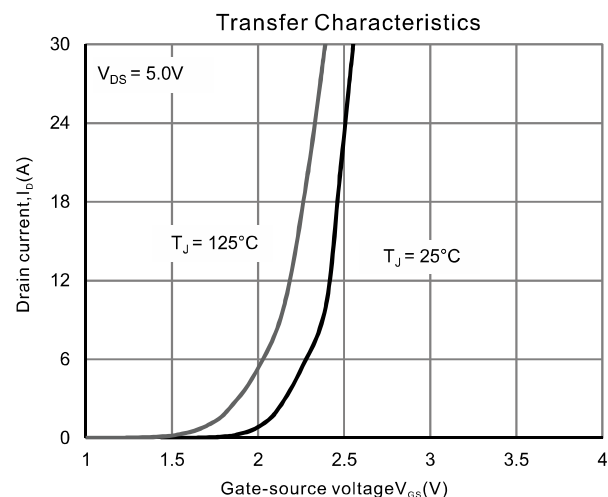
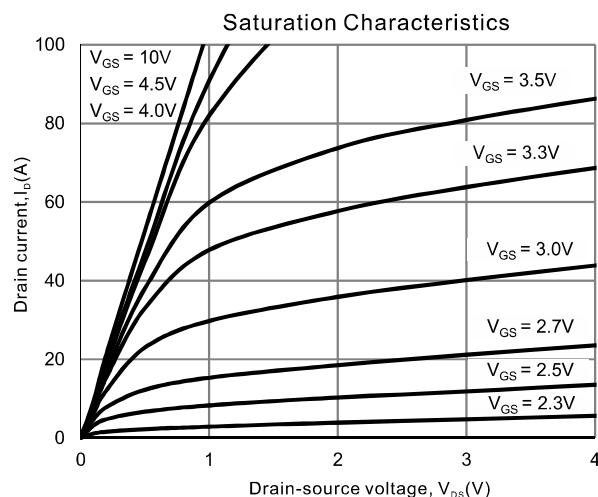
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	60			V
Drain-source leakage current	I _{DSS}	V _{DS} =48V, V _{GS} =0V			1	μA
		V _{DS} =48V, V _{GS} =0V, T _J =55°C			5	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
On characteristics						
Gate threshold voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D =250μA	1.2	1.6	2.5	V
Static drain-source on-resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		3.6	4.5	mΩ
		V _{GS} =4.5V, I _D =15A		4.7	5.9	
Forward transconductance	g _{FS}	V _{DS} =5V, I _D =20A		121		S
Dynamic parameters (Note 5)						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =30V, f=1.0MHz		2030		pF
Out capacitance	C _{oss}			445		
Reverse transfer capacitance	C _{rss}			4.4		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		1.78		Ω
Switching parameters (Note 5)						
Total gate charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =20A		32		nC
		V _{GS} =4.5V, V _{DS} =30V, I _D =20A		14.9		
Gate to source charge	Q _{gs}	V _{GS} =0 to 10V, V _{DS} =30V, I _D =20A		4.4		nC
Gate to drain charge	Q _{gd}			4.9		
Turn-on delay time	t _{d(on)}	V _{DS} =30V, V _{GS} =10V, R _L =1.5Ω, R _G =6Ω		6.3		ns
Rise time	t _r			7.8		
Turn-off delay time	t _{d(off)}			39		
Fall time	t _f			15.5		
Source-drain diode ratings and characteristics						
Maximum body-diode continuous current	I _S	T _C =25°C			100	A
Drain-source diode forward voltage	V _{SD}	I _S =1A, V _{GS} =0V		0.7	1	V
Body diode reverse recovery time	t _{rr}	I _F =20A, dI _F /dt = 100A/μs		39		ns
Body diode reverse recovery charge	Q _{rr}			45		nC

Notes :

1. Computed continuous current assumes the condition of $T_{J(MAX)}$ while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under $T_{J(MAX)}=175^{\circ}\text{C}$.
3. This single-pulse measurement was taken under the following condition ($L=300\mu\text{H}$, $V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$) while its value is limited by $T_{J(MAX)}=175^{\circ}\text{C}$.
4. The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$.
5. This value is guaranteed by design hence it is not included in the production test.

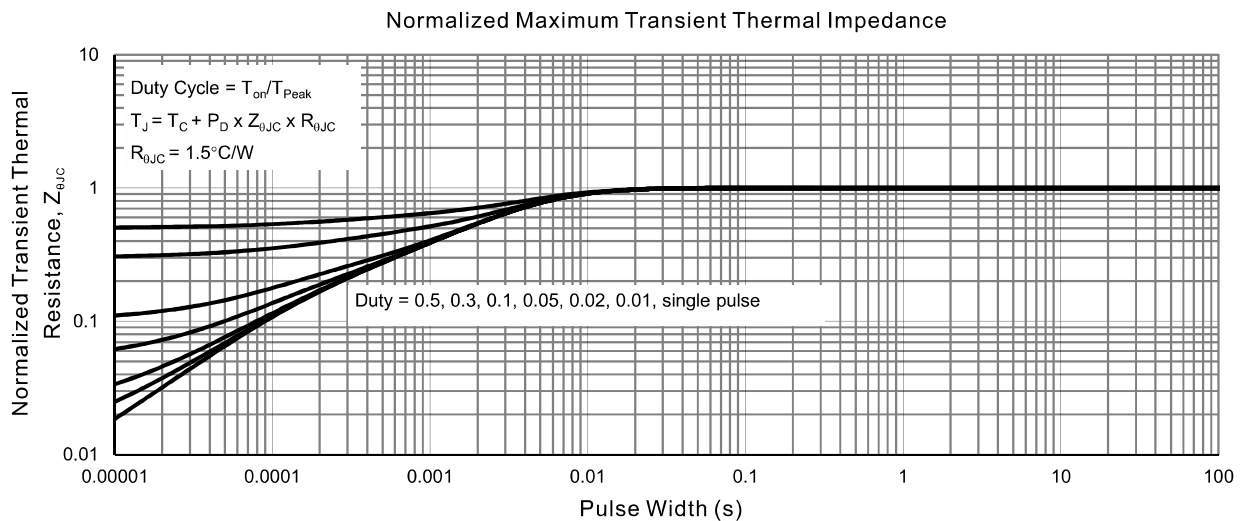
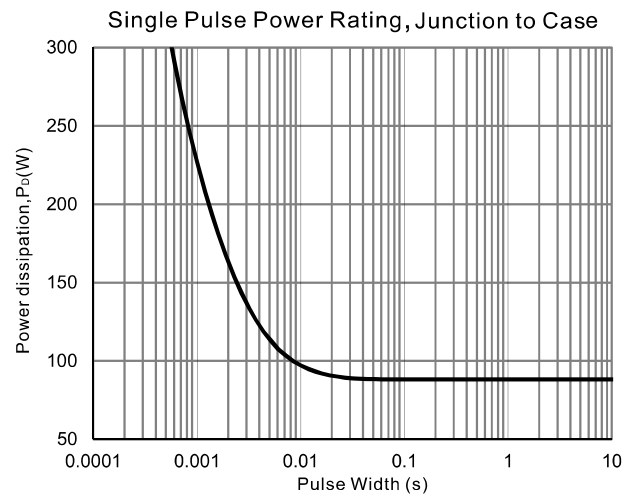
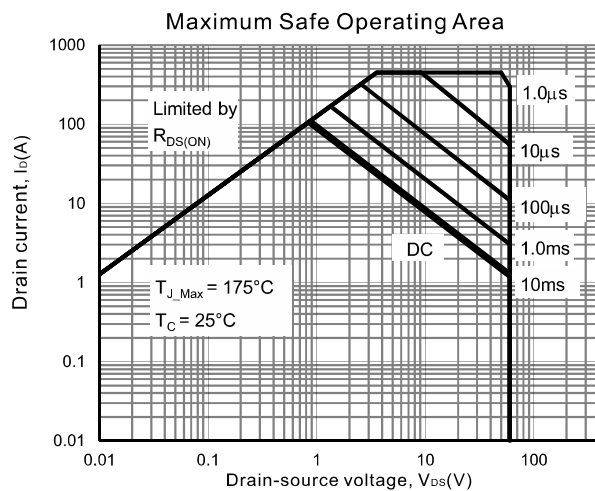
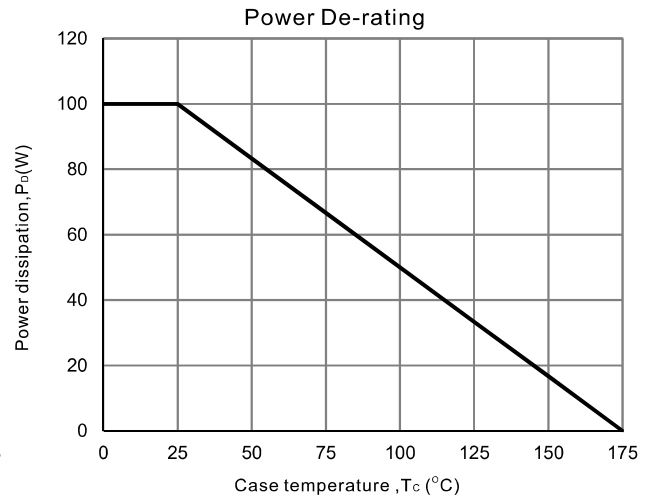
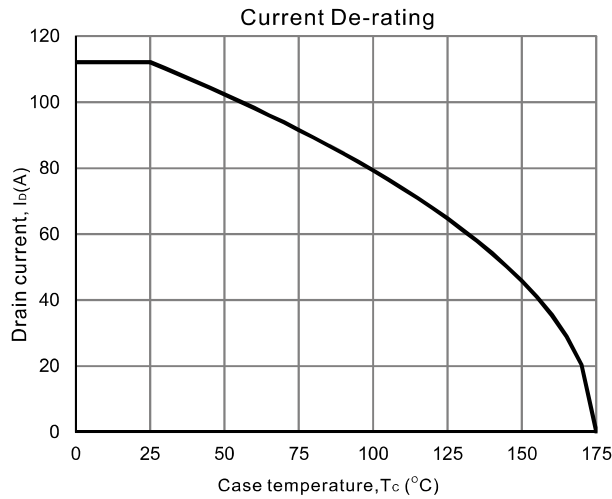
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Rating and characteristic curves



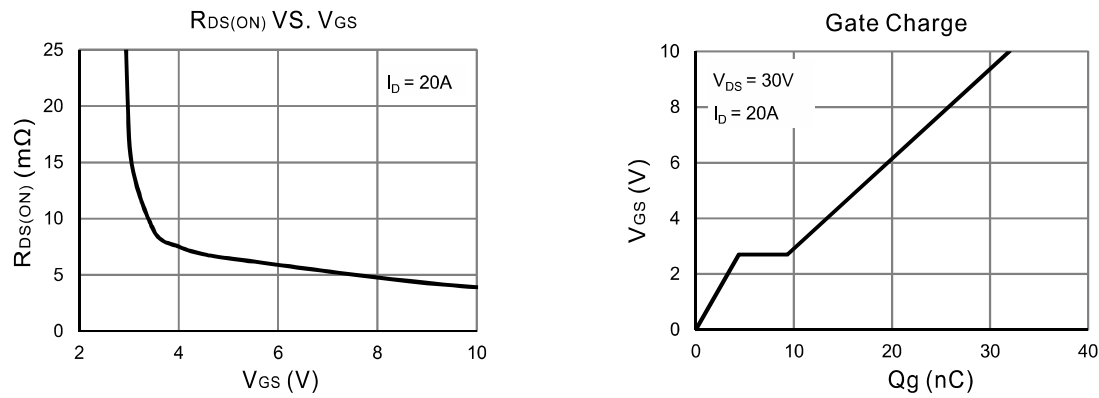
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Rating and characteristic curves



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Rating and characteristic curves



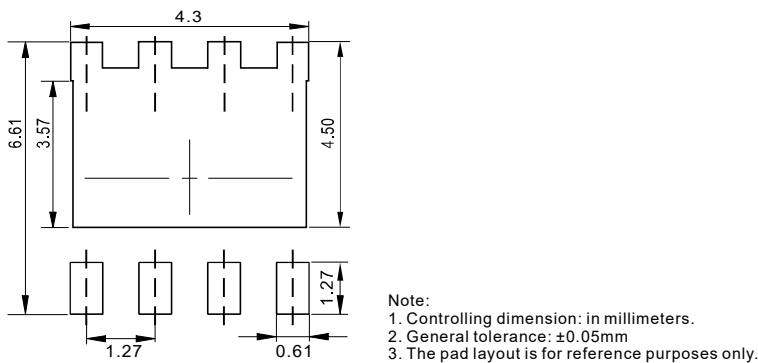
Pinning information

Pin	Simplified outline	Symbol
Pin 1, 2, 3 Source	Top view Bottom view	
Pin 4 Gate		
Pin 5, 6, 7, 8 Drain		

Marking

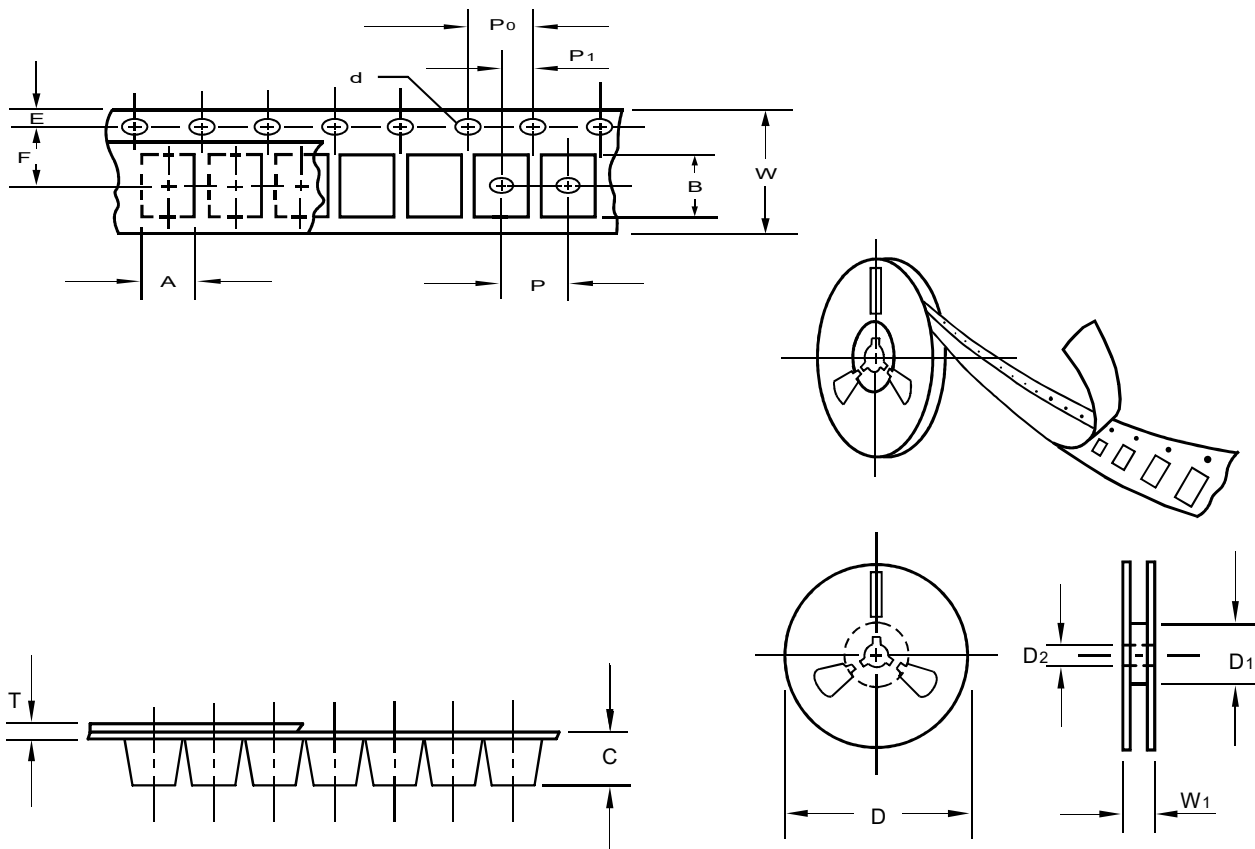
Type numbe	Marking code
FMOSAC112N06-Q1	AC112N06

Suggested solder pad layout



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Packing information



unit:mm

Item	Symbol	Tolerance	T5060P8
Carrier width	A	0.1	6.40
Carrier length	B	0.1	5.40
Carrier depth	C	0.1	1.25
Sprocket hole	d	0.1	1.55
13" Reel outside diameter	D	2.0	330.00
13" Reel inner diameter	D ₁	min	100.00
7" Reel outside diameter	D	2.0	-
7" Reel inner diameter	D ₁	min	-
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	5.50
Punch hole pitch	P	0.1	8.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.30
Tape width	W	0.3	12.00
Reel width	W ₁	1.0	17.60

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

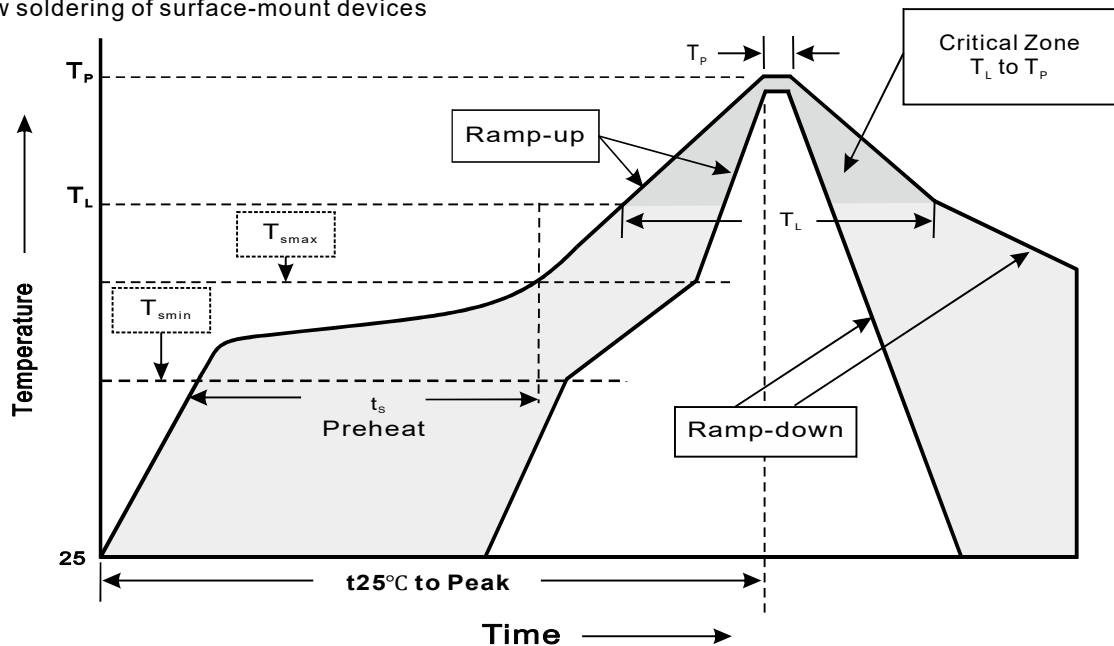
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Reel packing

Device	Outline	Package	Reel Size	Reel (PCS)
FMOSAC112N06-Q1	TAPING	T5060P8	13inch	5000

Suggested thermal profiles for soldering processes

- 1.Storage environment : Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering Condition
Average ramp-up rate (T_L to T_p)	< 3°C/sec
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (min to max) (t_s)	150°C 200°C 60 ~ 120sec
T_{smax} to T_L -Ramp-up rate	< 3°C/sec
Time maintained above: -Temperature (T_L) -Time(T_L)	217°C 60 ~ 260 sec
Peak Temperature(T_p)	255°C -0/+5°C
Time within 5°C of actual peak Temperature(T_p)	10 ~ 30sec
Ramp-down rate	< 6°C/sec
Time 25°C to peak temperature	< 6 minutes