

FMOS3422

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FMOS3422

4.2A 60V N-Channel High Density Trench MOSFET

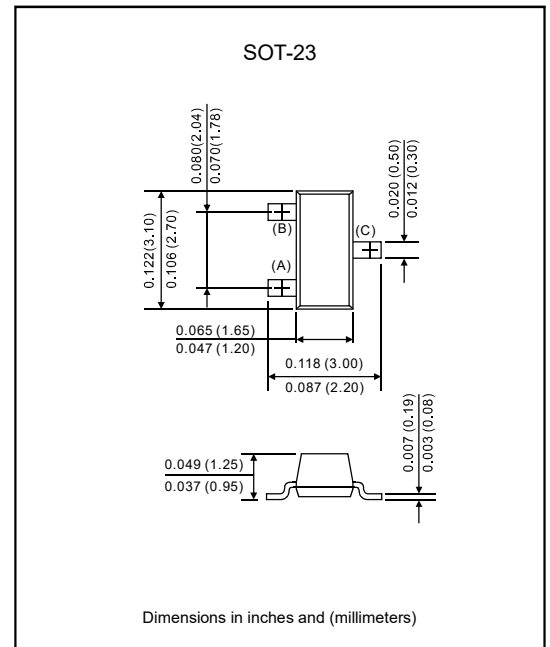
Features

- $V_{DS}=60V$, $I_D=4.2A$.
- $R_{DS(ON)} \leq 90m\Omega$, @ $V_{GS}=10V$, $I_D=4.2A$.
- $R_{DS(ON)} \leq 105m\Omega$, @ $V_{GS}=4.5V$, $I_D=2.8A$.
- Super high density cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen-free part, ex.FMOS3422-H.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, SOT-23.
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026.
- Mounting Position : Any.

Package outline



Maximum ratings (At $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Units
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current (Note 1)	I_D	4.2	A
Pulsed drain current (Note 2)	I_{DM}	20	A
Drain-source diode forward current (Note 1)	I_S	2.5	A
Power dissipation (Note 1)	P_D	1.25	W
		0.75	
Thermal resistance, junction to ambient (Note 1)	$R_{\theta JA}$	100	$^\circ C/W$
Operation junction temperature	T_J	+150	$^\circ C$
Storage temperature range	T_{STG}	-55 to +150	$^\circ C$

Note: 1. Surface mounted on FR4 board, $t \leq 10\text{sec}$.

2. Pulse width limited by maximum junction temperature.

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Electrical characteristics (At $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Condition	Symbol	Min	Typ	Max	Units
Off characteristics						
Drain-source breakdown voltage	$V_{GS}=0\text{V}, I_D=250\text{A}$	$B_{V_{DS}}$	60			V
Zero gate voltage drain current	$V_{DS}=60\text{V}, V_{GS}=0\text{V}$	I_{DSS}			1	μA
Gate-body leakage current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	I_{GSS}			± 100	nA

On characteristics (Note1)

Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	$V_{GS(th)}$	1	1.5	2	V
Drain-source on-state resistance	$V_{GS}=10\text{V}, I_D=4.2\text{A}$	$R_{DS(on)}$		79	90	m Ω
	$V_{GS}=4.5\text{V}, I_D=2.8\text{A}$			88	105	
Forward transconductance	$V_{DS}=5\text{V}, I_D=3\text{A}$	g_{FS}		10		s

Dynamic parameters (Note2)

Input capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1.0\text{MHz}$	C_{iss}		551		pF
Output capacitance		C_{oss}		54		
Reverse transfer capacitance		C_{rss}		46		

Switching parameters (Note2)

Total gate charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=3\text{A}$	Q_g		13.2		nC
Gate-source charge		Q_{gs}		2.2		
Gate-drain charge		Q_{gd}		1.7		
Turn-on delay time	$V_{DD}=15\text{V}, I_D=1\text{A}, V_{GEN}=10\text{V}, R_L=15\Omega, R_{GEN}=6\Omega$	$t_{d(on)}$		6.5		ns
Turn-on rise time		t_r		2		
Turn-off delay time		$t_{d(off)}$		28.6		
Turn-off fall time		t_f		2.6		

Source-drain diode ratings and characteristics (Note1)

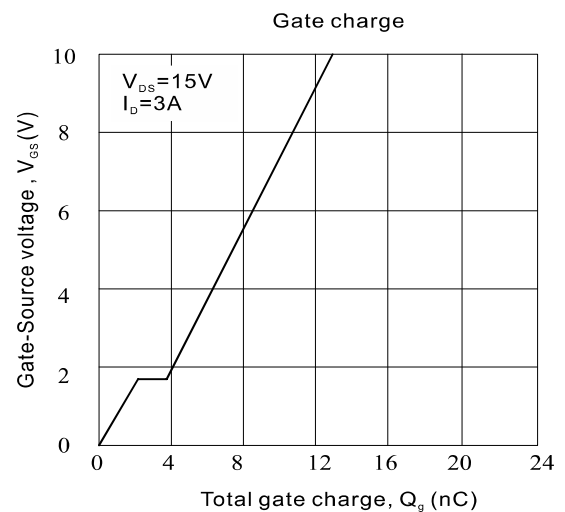
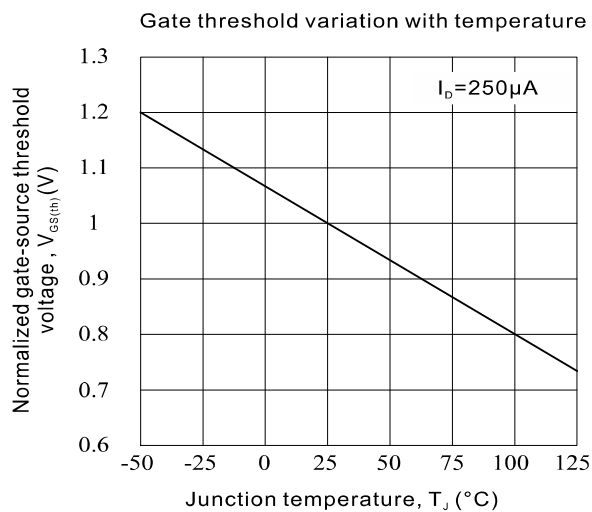
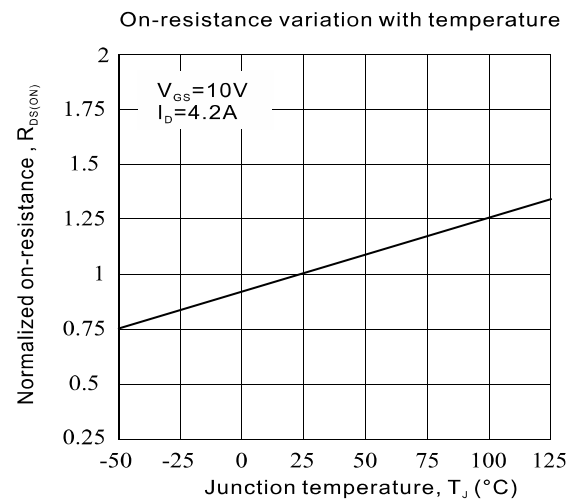
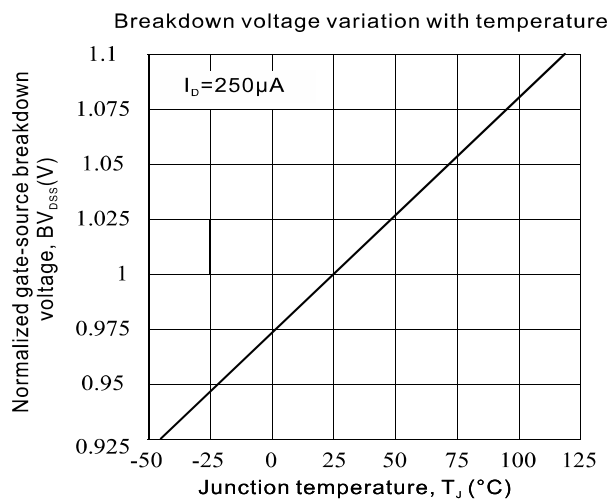
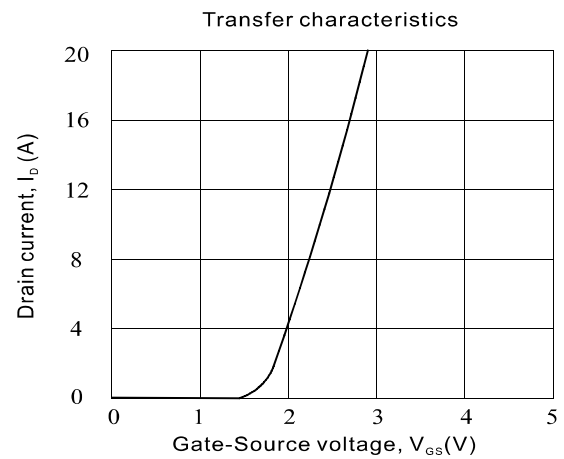
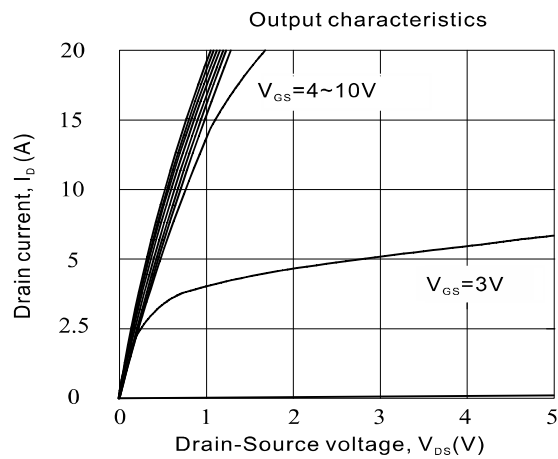
Drain-source diode forward voltage (Note 4)	$V_{GS}=0\text{V}, I_S=1\text{A}$	V_{SD}			1.2	V
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Note: 1. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

2. Guaranteed by design, not subject to production testing.

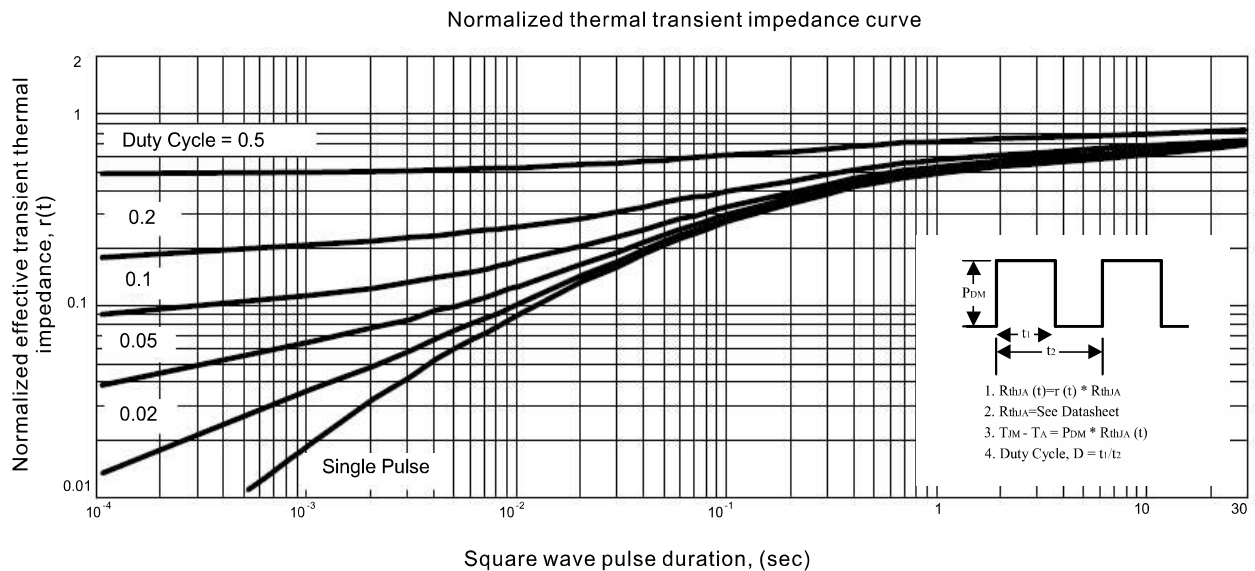
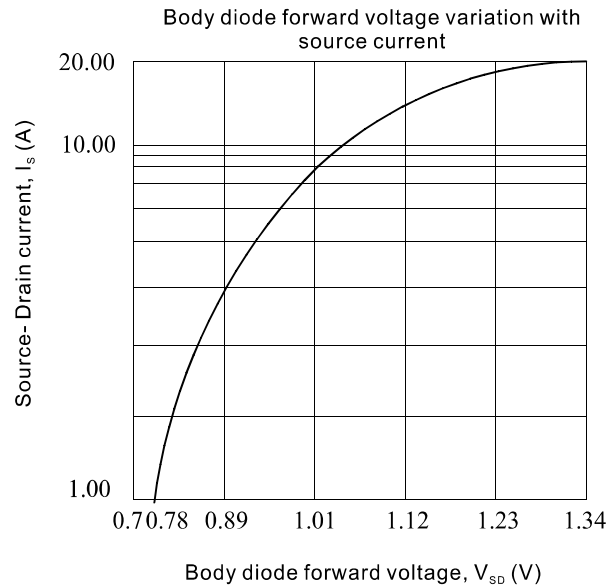
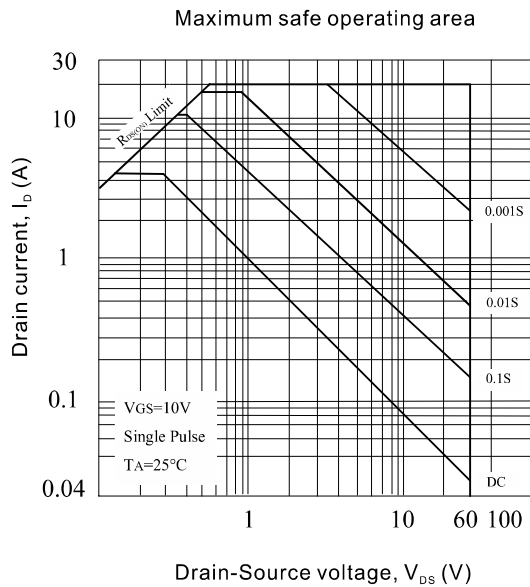
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Rating and characteristic curves



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Rating and characteristic curves



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Pinning information

Pin	Simplified outline	Symbol
Pin 1 Gate Pin 2 Source Pin 3 Drain		

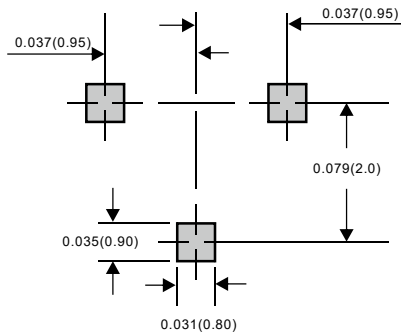
Marking

Type number	Marking code
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Note:1. "ARMA" is a fixed code.
2. "YWW" is the wafer lot code.
Y : year
WW: week

Suggested solder pad layout

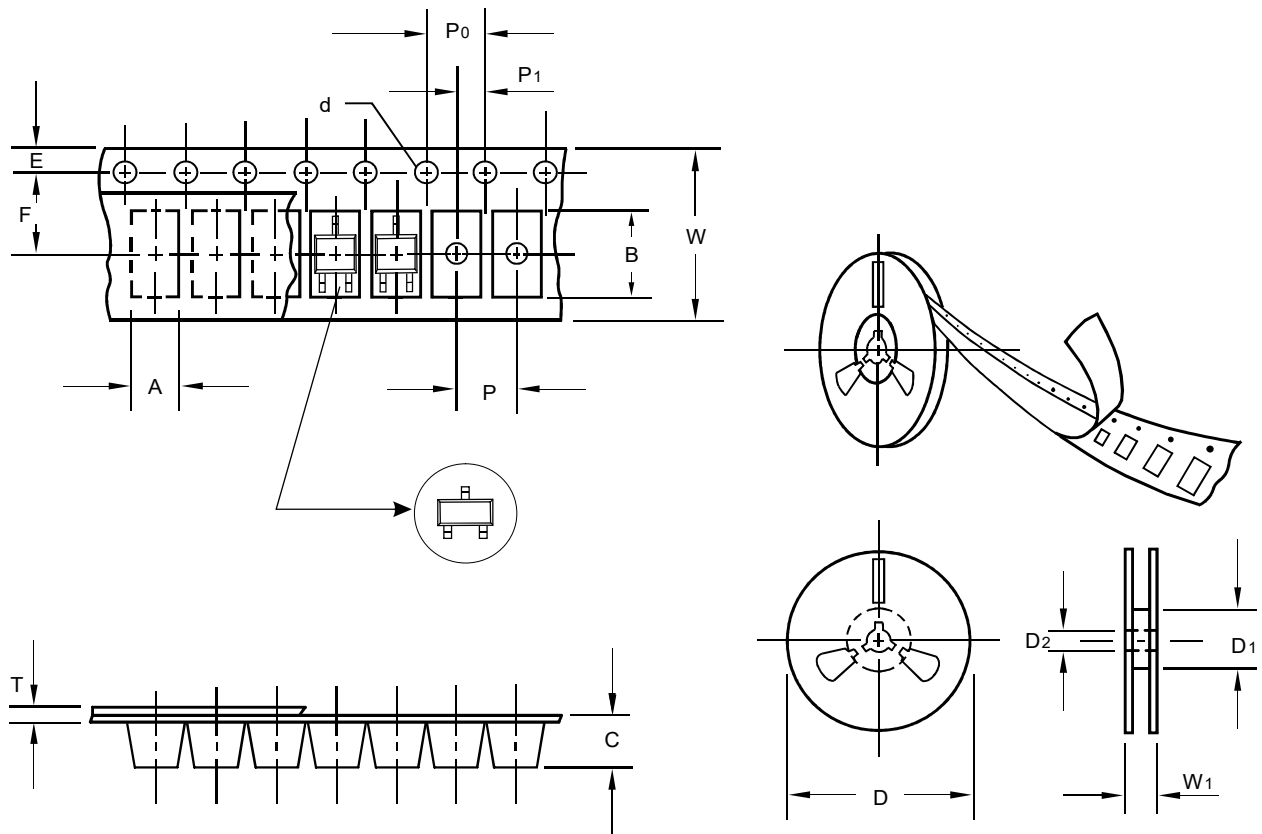
SOT-23



Dimensions in inches and (millimeters)

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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-23
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	55.00
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W1	1.0	12.0

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

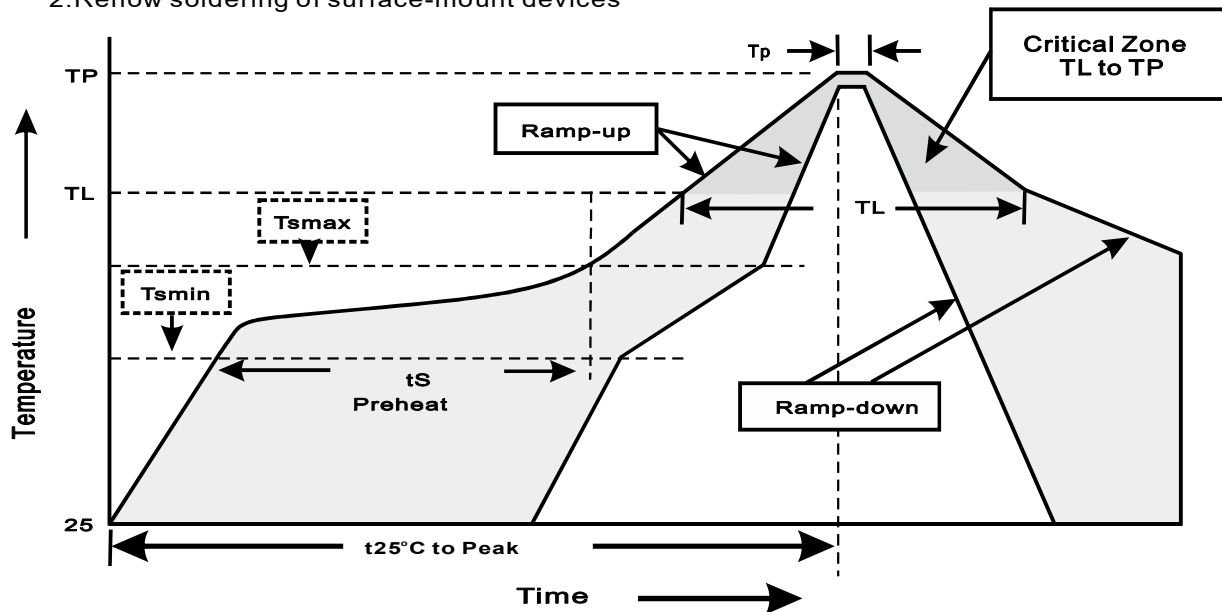
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
SOT-23	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smmin}) -Temperature Max(T _{smmax}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smmax} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _p)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes