

FMOS2312K

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FMOS2312K

20V N-Channel Enhancement Mode MOSFET

Features

- $R_{DS(ON)} \leq 25m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 33m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Rugged and reliable.
- ESD Protected 2KV.
- Lead-free parts meet RoHS requirements
- Suffix "-H" indicates Halogen-free part, ex. FMOS2312K-H

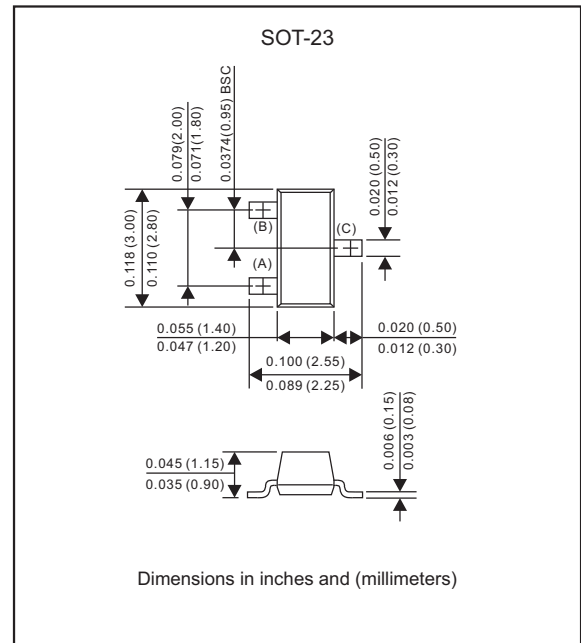
Applications

- Power management in note book
- Portable equipment
- Battery powered system
- Load switch
- DSC

Mechanical data

- Epoxy: UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-23
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.008 gram

Package outline



Maximum ratings (AT $T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	Limit	UNIT
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	± 12	V
Continuous drain current (Note 1)	I_D	5.5	A
Pulsed drain current (Note 2)	I_{DM}	22	A
Drain-source diode forward current (Note1)	I_S	1.7	A
Power dissipation (Note 1)	P_D	$T_A = 25^\circ C$ 1.25 $T_A = 75^\circ C$ 0.75	W
Operation junction temperature range	T_J	-55 to +150	$^\circ C$
Storage temperature range	T_{STG}	-55 to +150	$^\circ C$
Junction-to-ambient (Note1)	$R_{\theta JA}$	100	$^\circ C/W$

Note:

1. The device mounted on FR-4 board, $t \leq 0sec$.
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
3. Pulse width limited by maximum junction temperature.

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Electrical characteristics (At $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Static (Note 1)						
Drain-source breakdown voltage	$V_{GS} = 0V, I_D = 250\mu A$	B_{VDS}	20			V
Zero gate voltage drain current	$V_{DS} = 16V, V_{GS} = 0V$	I_{DSS}			1.0	μA
Gate-body leakage current	$V_{GS} = \pm 12V, V_{DS} = 0$	I_{GSS}			± 10	μA
Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(th)}$	0.6	0.8	1.0	V
Drain-source on-state resistance	$V_{GS} = 4.5V, I_D = 5.4A$ $V_{GS} = 2.5V, I_D = 4.3A$	$R_{DS(ON)}$		20 26	25 33	$m\Omega$
Diode forward voltage	$I_S = 1.5A, V_{GS} = 0V$	V_{SD}		0.7	1.2	V
Forward transconductance	$V_{DS} = 10V, I_D = 5A$	g_{fs}		18.5		S
Dynamic (Note 2)						
Total gate charge	$V_{DS} = 12V, V_{GS} = 4.5V, I_D = 3A$	Q_g		5.0		nC
Gate-source charge		Q_{gs}		2.6		
Gate-drain charge		Q_{gd}		1.6		
Input capacitance	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz$	C_{iss}		333		pF
Output capacitance		C_{oss}		121		
Reverse transfer capacitance		C_{rss}		34		
Turn-on delay time	$V_{DD} = 10V, R_L = 5\Omega$ $V_{GEN} = 4.5V, R_G = 6\Omega$ $I_D = 2A$	$t_{d(on)}$		360		ns
Turn-on rise time		t_r		836		
Turn-off delay time		$t_{d(off)}$		3920		
Turn-off fall time		t_f		2120		

Note:

1. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.

Rating and characteristic curves (FMOS2312K)

Fig-1. Output Characteristics

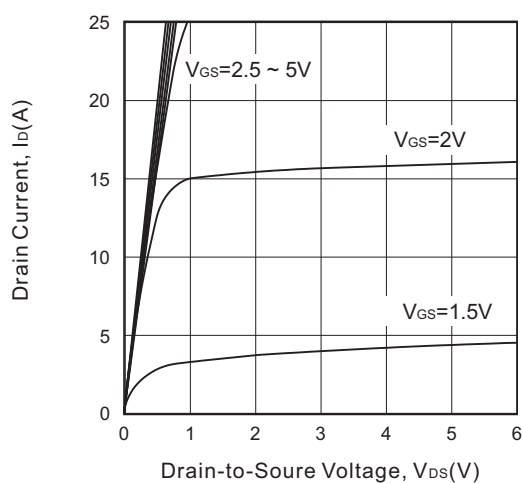


Fig-2. Transfer Characteristics

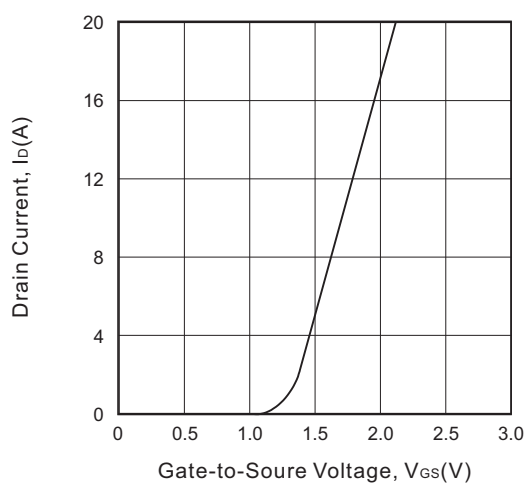


Fig-3. Breakdown Voltage Variation with Temperature

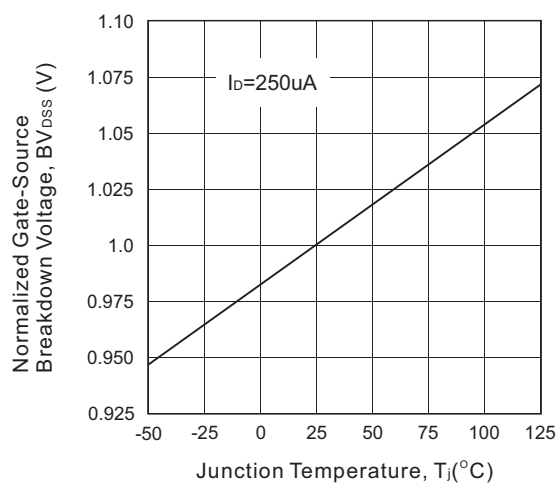


Fig-4. On-Resistance Variation With Temperature

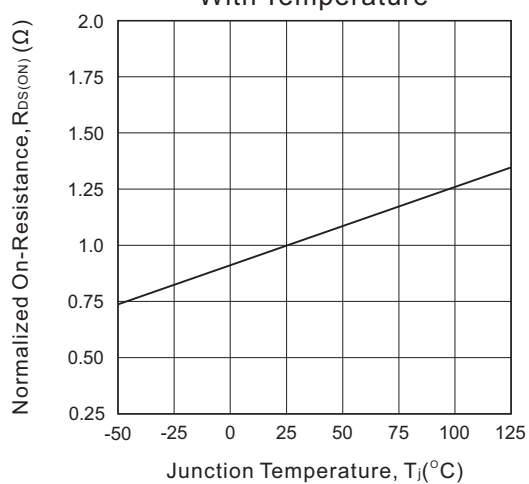


Fig-5. Gate Threshold Variation with Temperature

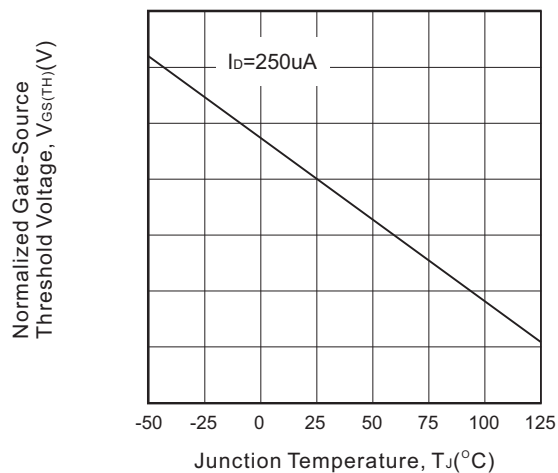
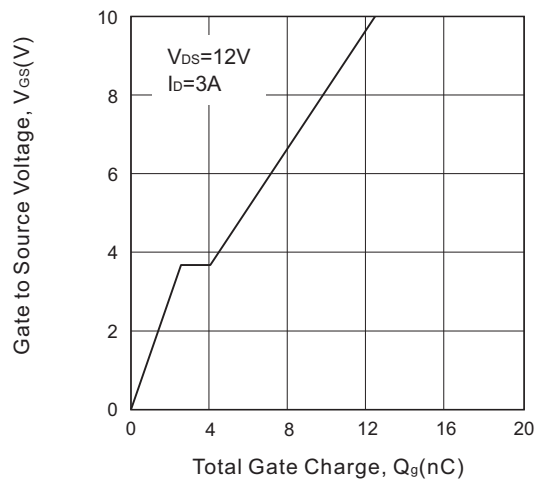


Fig-6. Gate Charge



Rating and characteristic curves (FMOS2312K)

Fig-7. Maximum Safe Operating Area

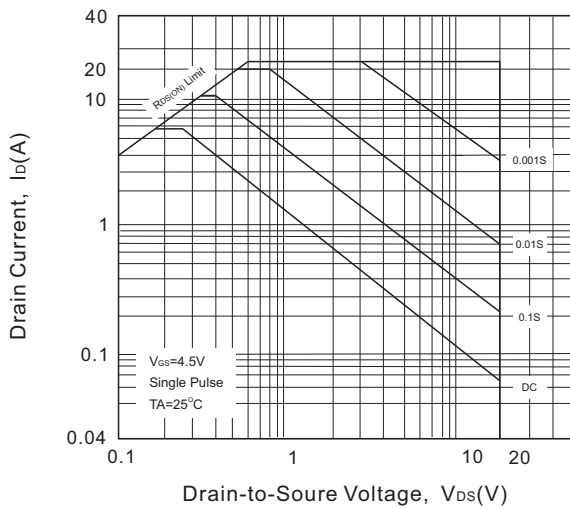


Fig-8. Body Diode Forward Voltage Variation with Source Current

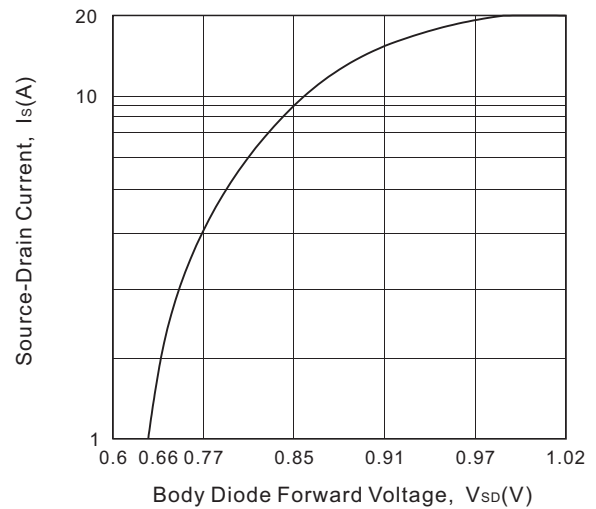


Fig-9. Switching Test Circuit and Switching Waveforms

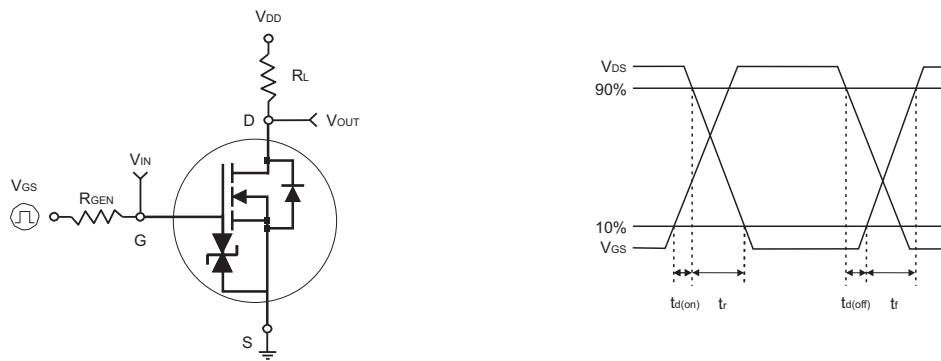
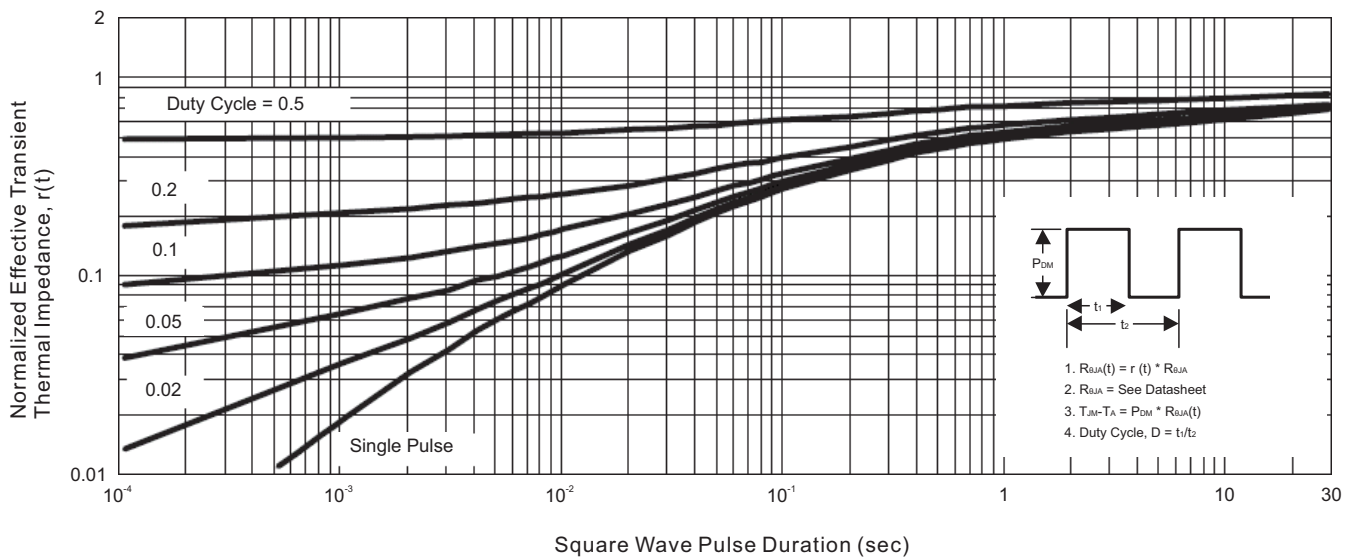
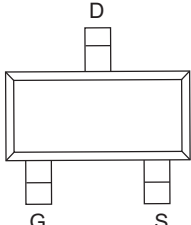
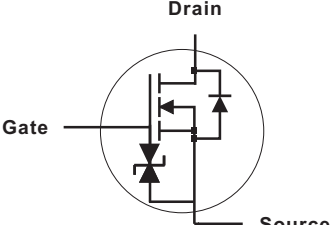


Fig-10. Normalized thermal Transient Impedance Curve



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Pinning information

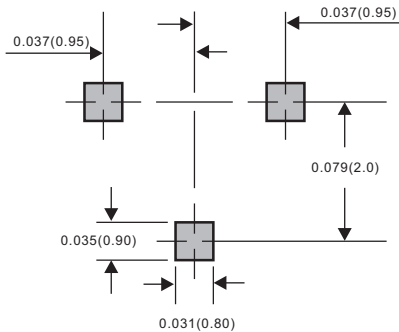
Pin	Simplified outline	Symbol
PinD Drain PinG Gate PinS Source		

Marking

Type number	Marking code
FMOS2312K	2622E

Suggested solder pad layout

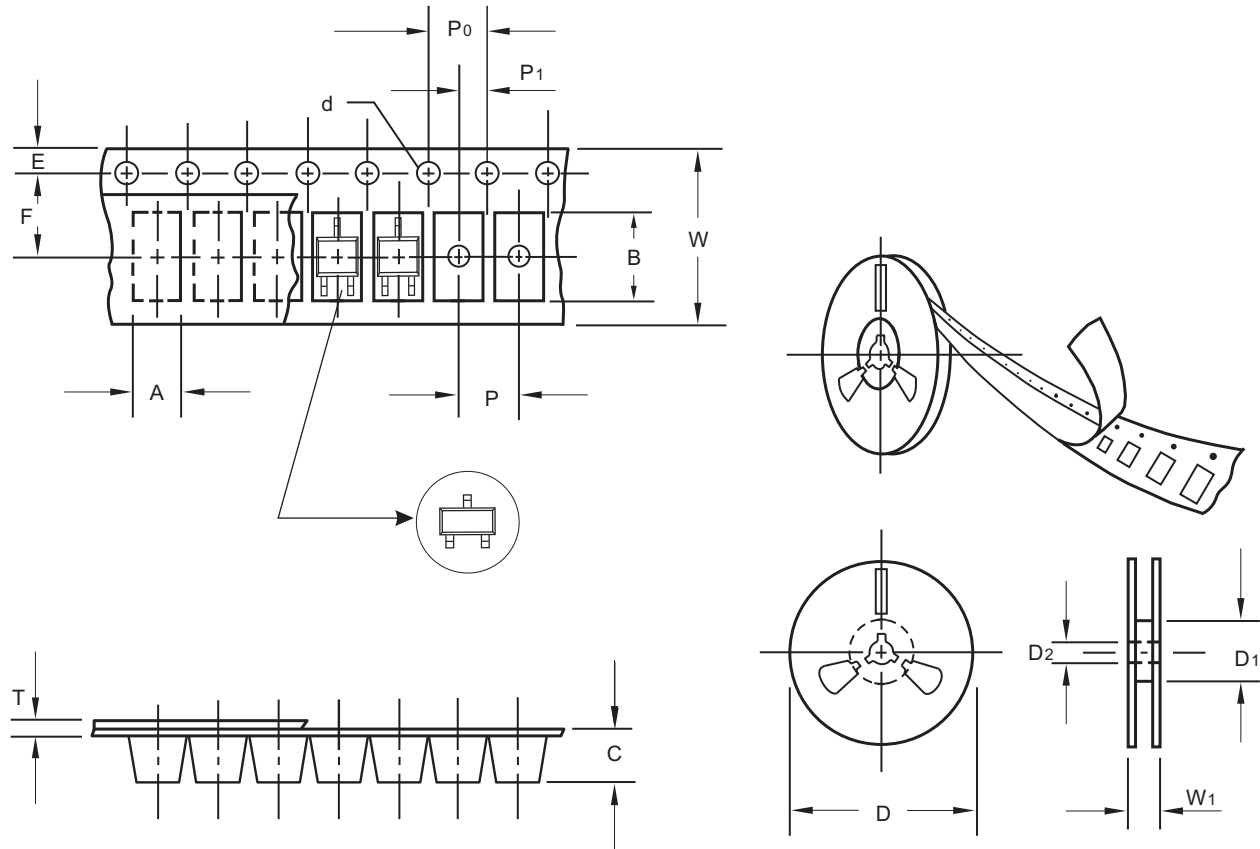
SOT-23



Dimensions in inches and (millimeters)

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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-23
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	55.00
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W1	1.0	12.0

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

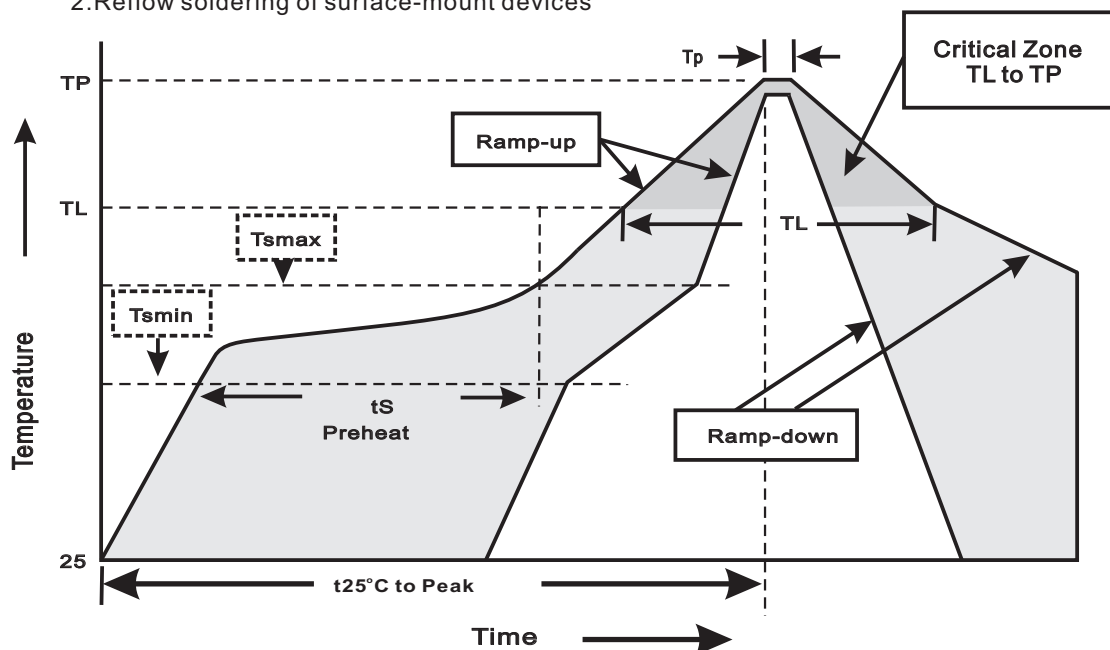
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-23	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000	11.6

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	$<3^{\circ}\text{C}/\text{sec}$
Preheat -Temperature Min(T_{smin}) -Temperature Max(T_{smax}) -Time(min to max)(t_s)	150°C 200°C 60~120sec
T_{smax} to T_L -Ramp-upRate	$<3^{\circ}\text{C}/\text{sec}$
Time maintained above: -Temperature(T_L) -Time(t_L)	217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	$<6^{\circ}\text{C}/\text{sec}$
Time 25°C to Peak Temperature	$<6\text{minutes}$