

FMOS0098N02E

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FMOS0098N02E

0.98A 20V N-Channel Enhancement Mode MOSFET ESD Protection

Features

- $V_{DS} = 20V$, $I_D = 0.98A$.
- $R_{DS(ON)} < 230m\Omega$ @ $V_{GS}=4.5V$, $I_D=0.55A$.
- $R_{DS(ON)} < 330m\Omega$ @ $V_{GS}=2.5V$, $I_D=0.45A$.
- $R_{DS(ON)} < 550m\Omega$ @ $V_{GS}=1.8V$, $I_D=0.35A$.
- Reliable and rugged.
- ESD protection.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen-free part, ex.FMOS0098N02E-H.

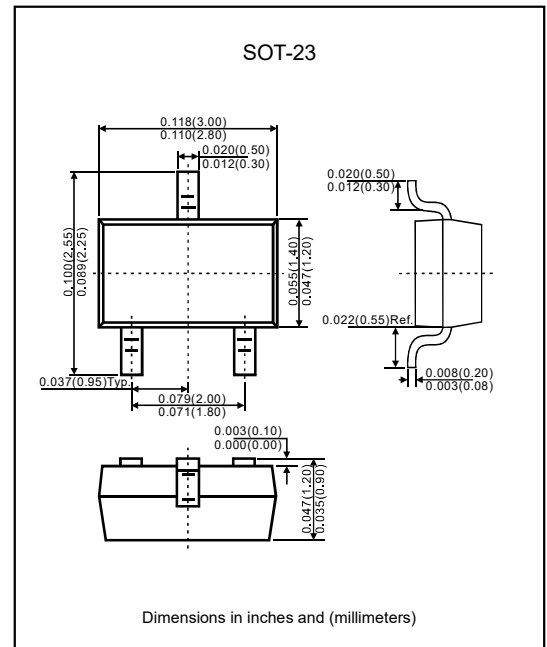
Applications

- Power management in DC/DC converters.
- Power load switch.
- Notebook battery management.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, SOT-23.
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026.
- Mounting Position : Any.

Package outline



Maximum ratings ($T_J=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	± 12	V
Continuous drain current (Note 1)	I_D	($T_A=25^\circ C$)	0.98
		($T_A=70^\circ C$)	0.78
Pulse drain current tested (Note 1)	I_{DM}	1.8	A
Power dissipation	P_D	($T_A=25^\circ C$)	0.36
		($T_A=70^\circ C$)	0.23
Thermal resistance, junction to ambient (Note 3) (steady state)	$R_{\theta JA}$	350	$^\circ C/W$
Operating Junction temperature	T_J	+150	$^\circ C$
Storage temperature range	T_{STG}	-55 to +150	$^\circ C$

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Electrical characteristics (At $T_j=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Off characteristics						
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
Drain-source leakage current	I_{DSS}	$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=\pm 12\text{V}$, $V_{DS}=0\text{V}$			± 10	μA
On characteristics						
Gate threshold voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.5	0.75	1	V
Forward transconductance	g_{FS}	$V_{DS}=5\text{V}$, $I_D=0.55\text{A}$		1.8		S
Static drain-source on-resistance (Note 4)	$R_{DS(ON)}$	$V_{GS}=4.5\text{V}$, $I_D=0.55\text{A}$		190	230	m Ω
		$V_{GS}=2.5\text{V}$, $I_D=0.45\text{A}$		255	330	
		$V_{GS}=1.8\text{V}$, $I_D=0.35\text{A}$		365	550	
Dynamic Parameters (Note 5)						
Gate resistance	R_G	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1.0\text{MHz}$		198		Ω
Input capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=10\text{V}$, $f=1.0\text{MHz}$		41		pF
Output capacitance	C_{OSS}			17		
Reverse transfer capacitance	C_{rSS}			10		
Switching parameters						
Total gate charge	Q_g	$V_{GS}=2.5\text{V}$, $V_{DS}=10\text{V}$, $I_D=1\text{A}$, $V_T=0.8\text{V}$		0.54		nC
				1		
				0.3		
Gate to source charge	Q_{gs}	$V_{GS}=4.5\text{V}$, $V_{DS}=10\text{V}$, $I_D=1\text{A}$, $V_T=0.8\text{V}$		0.3		ns
Gate to Drain charge	Q_{gd}			0.1		
Turn-on delay time	$t_{d(on)}$		$V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=2\text{A}$, $R_G=6\Omega$		1.2	
Rise time	t_r			24.7		
Turn-off delay time	$t_{d(off)}$			13.6		
Fall time	t_f			14.8		
Source-drain diode ratings and characteristics						
Reverse recovery time	t_{rr}	$I_F=1\text{A}$, $V_R=10\text{V}$, $dI_F/dt=100\text{A}/\mu\text{s}$		9.2		ns
Reverse recovery charge	Q_{rr}			0.8		nC
Drain - source diode forward voltage (Note 4)	V_{SD}	$V_{GS}=0\text{V}$, $I_{SD}=1\text{A}$		0.85	1.1	V

Note: 1. Max. current is limited by bonding wire.

2. UIS tested and pulse width are limited by maximum junction temperature 150°C .

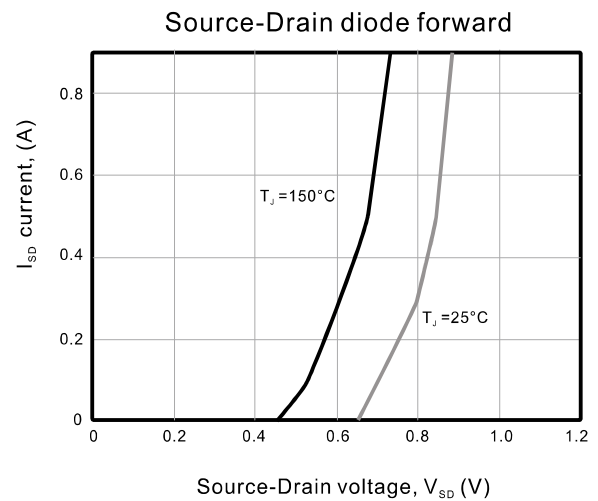
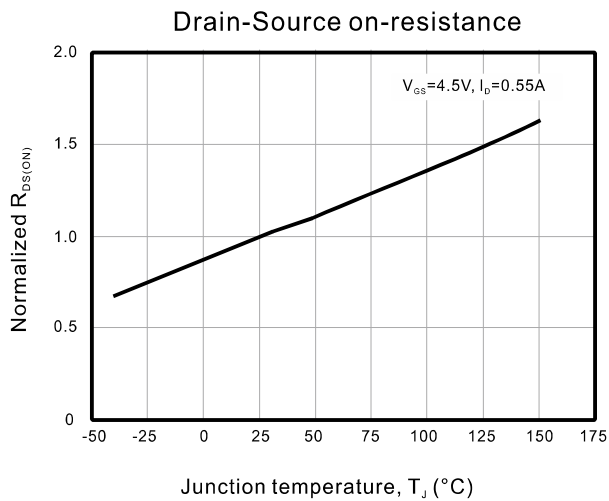
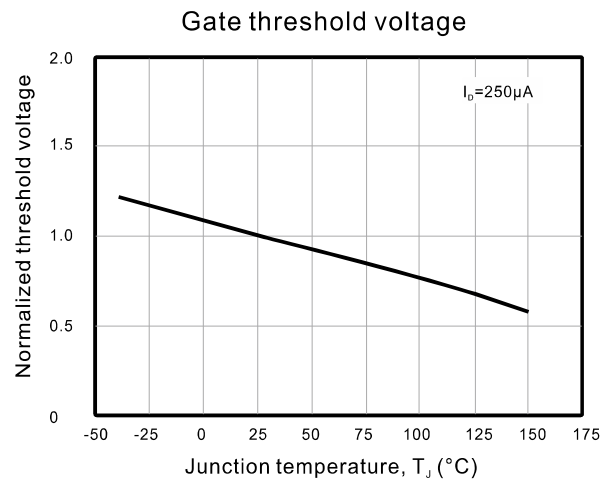
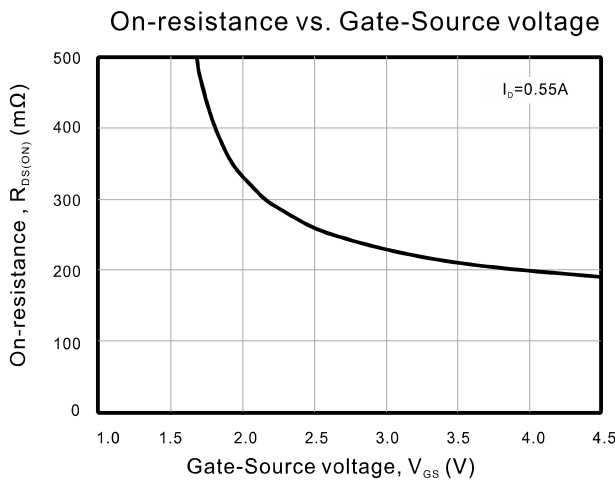
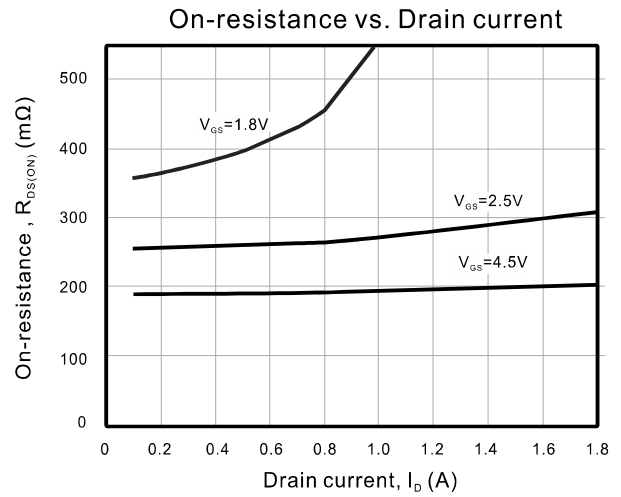
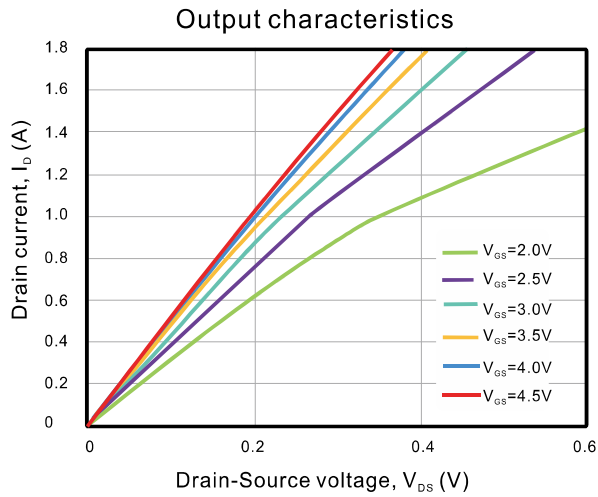
3. Surface mounted on 1in^2 FR-4 board with 1oz.

4. Pulse test (pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$).

5. Guaranteed by design, not subject to production testing.

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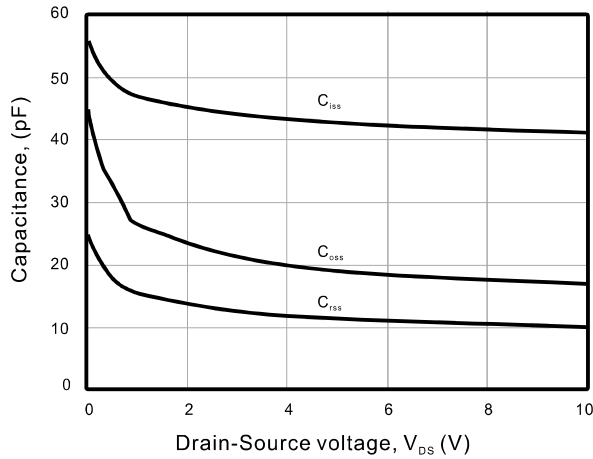
Rating and characteristic curves



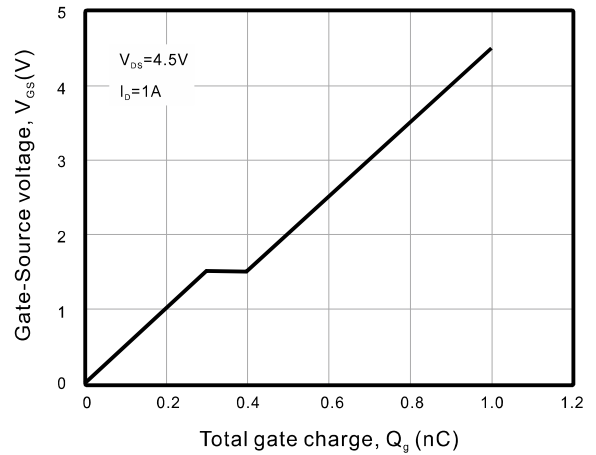
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Rating and characteristic curves

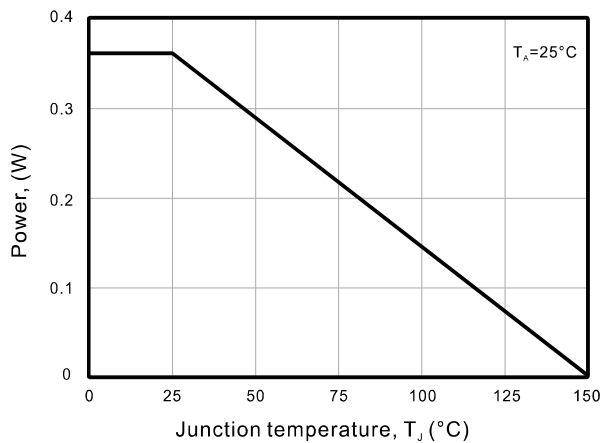
Capacitance



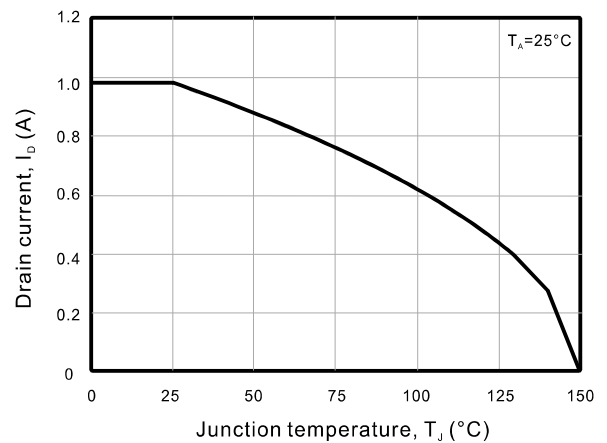
Gate charge characteristics



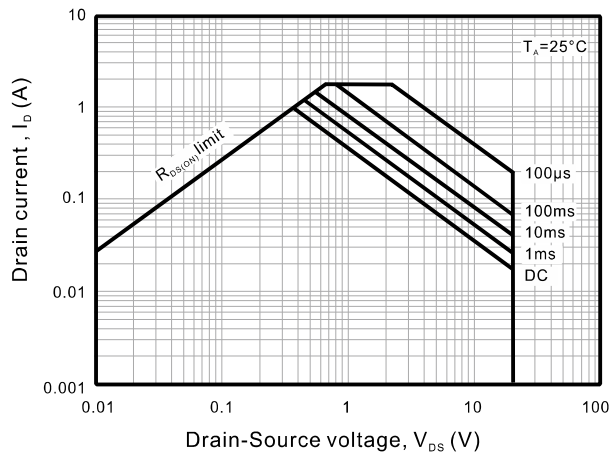
Power dissipation



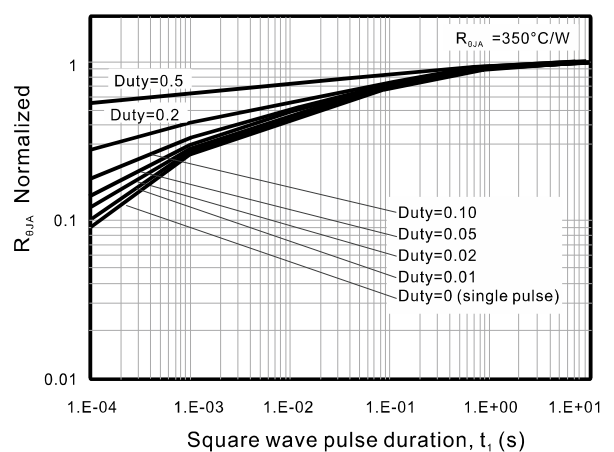
Drain current



Safe operating area

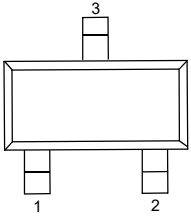
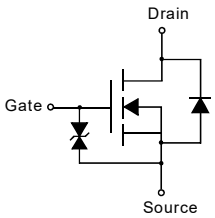


R_{θJA} transient thermal impedance



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Pinning information

Pin	Simplified outline	Symbol
Pin1 Gate Pin2 Source Pin3 Drain		

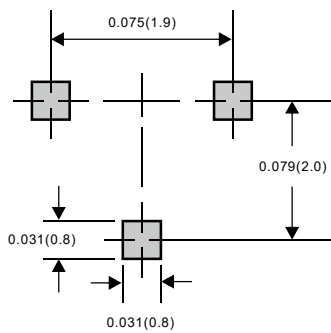
Marking

Type number	Marking code
FMOS0098N02E	06YWS

*06 : fixed code.
 YWS: Wafer lot code.
 Y: Year
 W: Weekly
 S: Sequence

Suggested solder pad layout

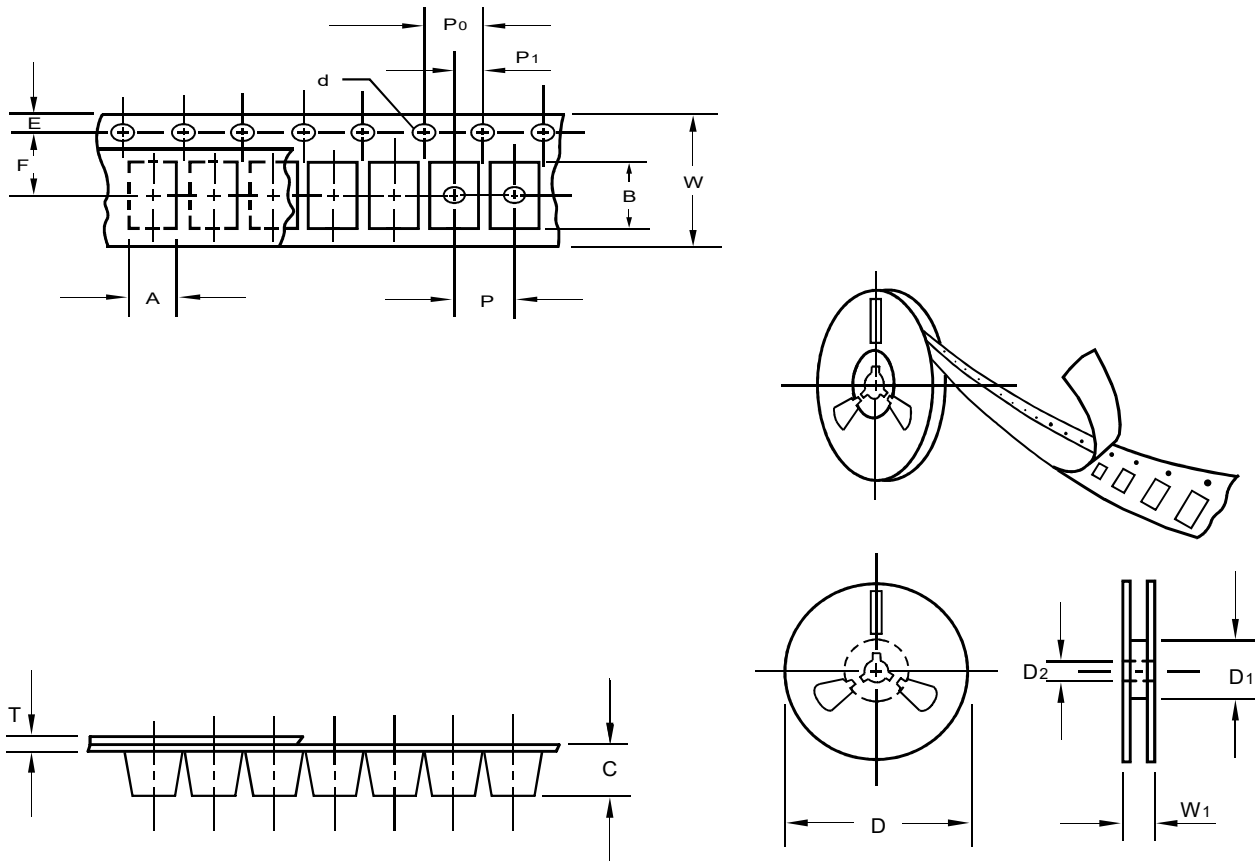
SOT-23



Dimensions in inches and (millimeters)

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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-23
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	54.40
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W1	1.0	11.40

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

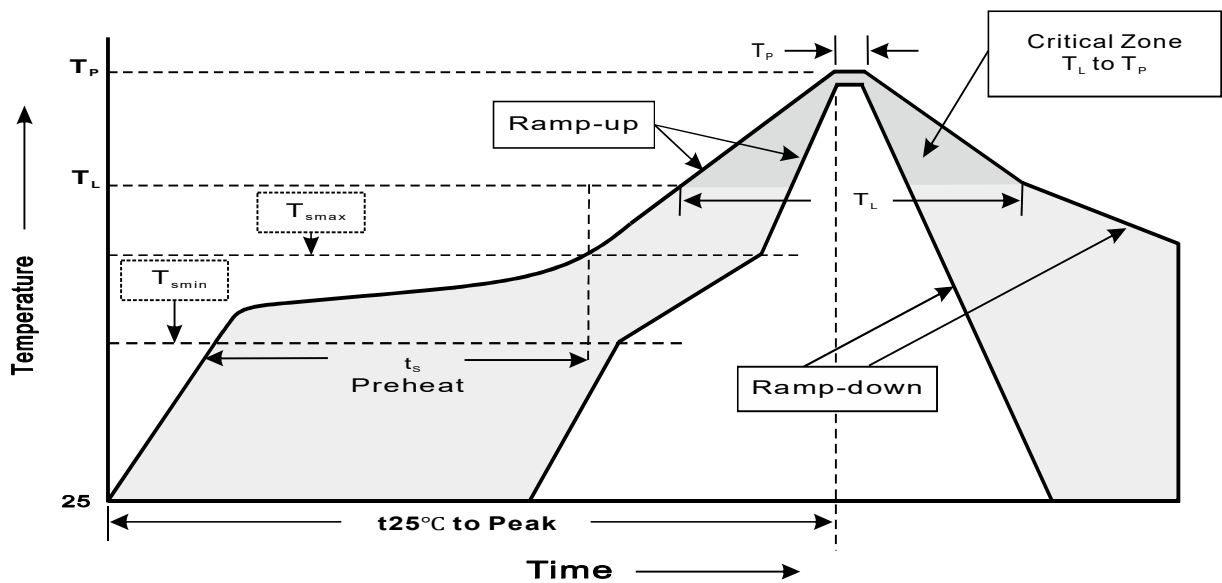
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	REEL DIA, (m/m)	CARTON (pcs)
SOT-23	7"	3,000	4.0	30,000	178	240,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile feature	Soldering Condition
Average ramp-up rate (T_L to T_p)	< 3°C/sec
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (min to max) (t_s)	150°C 200°C 60 ~ 120sec
T_{smax} to T_L -Ramp-up rate	< 3°C/sec
Time maintained above: -Temperature (T_L) -Time(T_L)	217°C 60 ~ 260 sec
Peak Temperature(T_p)	255°C -0/+5°C
Time within 5°C of actual peak Temperature(T_p)	10 ~ 30sec
Ramp-down rate	< 6°C/sec
Time 25°C to peak temperature	< 6 minutes