FMLDC0610A3V3ATH

List

FMLDC0610A3V3ATH

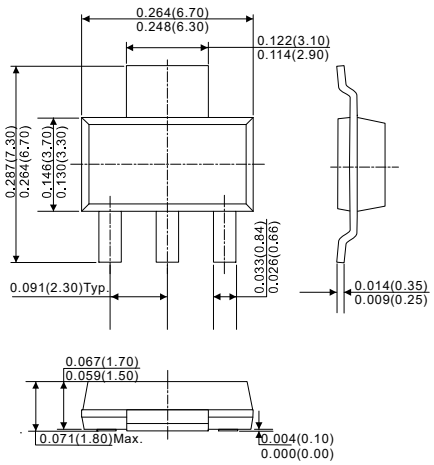
1300mA Low Voltage Difference CMOS Voltage Regulators

Features

- Guaranteed Output Current: 1.0A(Typ.)
- Input voltage range : 1.6V ~ 6.0V.
- Output voltage : 0.9V ~ 4.0V .
- High Accuracy : ±2%(Typ).
- Low Quiescent current : 70μA (Typ).
- Dropout voltage : 320mV @1.0A (V_{OUT} = 3.3V Typ).
- High PSRR : 70dB@10KHz.
- Excellent Line Regulation:0.02%/V.
- Build in Current Limiter and Thermal Protection.
- Lead-free parts meet RoHS requirements.

Package Outline

SOT-223



Applications

- CD/DVD-ROM, CD/RW.
- Wireless devices.
- Battery charger, battery-powered systems.
- Portable instrumentations.
- PC peripherals.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, SOT-223.
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026.
- Weight : Approximated 205mg.

Maximum ratings (T_{OPT}=25℃, unless otherwise note)

Parameter	Symbol	Ratings	Unit
Input voltage (Note 2)	V_{IN}	-0.3~7.0	V
Output current (Note 2)	I_{OUT}	1300	mA
Output voltage (Note 2)	V_{OUT}	-0.3~V_{IN}+0.3	V
Power dissipation (Note 3)	P_D	1.0	W
Thermal resistance, junction to ambient	$R_{\theta JA}$	102.6	℃/W
Thermal resistance, junction to case	$R_{\theta JC}$	18.6	℃/W
Ambient temperature range	T_A	-40 to +85	℃
Junction temperature range (Note 3)	T_J	-40 to +85	℃
Storage temperature	T_{STG}	+125	℃
Soldering temperature and time (10s)	T_{Solder}	+260	℃

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Electrical characteristics

(V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=4.7μF, T_A=25℃,unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input voltage	V_{IN}			1.6		6.0	V
Output voltage	V_{OUT}	T_J= 25°C, I_{OUT} = 100mA		-2		2	%
Output Current	I_{OUT}			1000	1300		mA
Quiescent current	I_Q	I_{OUT}=0mA			70	140	μA
Dropout voltage (note 8)	V_{DO}	I_{OUT}=300mA			90		mV
		I_{OUT}=1000mA			320		
Line regulation (note 9)	LNR	I_{OUT} = 100mA, V_{OUT} +1V to 6.0V,			0.02	0.2	%/V
Load regulation	ΔV_{LOAD}	V_{IN}= V_{OUT} +1V, I_{OUT} = 1 mA to1.0A			30		mV
Output voltage temperature characteristics (note 10)	TR	I_{OUT} = 10mA, T_A= -40 to 85℃			50		ppm/℃
Supply current	I_{SS}	I_{OUT}=0			70	140	μA
Short current	I_{short}	V_{OUT} =GND			120		mA
Standby current	I_{STBY}	V_{EN}=GND			0.1	1.0	μA
EN logic low voltage	V_{ENH}			1.5		V_{IN}	V
	V_{ENL}					0.3	V
Ripple suppression ratio	PSRR	I_{OUT} = 100mA	f = 10Hz		70		dB
			f = 1kHz		75		
EN logic voltage	V_{ENH}			1.5		V_{IN}	V
	V_{ENL}					0.3	V
Auto discharge resistance	$R_{discharge}$	V_{IN}=5V, V_{OUT}=3.0V, EN=GND			100		Ω
Thermal shutdown	T_{SD}				150		℃
Thermal shutdown hysteresis	ΔT_{SD}				30		℃

Note :

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) Refer to Thermal Information for details.

(4) It is necessary to ensure that the operating junction temperature of the device does not exceed the rated value of the recommended operating conditions when using the device for design.

(5) ESD testing is conducted in accordance with the relevant specifications formulated by the Joint Electronic Equipment Engineering Commission (JEDEC). The human body model (HBM) electrostatic discharge test is based on the JESD22-114D test standard, using a 100pF capacitor and discharging to each pin of the device through a resistance of 1.5kΩ. The electrostatic discharge test in mechanical model (MM) is based on the JESD22-115-A test standard and uses a 200pF capacitor to discharge directly to each pin of the device.

(6) Thermal metric is measured in still air with TA = 25°C and installed on a 1 in2 FR-4 board covered with 2 ounces of copper.

(7) Typical numbers are at 25°C and represent the most likely norm.

(8) Test the difference of output voltage and input voltage when input voltage is decreased gradually till output voltage equals to 98% of V_{OUT} Normal.

(9) The line regulation is calculated by the following formula :

Where, ΔV_{OUT} is the variation of the output voltage, ΔV_{IN} is the variation of the input voltage.

$$LNR = \frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$$

(10) The output voltage temperature characteristics (TR) is calculated by the following formula:

Where, ΔVOUT is the variation of the output voltage, ΔT is the variation of the ambient temperature.

$$TR = \frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T}$$

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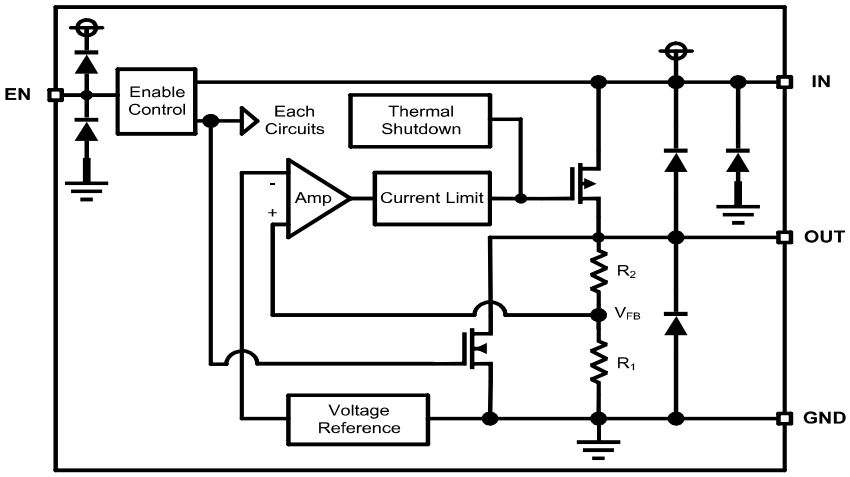
Detailed Description

1. Description

The FMLDC0610A3V3ATH is a group of positive voltage regulators manufactured by CMOS technologies with high ripple rejection, ultra fast transient response and low dropout voltage, and can provide large output current even if the input and output voltage difference is small. FMLDC0610A3V3AAH consists of a high precision voltag ereference, an error correction circuit and a current limiting output driver. Therefore, this product is very suitable for the following equipment application scenarios: industrial applications, battery power supply ,wireless communication and so on.

2. Functional block diagram



The internal feedback resistors R1 and R2 form a voltage divider circuit to compare the V_{FB} input error amplifier with the reference voltage. The internal regulator tube (PMOS) will control its conduction degree through the grid voltage provided by the error amplifier output, which will make the output voltage VOUT not affected by temperature changes or input voltage changes to a certain extent, thus maintaining the stability of the device output voltage.

3. Power Supply Input

When the input voltage is lower than the rated range of the data sheet, the device will lose the regulation function of stabilizing the output voltage, that is, it is unable to maintain the output voltage within the rated range. At this time, compared with normal operation, the quiescent current of the device may exceed the rated range, and the transient response performance may be seriously degraded. When the input voltage is higher than the rated range of the data sheet, the device may cause irreversible damage or failure due to exceeding the maximum rated range of electrical stress. For the rated input voltage of the device, see Recommended Operating Conditions and Dropout Voltage.

4. Output Current

When the circuit design is appropriate, the FMLDC0610A series can reach the maximum load capacity of at least 1A. According to the power dissipation of the package and the effective connection thermal resistance with the environment, selecting the appropriate package for the circuit design can make the device emit more heat energy.

5. Enable Control

The enable pin of the device (EN) is active at high level. When the voltage of the EN is greater than the EN logic high voltage ($V_{EN\,H}$), the device will be enabled and maintain the normal output. When the voltage of the EN is lower than the EN logic low voltage ($V_{EN\,L}$), the internal circuit of the device will be disabled and the output will be turned off, the device, the device will be in the standby mode until EN is turned to high level again. The $V_{EN\,H}$ and $V_{EN\,L}$ can be found in the Electrical Characteristics. Normal startup waveform and startup slope rate control can be ensured when the device starts from any low voltage lower than $V_{EN\,L}$, but the discharge time of output capacitor must be taken into account. EN can not be float, if EN is not required to control the output voltage independently, connect EN to IN.

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6. Dropout Voltage

Dropout voltage (V_{DO}) refers to the minimum voltage difference between input and output (V_{IN} - V_{OUT}) to make the device output voltage reach the rated range at rated current. When the dropout voltage condition required by the device is reached, the internal MOSFET will be fully turned on, at this time, the MOSFET is equivalent to a switch for regulation. The V_{DO} increases with the increase of load current. Since V_{IN} - V_{OUT} must be no less than the V_{DO}, the V_{DO} indirectly specifies the minimum input voltage of devices under different load current conditions. If the V_{IN} - V_{OUT} is less than the V_{DO}, the performance of the device may deteriorate (see Operation in Dropout Mode for details).

7. Auto-discharge Function

The device with enable control has an auto-discharge circuit. When the enable control is turned off, the device will be disabled. An internally integrated pull-down MOSFET (see Functional Block Diagram) will connect a resistor ($R_{Discharge}$) to the ground to release the charge in the output capacitor, thus closing the entire device circuit. The value of $R_{Discharge}$ can be found in the Electrical Characteristics. The discharge time of the output capacitor after the device is disabled is determined by the output capacitance (C_{OUT}) and load resistance (RL) in parallel with the $R_{Discharge}$. The time constant τ can be calculated by the following formula:

$$\tau = C \times R_{Discharge} \quad (R_L = 0)$$

$$\tau = C \times \left(\frac{R_L \times R_{Discharge}}{R_L + R_{Discharge}} \right) \quad (R_L \neq 0)$$

The output voltage after discharging through pull-down MOSFET can be calculated by the following formula:

$$V = V_{OUT} \times e^{-\frac{t}{\tau}}$$

$$t = \tau \times \ln\left(\frac{V}{V_{OUT}} \right)$$

8. Built-in Current Limit & Short Circuit Protection

The FMLDC0610A series has an internal current limiting circuit, which can protect the device by limiting the load current value in case of instantaneous high load current. When the current limiting is triggered, the output voltage is not regulated. If the out pin of the regulator is short circuited, the internal current limiting circuit will be triggered, the output current of the device will maintain at a relatively small value to protect the device. The typical value of short current I_{Short} can be found in Electrical Characteristics. The current limiting state will continue until the load current drops to the normal range.

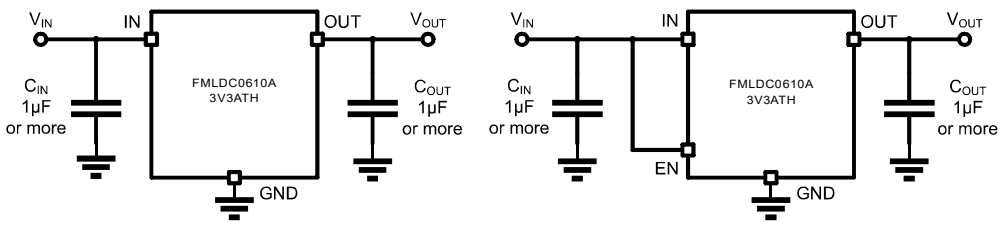
When the load current of the device is large, the device will generate more heat due to the increase of power consumption, which may cause the device to turn off its output due to the internal thermal shutdown protection before the current limit is triggered.

In order to ensure the normal operation of current limit, the inductance of input and load shall be minimized. Continuous operation under current limit is not recommended.

The current limit mode of the FMLDC0610A series is fold-back current limit. Please refer to the Fold-back Current Limit for more details.

Application and Implementation

1. Typical Application Circuit



2. Application Information

2.1. Selection of Bypass Capacitances(continued)

Output Capacitors (C_{OUT}): Recommended 1μF output ceramic capacitor to keep the device output stable, and the capacitor position should be as close to the device pin as possible. For FMLDC0610A series, the device needs an output capacitor to achieve loop stability. As with any regulator, a larger outputcapacitance reduces the peaks during a load transient but slows down the response time of the device. The proper capacitor can help to obtain better dynamic performance.

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Fold-back Current Limit

The FMLDC0610A series adopts the fold-back current limit. The following is some application information of the fold-back current limit. Current Limit Type: Current limit can impose certain restrictions on the current value provided by the device. Compared with the so called "brick-wall" current limiting mode, the significant difference of the fold-back current limit is that overload and short circuit are obviously different. Figure 9-1 and Figure 9-2 show the typical operating characteristics of these two current limiting mechanisms.

1. Operating characteristic curve R_1 represents the curve of linear resistance as load under normal working condition;
2. When the linear resistance as the load gradually decreases and causes the device to enter the overload state, the operating characteristic curve is shown in R_2;
3. When the linear resistance decreases to 0Ω, the device will enter the short-circuit state, and the operating characteristic curve is shown in R_3

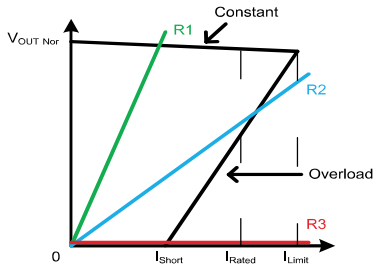


Figure 9-1. Fold-back Current Limit

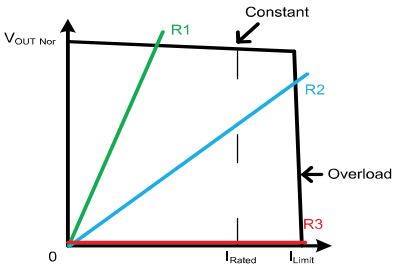


Figure 9-2. Brick-wall Current Limit

After entering the short circuit state, the short-circuit current of the "brick-wall" type current limiting mechanism is limited to I_{Limit}, and the reliability and stability of the voltage regulator may be affected due to the large amount of heat generated during the short circuit, while the I_{Short} of fold-back current limit in the short circuit state is far lower than I_{Limit}, which can reduce the heat energy generated due to power dissipation during the device short circuit. The fold-back current limit allows the device to limit the short circuit current to a small current value without losing the rated range of output current. This is very important if continuous short circuit faults need to be solved. The current limiting mechanism limits the maximum load current of the device, and the internal transmission transistor of the device will not move outside its safe operation area (SOA) during operation. See Recommended Continuous Operating Areas for details.

Usage and Precautions:

When using the voltage regulator with the fold-back current limit, it should be noted that the device cannot be started normally under certain loads because the short-circuit current of the fold-back current limit is obviously different from the maximum load current. As shown in the curves S_1 and S_2 in Figure 9-3, the nonlinear load S_1 is distributed in the range of the load curve region where the device can work, because the current provided by the device is always greater than the requirements of the load under all voltage conditions, the device can start normally, and the output will reach the ideal operating point P_1; The situation of nonlinear load S_2 is different, during actual startup, when the voltage and current are gradually rising, the output of S_2 will be limited at P_2, because the device cannot provide more current under the voltage at P_2, which will make the output stuck at the intersection and maintain at this level, and the device cannot reach the ideal operating point P_3 for normal startup.

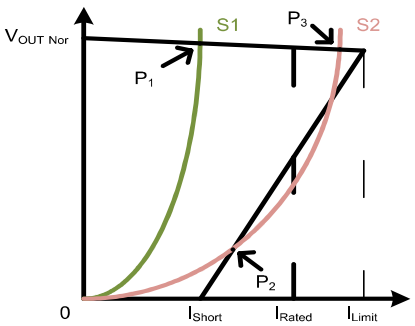


Figure 9-3. Nonlinear Load Example

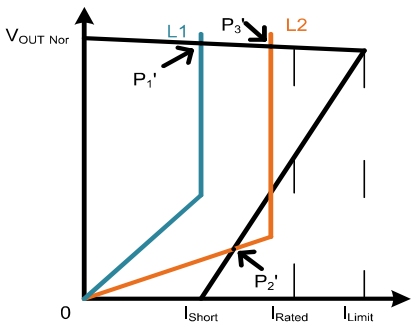


Figure 9-4. Active Load Profile

2.2. Transient Response

Transient response refers to the change of system output from initial state to stable state under the action of typical signal input. For LDO, the designer should pay attention to the possible impact of linear transient response and load transient response on the system: linear transient response refers to the transient response of output to change when the input voltage changes, while load transient response refers to the transient response of output to change when the output current changes. The specific phenomenon is that the output voltage of the device will have a short spike, especially when the input voltage or output current changes greatly in a short time. This change is not only related to the performance of the chip itself, but also related to the change of output current, change rate and output capacitance:

1. When the output current increases, the output voltage of the device will decrease to a certain extent, and the larger output current will provide a higher current discharge path for the output capacitor, which will affect the peak value generated by the transient spike and reduce the peak value;
2. The output current or input voltage changes relatively slowly, and the output change of the device is relatively small, affecting the spike caused by the change;
3. The use of large input and output capacitors can reduce the spike caused by transient response to a certain extent to improve the transient performance, but large output capacitors can also affect the response time of devices.

For the selection of bypass capacitance value, refer to the Section of Bypass Capacitances selection.

2.3. Operation in Dropout Mode

The FMLDC0610A series is internally integrated with a P-MOSFET to achieve low dropout voltage. The voltage difference between the input and the output (V_{IN} - V_{OUT}) of the device must not be lower than the corresponding dropout voltage (V_{DO}) to ensure that the output voltage tolerance is within the rated range of the data sheet. The dropout voltage will increase with the increase of load current. When the V_{IN} - V_{OUT} is less than the V_{DO}, the P-MOSFET inside the device is in a linear state, the resistance from the input pin to the output pin is equal to the resistance from the drain to the source of the P-MOSFET, and the device functions like a resistor. When operating in this state, the response time of the error amplifier inside the device will be limited, which will seriously degrade the transient performance of the device, when the external circuit has a transient change, the deviation of the output voltage will become larger than the normal operating state. In addition, the PSRR and noise performance of the device will be worse than that under normal operating conditions.

2.4.Recommended Continuous Operating Areas

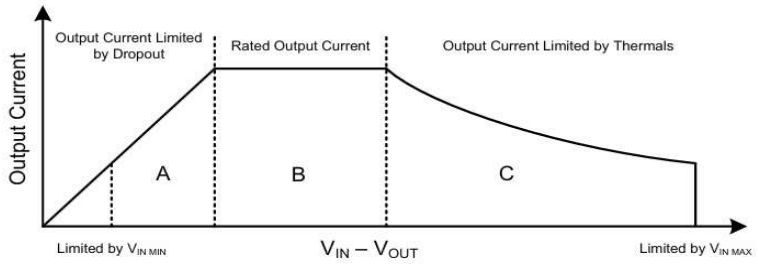
As an LDO, the working area of FMLDC0610Aseries is limited by dropout voltage, output current, junction temperature and input voltage under continuous working condition. The recommended areas for continuous operation are shown in Figure :

A. The LDO input and output voltage difference V_{IN} - V_{OUT} must meet the dropout voltage V_{DO} conditions. See Dropout Voltage for more details.

B. Rated output current range I_{rated}.

C.The actual junction temperature T_J of LDO shall not exceed the rated junction temperature. The product of voltage difference and current at both ends of LDO is power consumption, which determines the actual working junction temperature of LDO, so the curve is not linear.

In addition, the working area of FMLDC0610A series is limited by the rated V_{IN} MIN and V_{IN} MAX.



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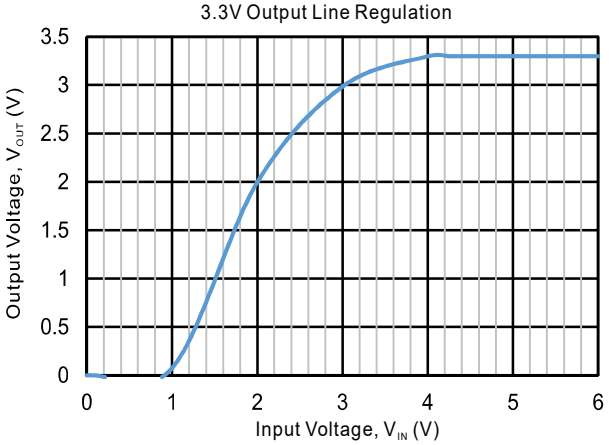
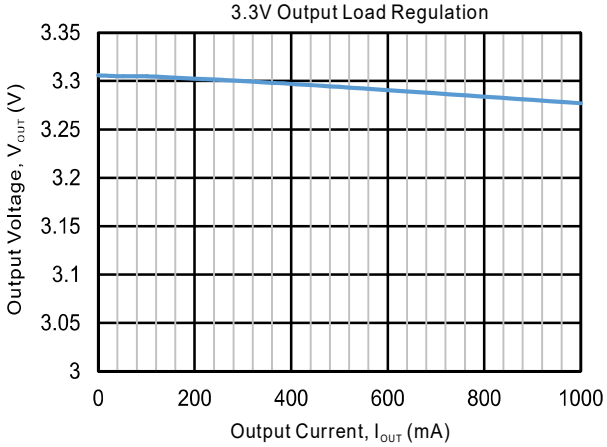
Rating and characteristic curves (V_{EN} = V_{IN}, C_{IN} = 1.0μF, C_{OUT} = 1.0μF, T_A = 25°C, unless otherwise specified)

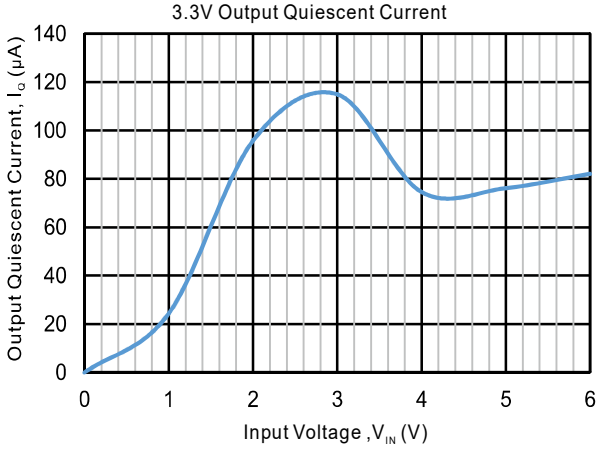
3.3V Output Line Regulation



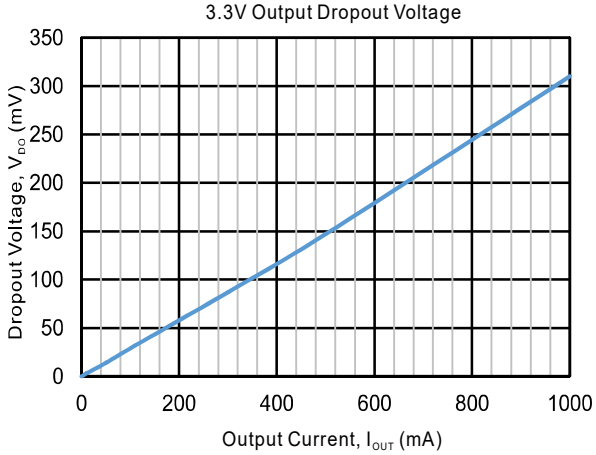
3.3V Output Load Regulation



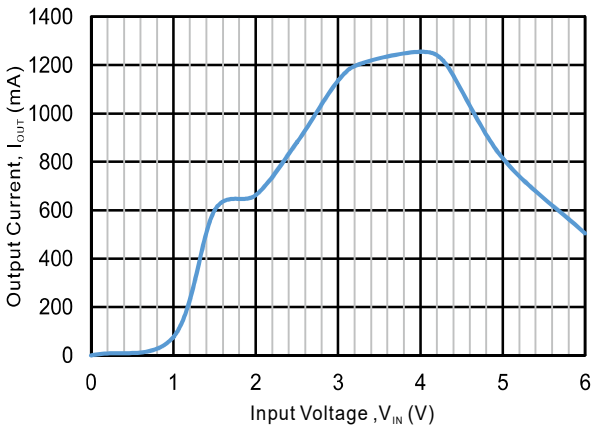
3.3V Output Quiescent Current



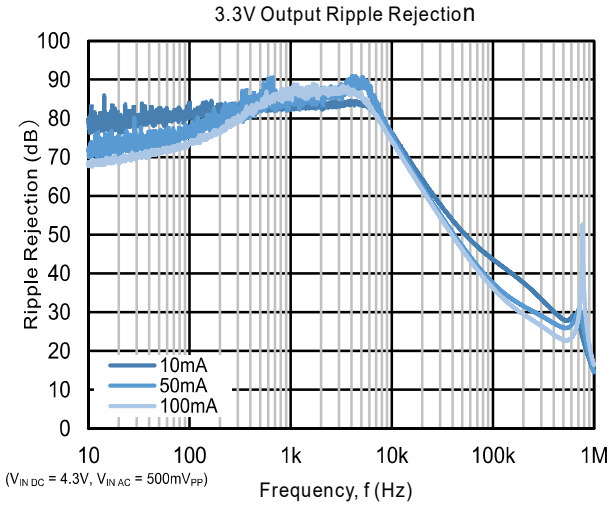
3.3V Output Dropout Voltage



3.3V Output Current Limit



3.3V Output Ripple Rejection



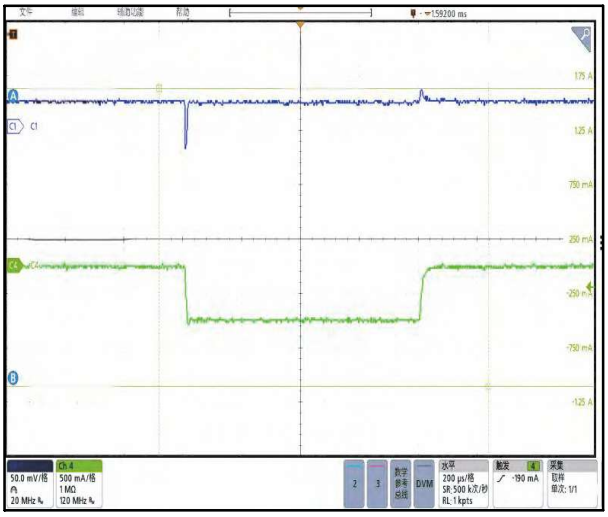
FMLDC0610A3V3ATH

Rating and characteristic curves (V_{EN} = V_{IN}, C_{IN} = 1.0μF, C_{OUT} = 1.0μF, T_A = 25°C, unless otherwise specified)

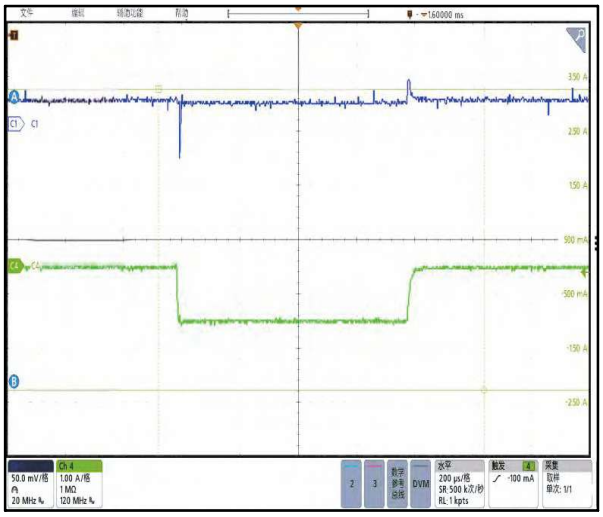
Load Transient

V_{OUT} = 3.3V, V_{IN} = V_{EN} = V_{OUT}+1V, CH2: V_{OUT}, CH4: I_{OUT}

I_{OUT}:1~500mA



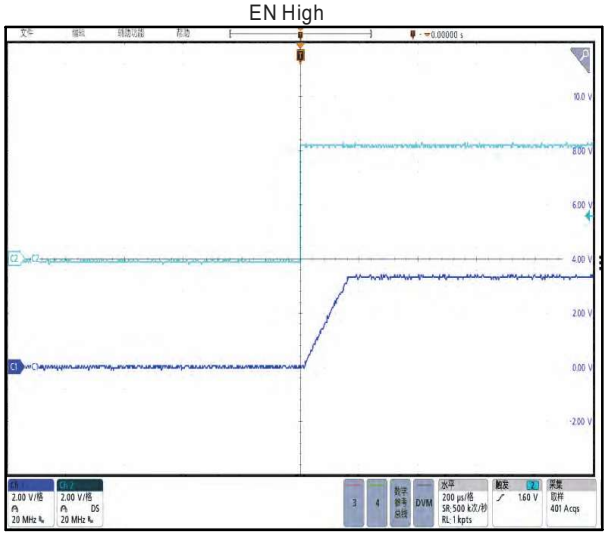
I_{OUT}:1~1000mA



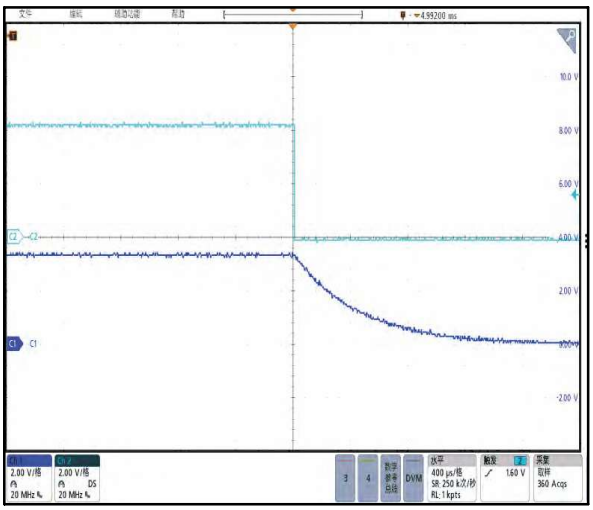
EN

V_{OUT} = 3.3V, V_{IN} = V_{OUT} +1V, V_{EN} = 0 ~ 4.3V, CH2: V_{EN}, CH1: V_{OUT}

EN High



EN Low



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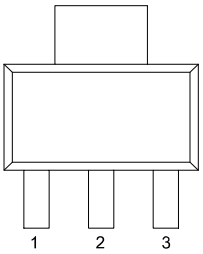
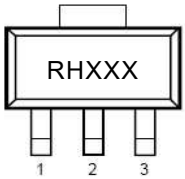
Pinning information

Pin	Simplified outline
Pin 1 V_{IN} Pin 2 V_{OUT} Pin 3 V_{SS}	

Marking

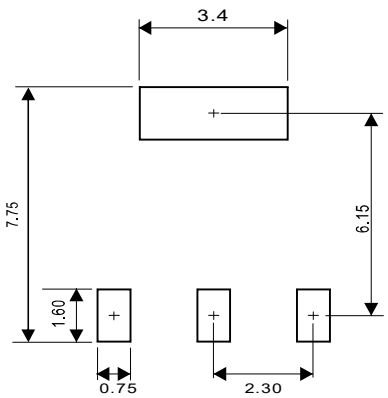


Marking code	Description
RH	FMLDC0610A3V3ATH
XX	Code, indicates weekly record information of wafer lot code
X	Code, special pin arrangement sequence. (blank): Normal

X : Represents any character.

Suggested solder pad layout

SOT-223



Note :
1. Controlling dimension : In millimeters.
2. General tolerance : ±0.05mm.
3. The pad layout is for reference purposes only.

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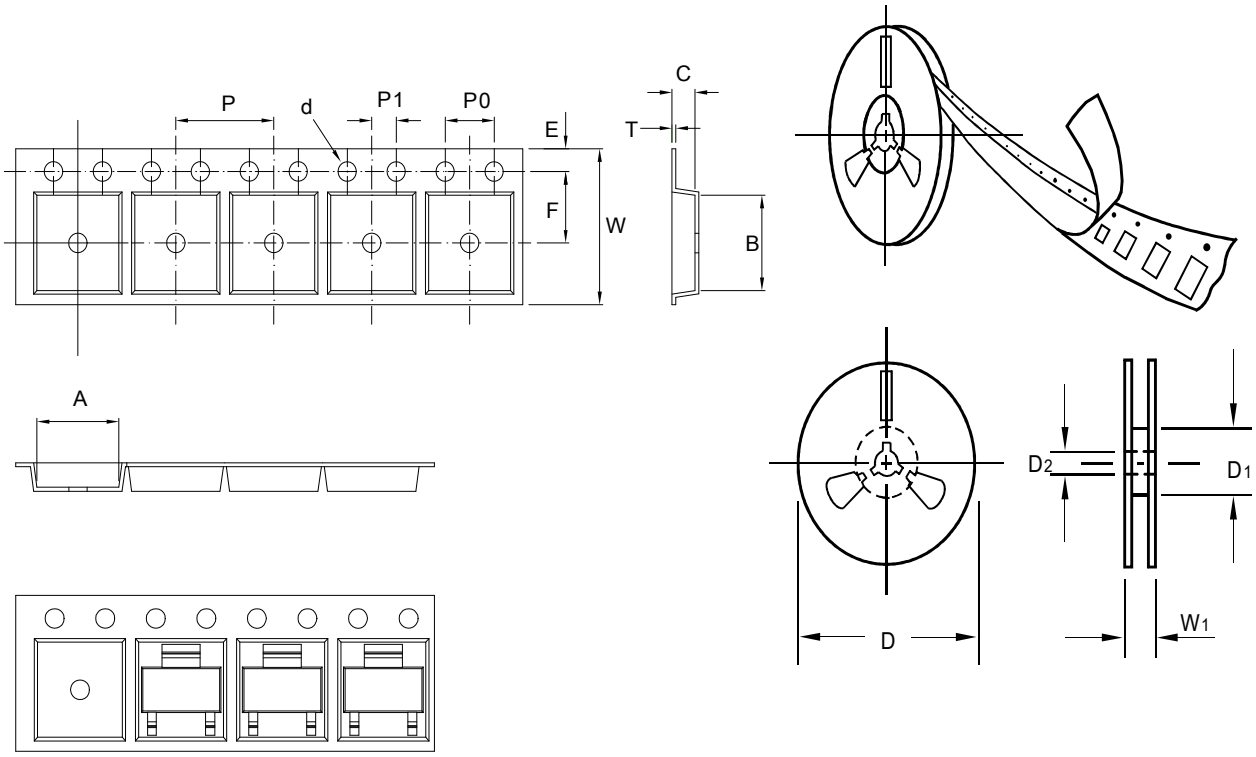
Packing information



Unit : mm

Item	Symbol	Tolerance	SOT-223
Carrier width	A	±0.1	6.90
Carrier length	B	±0.1	7.30
Carrier depth	C	±0.1	1.85
Sprocket hole	d	±0.1	1.50
13" Reel outside diameter	D	±1.0	330.0
13" Reel inner diameter	D1	±0.5	99.0
Feed hole diameter	D2	±0.3	13.1
Sprocket hole position	E	±0.1	1.75
Punch hole position	F	±0.1	5.50
Punch hole pitch	P	±0.1	8.00
Sprocket hole pitch	P0	±0.1	4.00
Embossment center	P1	±0.1	2.00
Over all tape thinkness	T	±0.1	0.25
Tape width	W	±0.5	12.00
Reel width	W1	±0.5	12.80

Note : Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

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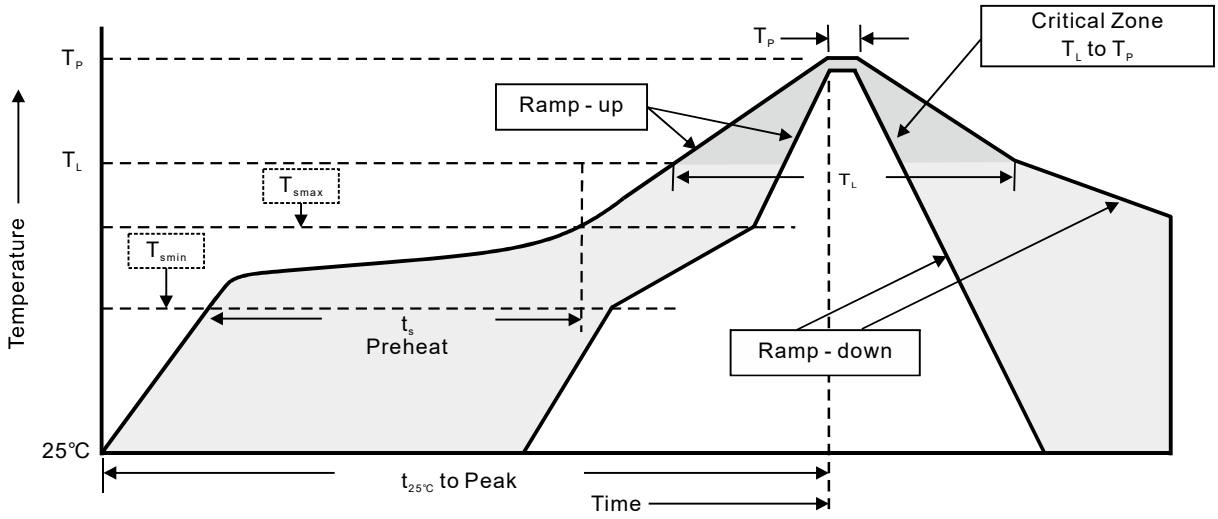
Reel packing

Package	Units (pcs)			Dimension (Unit : mm³)		
	Reel	Inner Box	Outer Box	Reel DIA,	Inner Box	Outer Box
SOT-223	2,500	5,000	25,000	330 (13")	340x 340 x 50	385 x 257 x 392

Suggested thermal profiles for soldering processes

1. Storage environment : Temperature = 5℃ ~ 40℃, Humidity = 55%, ±25%.
2. Reflow soldering of surface - Mount devices.



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_P)	< 3 ℃/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	 150℃ 200℃ 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	 < 3 ℃ / sec
Time maintained above : - Temperature (T_L) - Time (T_L)	 217℃ 60 ~ 260 sec
Peak temperature (T_P)	255 ℃ -0 / +5℃
Time with 5℃ of actual peak temperature (T_P)	10 ~ 30 sec
Ramp-down rate	< 6℃ / sec
Time 25℃ to peak temperature	< 6 minutes