FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

List

FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

1000mA Low Voltage Difference CMOS Voltage Regulators:

Features

- Input voltage range : 1.0V ~ 6.0V.
- Fixed output voltage : designed for 0.6V to 4.5V output.
- Output voltage tolerance : ±15mV for V_{OUT} <1.5V
  ±1% for V_{OUT}>1.5V .
- Dropout voltage : 310mV @1.0A (V_{OUT} = 3.3V).
- Power supply rejection ratio : 75dB@1KHz.
- Low output noise : 27×V_{OUT} μ V_{RMS} (10Hz ~ 100kHz).
- Integrated fault protection : Fold-back current limit, short-circuit protection.
- Lead-free parts meet RoHS requirements.

Applications

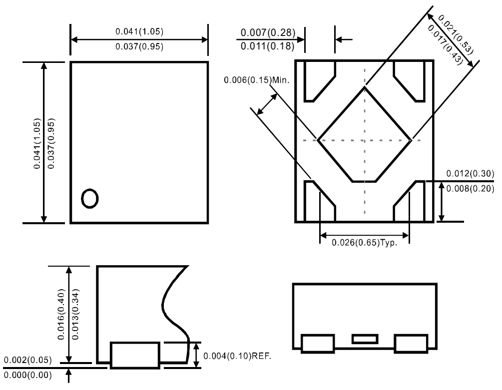
- Portable Consumer Equipments
- Radio Control Systems
- Laptop, Palm tops and PDAs.

Mechanical data

- Epoxy : UL94-V0 rated flame retardant.
- Case : T1010P4.
- Weight : Approximated 1.5mg.

Package outline

T1010P4



Dimensions in inches and (millimeters)

Maximum ratings (T_{OPT}=25°C, unless otherwise note)

Parameter	Symbol	Ratings	Unit
Input voltage (note 2)	V_{IN}	-0.3~7.0	v
Output current (Min.)	I_{OUT}	1000	mA
Power dissipation (note 3)	P_D	0.45	W
Electrostatic discharge (Note 4)	$V_{ESD\text{-}HBM}$	2	KV
Thermal resistance, junction to ambient	$R_{\theta JA}$	220.0	°C/W
Thermal resistance, junction to case	$R_{\theta JC}$	115.0	°C/W
Operating temperature range	T_{OPT}	-40 to +85	°C
Junction temperature range	T_J	+125	°C
Storage temperature	T_{STG}	+125	°C
Soldering temperature and time	T_{Solder}	+260	°C

Note :

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) Refer to Thermal Information for details.

(4) ESD testing is conducted in accordance with the relevant specifications formulated by the Joint Electronic Equipment Engineering Commission (JEDEC). The human body model (HBM) electrostatic discharge test is based on the JESD22-114D test standard, using a 100pF capacitor and discharging to each pin of the device through a resistance of 1.5kΩ. The electrostatic discharge test in mechanical model (MM) is based on the JESD22-A115-A test standard and uses a 200pF capacitor to discharge directly to each pin of the device.

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Electrical characteristics (V_{out} =3.3V, T_A=25°C, unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input voltage	V_{IN}			1.8		6	V
Output voltage (note 8)	V_{OUT}	I_{OUT}=1mA		-2		2	%
		(note9)		-1		1	
Dropout voltage (note10)	V_{DROP}	V_{OUT}<1.5V	I_{OUT}=100mA		400		mV
		V_{OUT}=1.5 to 2.0V			200		
		V_{OUT}>2.0V			110		
Output Current limit	$I_{OUT LIMIT}$	V_{OUT} = 0.5 × V_{OUT}(Normal), V_{IN} = 5.0V		350	550	750	mA
Quiescent current	I_{SS}	I_{OUT}=0mA			0.8	1.5	μA
Short current	I_{SHORT}	V_{OUT} short to GND			100		mA
Standby current	I_{STBY}	V_{EN}=GND				0.1	μA
Line regulation (note11)	ΔV_{LINE}	V_{IN} = V_{OUT} +1V to 6V, I_{OUT} = 10mA			0.05	0.3	%/V
Load regulation	ΔV_{LOAD}	V_{IN} = V_{OUT} +1V, I_{OUT} = 1 to 100mA			10		mV
EN logic low voltage	V_{ENH}	V_{IN} = V_{OUT} +1V		1.5		V_{IN}	V
	V_{ENL}	V_{IN} = V_{OUT} +1V				0.3	V
EN input current	I_{EN}	V_{EN}=0 to 5.5V				1	μA
Ripple suppression ratio	PSRR	I_{OUT} = 50mA	f = 100Hz		60		dB
			f = 1kHz		50		
			f = 10kHz		40		
			f = 100kHz		35		

Note：

(5)Typical numbers are at 25°C and represent the most likely norm.

(6)The effective output voltage range, which refers to the tolerance range that the output voltage may reach when the input voltage is equal to the output voltage plus 1V and the output current maintains a certain value.

(7)Products with ±1% output tolerance can be customized.

(8)Test the difference of output voltage and input voltage when input voltage is decreased gradually till output voltage equals to 98% of V_{OUT} Normal.

(9)The line regulation is calculated by the following formula:

$$LNR = \frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$$

where, ΔV_{OUT} is the variation of the output voltage, ΔV_{IN} is the variation of the input voltage.

(10) The output voltage temperature characteristics (T_R) is calculated by the following formula:

$$TR = \frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T}$$

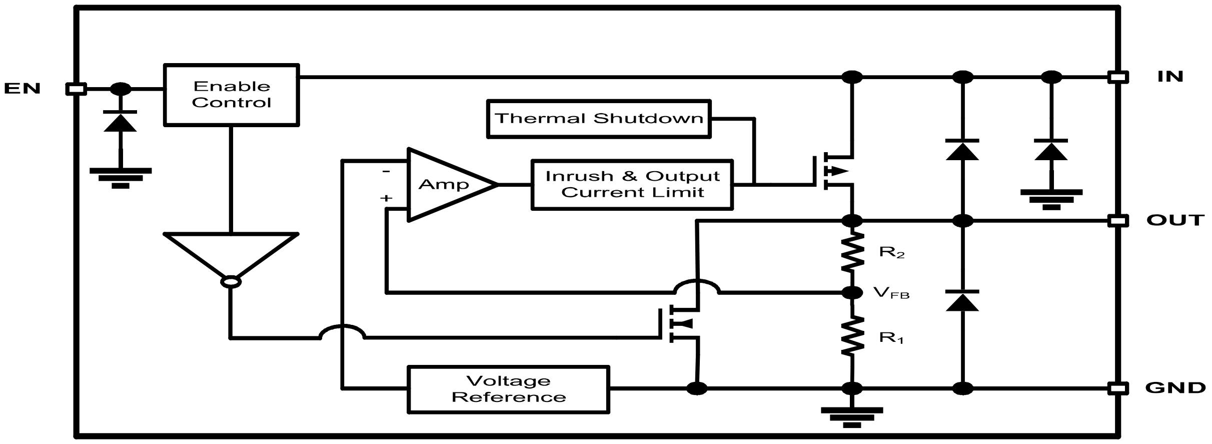
where, ΔV_{OUT} is the variation of the output voltage, ΔT is the variation of the ambient temperature.

Detailed Description

1. Description

The FMLDC0610A series is a group of 6V, low-power consumption, low-dropout linear regulators (LDOs). The FMLDC0610A series supports fixed voltage output from 0.6V to 4.5V, which enables it to use fewer external components to provide better accuracy. The FMLDC0610A series has low IQ performance and is internally integrated with current limiting, short-circuit protection and thermal shutdown protection, which makes it an ideal choice for battery power or line power applications.

2. Functional block diagram



The internal feedback resistors R_1 and R_2 form a voltage divider circuit to compare the V_{FB} input error amplifier with the reference voltage. The internal regulator tube (PMOS) will control its conduction degree through the grid voltage provided by the error amplifier output, which will make the output voltage V_{OUT} not affected by temperature changes or input voltage changes to a certain extent, thus maintaining the stability of the device output voltage.

3. Power Supply Input

When the input voltage is lower than the rated range of the data sheet, the device will lose the regulation function of stabilizing the output voltage, that is, it is unable to maintain the output voltage within the rated range. At this time, compared with normal operation, the quiescent current of the device may exceed the rated range, and the transient response performance may be seriously degraded.

When the input voltage is higher than the rated range of the data sheet, the device may cause irreversible damage or failure due to exceeding the maximum rated range of electrical stress.

For the rated input voltage of the device, see Recommended Operating Conditions.

4. Output Current

When the circuit design is appropriate, the FMLDC0610A series can reach the maximum load capacity of up to 1000mA. According to the power dissipation of the package and the effective connection thermal resistance with the environment, selecting the appropriate package for the circuit design can make the device emit more heat energy.

5. Enable Control

The enable pin of the device (EN) is active at high level. When the voltage of the EN is greater than the EN logic high voltage (VEN H), the device will be enabled and maintain the normal output. When the voltage of the EN is lower than the EN logic low voltage (VEN L), the internal circuit of the device will be disabled and the output will be turned off, the device, the device will be in the standby mode until EN is turned to high level again. The VEN H and VEN L can be found in the Electrical Characteristics.

Normal startup waveform and startup slope rate control can be ensured when the device starts from any low voltage lower than VEN L, but the discharge time of output capacitor must be taken into account. EN can not be float, if EN is not required to control the output voltage independently, connect EN to IN.

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6. Dropout Voltage

Dropout voltage (V_{DO}) refers to the minimum voltage difference between input and output (V_{IN} - V_{OUT}) to make the device output voltage reach the rated range at rated current. When the dropout voltage condition required by the device is reached, the internal MOSFET will be fully turned on, at this time, the MOSFET is equivalent to a switch for regulation. The V_{DO} increases with the increase of load current. Since V_{IN} - V_{OUT} must be no less than the V_{DO}, the V_{DO} indirectly specifies the minimum input voltage of devices under different load current conditions. If the V_{IN} - V_{OUT} is less than the V_{DO}, the performance of the device may deteriorate (see Operation in Dropout Mode for details).

7. Auto-discharge Function

The device has an automatic discharge mechanism. When the enabling control of the device is turned off, a pull down MOSFET inside the device (see Functional Block Diagram) will connect a resistor to the ground to release the charge in the output capacitor, so as to turn off the whole device circuit. Refer to Electrical Characteristics for the value of automatic discharge resistance ($R_{discharge}$). Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

8. Built-in Current Limit & Short Circuit Protection

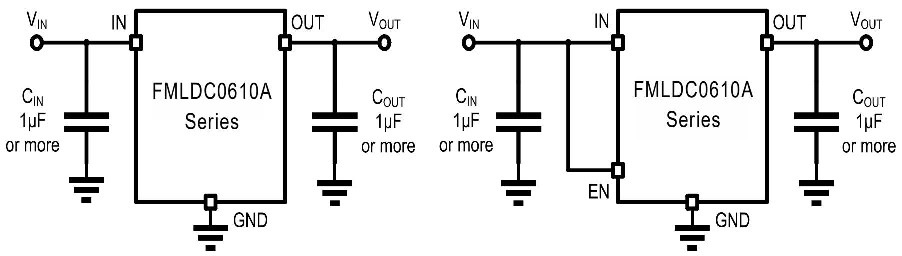
The FMLDC0610A series has an internal current limiting circuit, which can protect the device by limiting the load current value in case of instantaneous high load current. When the current limiting is triggered, the output voltage is not regulated. If the out pin of the regulator is short circuited, the internal current limiting circuit will be triggered, the output current of the device will maintain at a relatively small value to protect the device. The typical value of short current I_{Short} can be found in Electrical Characteristics. The current limiting state will continue until the load current drops to the normal range.

In order to ensure the normal operation of current limit, the inductance of input and load shall be minimized. Continuous operation under current limit is not recommended.

The current limit mode of the FMLDC0610A series is fold-back current limit. Using electronic load to test the starting characteristics may cause the device to fail to start normally.

Application and Implementation

1. Typical Application Circuit



2. Application Information

2.1. Selection of Bypass Capacitances

It is recommended to use 1μF input and output ceramic capacitors to keep the device stable, and the position of the capacitor should be as close to the pin of the chip as possible. For the FMLDC0610A series, the input capacitor is not necessary to maintain the output stability, but it can offset the reactive input source and improve the transient response, input ripple and PSRR performance of the device. It should be noted that although many types of capacitors can be used for input bypass, using ceramic capacitors for input filtering may cause problems. Due to the self resonance and high Q characteristics of some types of ceramic capacitors, under certain starting conditions, applying voltage steps to ceramic capacitors may lead to large current surges (such as directly connecting the input pin of LDO to the power supply), which may cause some energy stored in the parasitic inductance of the power lead. When the stored energy is transferred from these inductors to ceramic capacitors, large voltage spikes may occur in the circuit. These voltage spikes are easily twice the step amplitude of the input voltage, and are likely to bring potential risks to the normal operation and reliability of the device. Therefore, the selection of ceramic capacitors as input capacitors must be careful. Adding 3Ω resistors and X5R- type ceramic capacitors will minimize voltage transients during startup. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

2.2. Transient Response

Transient response refers to the change of system output from initial state to stable state under the action of typical signal input. For LDO, the designer should pay attention to the possible impact of linear transient response and load transient response on the system: linear transient response refers to the transient response of output to change when the input voltage changes, while load transient response refers to the transient response of output to change when the output current changes. The specific phenomenon is that the output voltage of the device will have a short spike, especially when the input voltage or output current changes greatly in a short time. This change is not only related to the performance of the chip itself, but also related to the change of output current, change rate and output capacitance:

1. When the output current increases, the output voltage of the device will decrease to a certain extent, and the larger output current will provide a higher current discharge path for the output capacitor, which will affect the peak value generated by the transient spike and reduce the peak value;
2. The output current or input voltage changes relatively slowly, and the output change of the device is relatively small, affecting the spike caused by the change;
3. The use of large input and output capacitors can reduce the spike caused by transient response to a certain extent to improve the transient performance, but large output capacitors can also affect the response time of devices.

For the selection of bypass capacitance value, refer to the Section of Bypass Capacitances selection.

2.3. Operation in Dropout Mode

The FMLDC0610A series is internally integrated with a P-MOSFET to achieve low dropout voltage. The voltage difference between the input and the output (V_{IN} - V_{OUT}) of the device must not be lower than the corresponding dropout voltage (V_{DO}) to ensure that the output voltage tolerance is within the rated range of the data sheet. The dropout voltage will increase with the increase of load current. When the V_{IN} - V_{OUT} is less than the V_{DO}, the P-MOSFET inside the device is in a linear state, the resistance from the input pin to the output pin is equal to the resistance from the drain to the source of the P-MOSFET, and the device functions like a resistor. When operating in this state, the response time of the error amplifier inside the device will be limited, which will seriously degrade the transient performance of the device, when the external circuit has a transient change, the deviation of the output voltage will become larger than the normal operating state. In addition, the PSRR and noise performance of the device will be worse than that under normal operating conditions.

2.4.Recommended Continuous Operating Areas

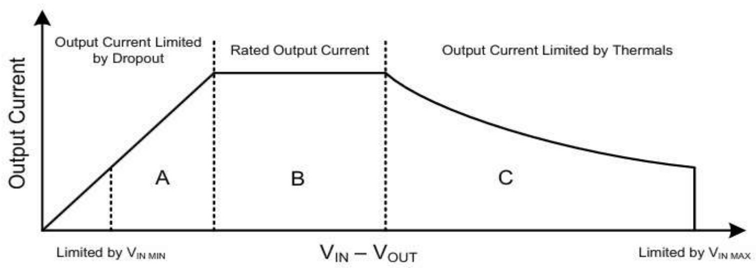
As an LDO, the working area of FMLDC0610A series is limited by dropout voltage, output current, junction temperature and input voltage under continuous working condition. The recommended areas for continuous operation are shown in Figure 9-5:

A. The LDO input and output voltage difference V_{IN} - V_{OUT} must meet the dropout voltage V_{DO} conditions. See Dropout Voltage for more details.

B. Rated output current range I_{rated}.

C. The actual junction temperature T_J of LDO shall not exceed the rated junction temperature. The product of voltage difference and current at both ends of LDO is power consumption, which determines the actual working junction temperature of LDO, so the curve is not linear.

In addition, the working area of FMLD6101A series is limited by the rated V_{IN} MIN and V_{IN} MAX.



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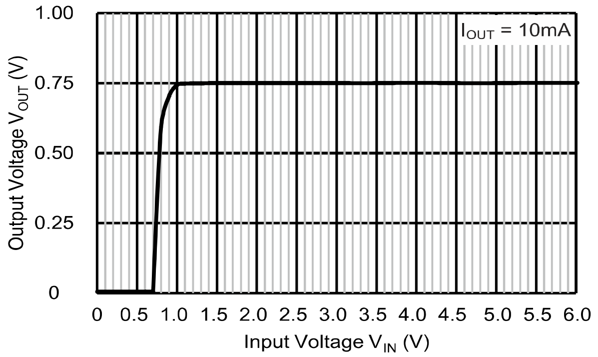
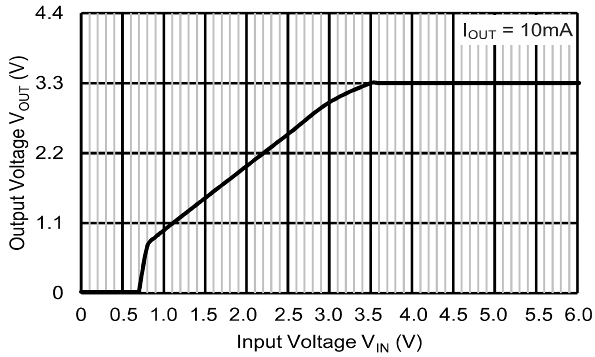
Rating and characteristic curves (C_{IN} = 1μF, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

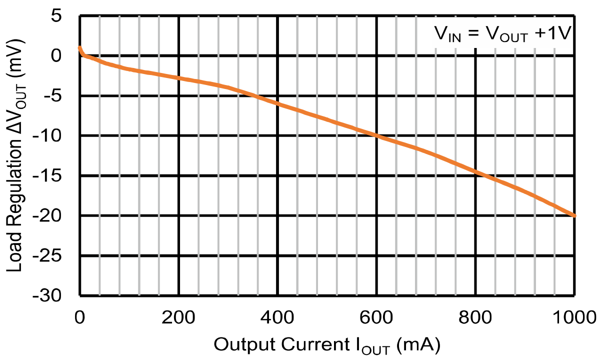
0.75V Output Line Regulation



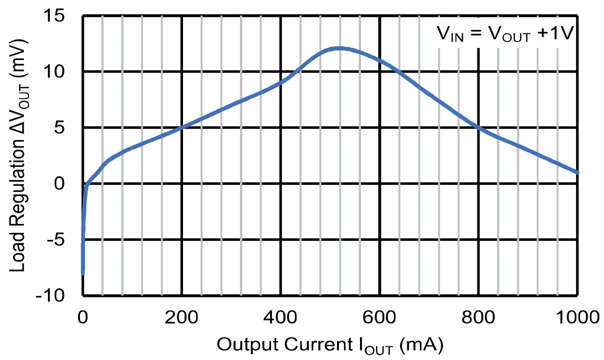
3.3V Output Line Regulation



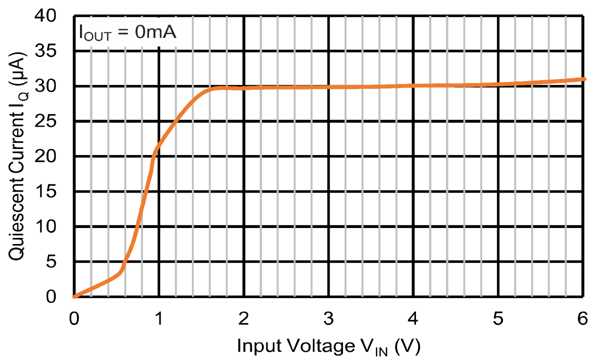
0.75V Output Load Regulation



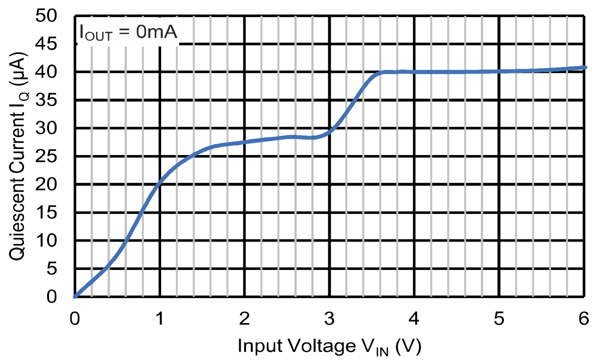
3.3V Output Load Regulation



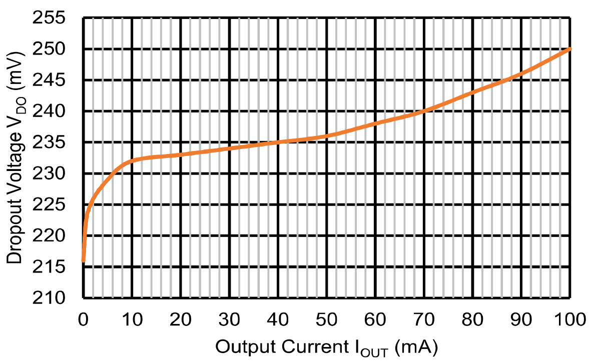
0.75V Output Quiescent Current



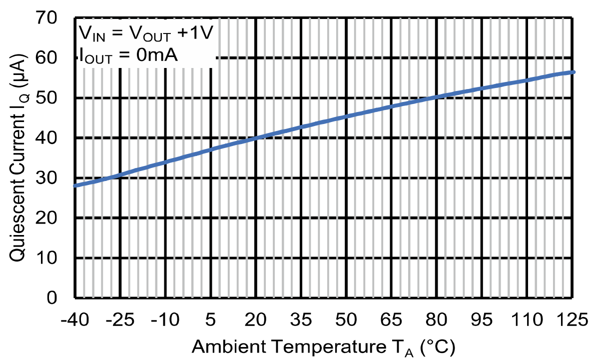
3.3V Output Quiescent Current



0.75V Output Dropout Voltage (100mA)



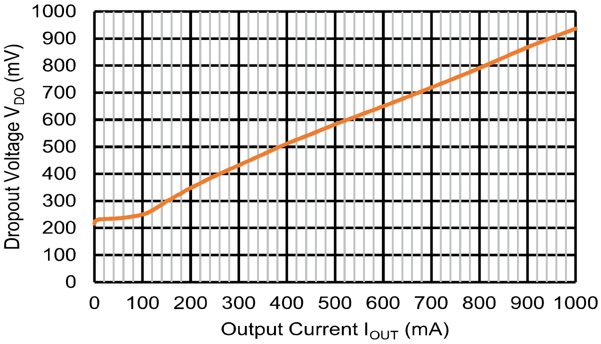
3.3V Output Quiescent Current



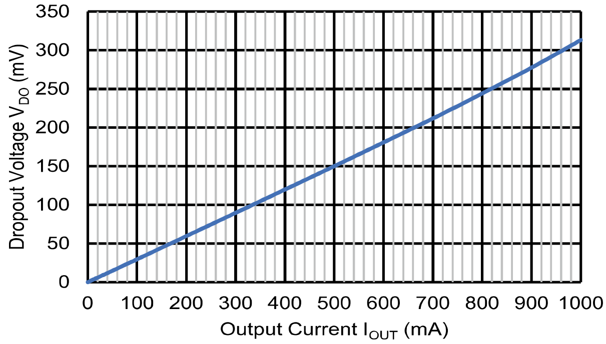
FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

Rating and characteristic curves (C_{IN} = 1μF, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

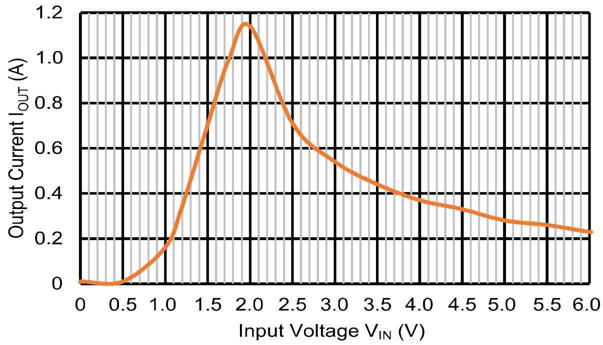
0.75V Output Dropout Voltage (1000mA)



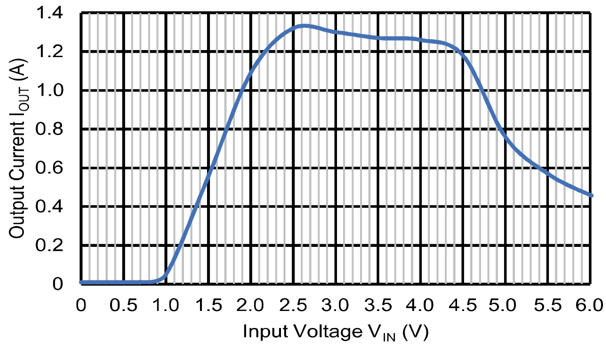
3.3V Output Dropout Voltage



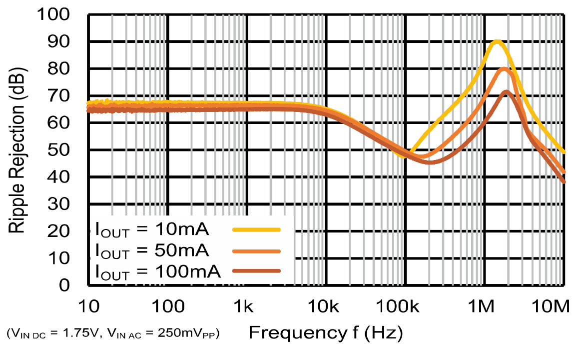
0.75V Output Current Limit



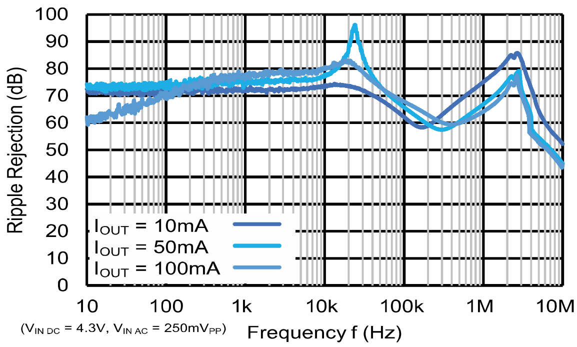
3.3V Output Current Limit



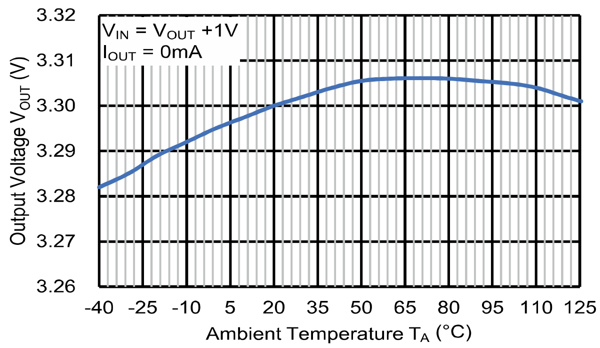
0.75V Output Ripple Rejection



3.3V Output Ripple Rejection



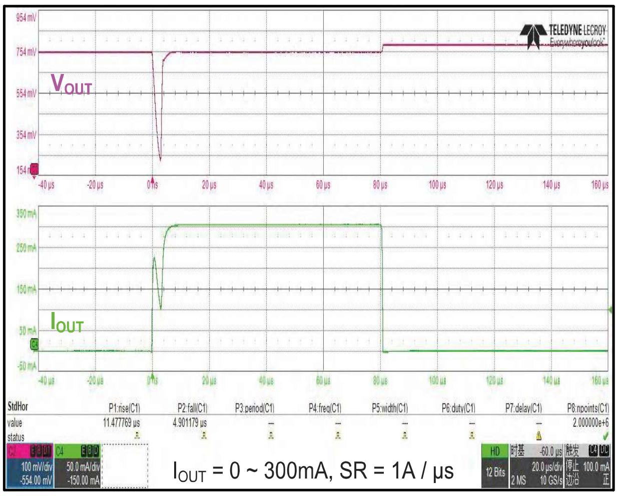
3.3V Output Temperature Characteristics



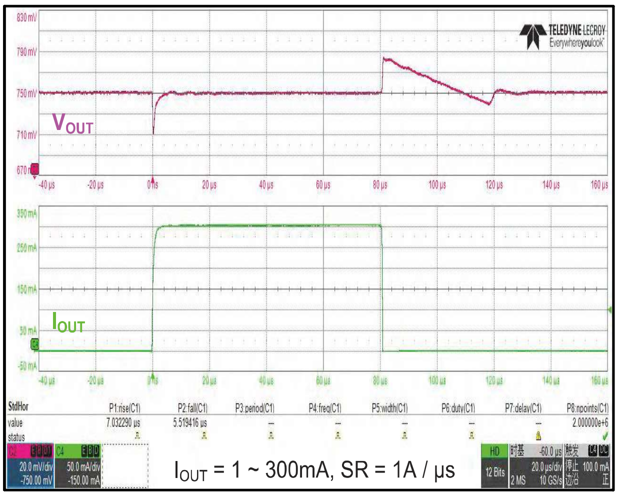
FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

Rating and characteristic curves (C_{IN} = 1μF, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

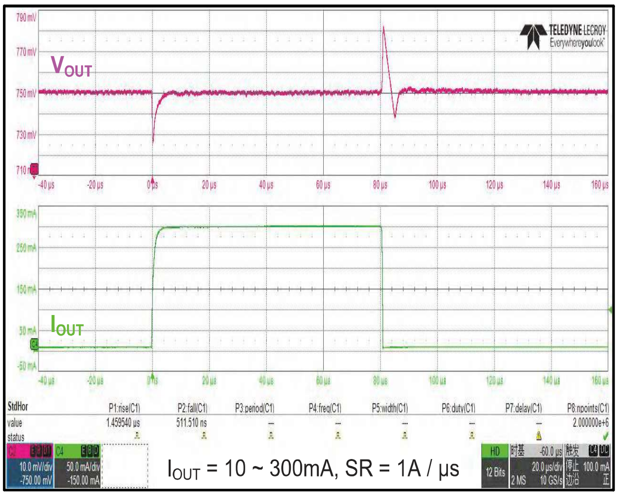
Load Transient (V_{IN} = 1.8V, V_{OUT} = 0.75V)



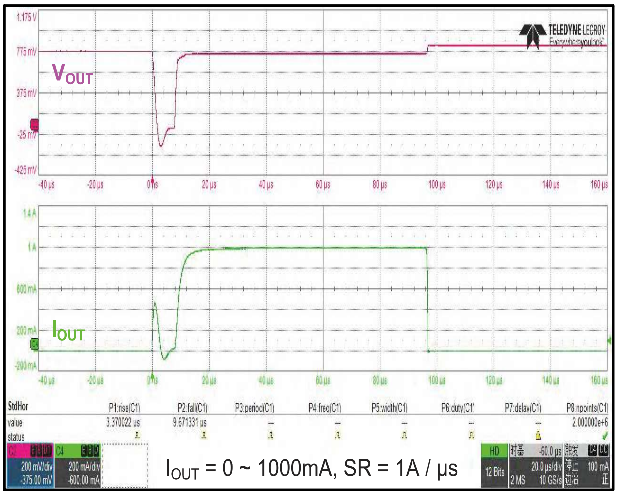
I_{OUT} = 0 ~ 300mA, SR = 1A / μs



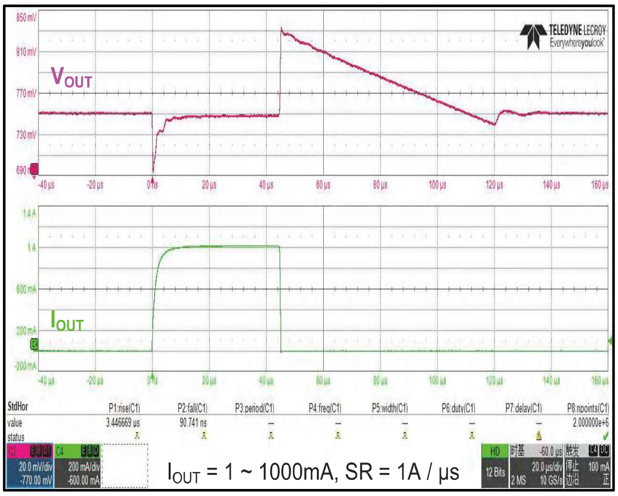
I_{OUT} = 1 ~ 300mA, SR = 1A / μs



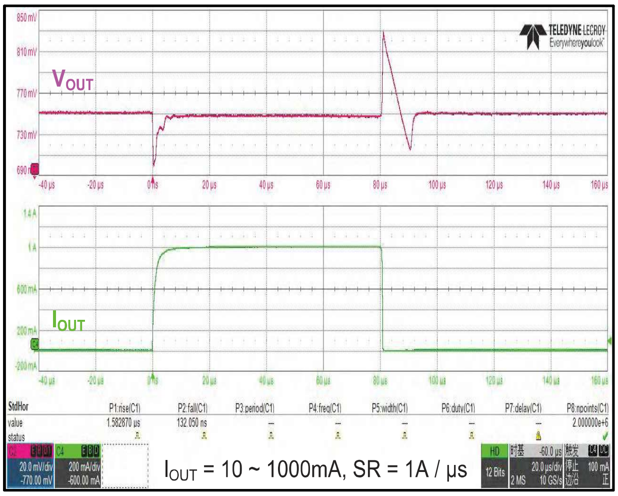
I_{OUT} = 10 ~ 300mA, SR = 1A / μs



I_{OUT} = 0 ~ 1000mA, SR = 1A / μs



I_{OUT} = 1 ~ 1000mA, SR = 1A / μs

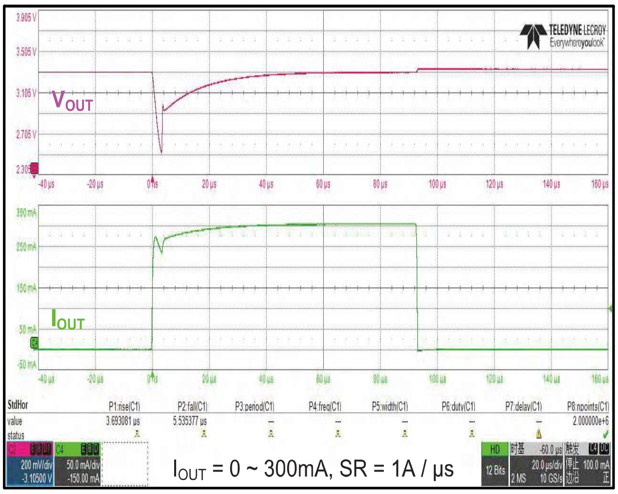


I_{OUT} = 10 ~ 1000mA, SR = 1A / μs

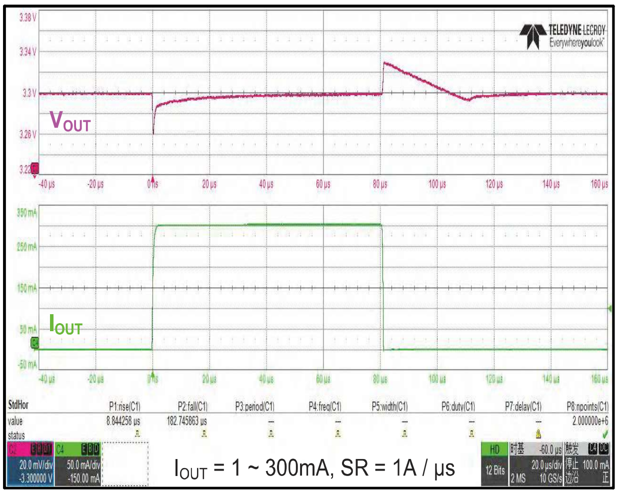
FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

Rating and characteristic curves (C_{IN} = 1μF, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

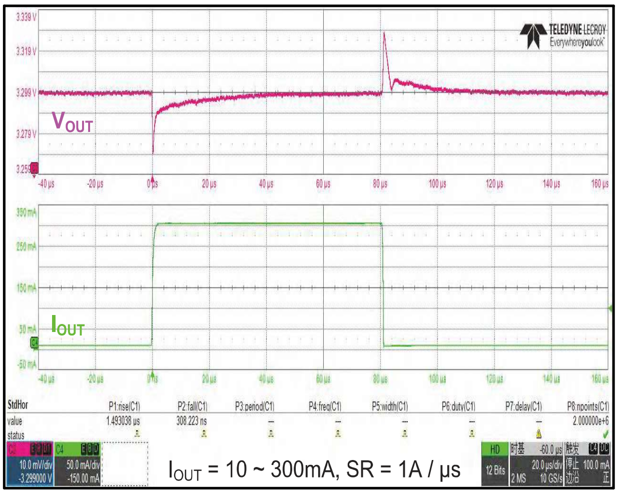
Load Transient (V_{IN} = 4.3V, V_{OUT} = 3.3V)



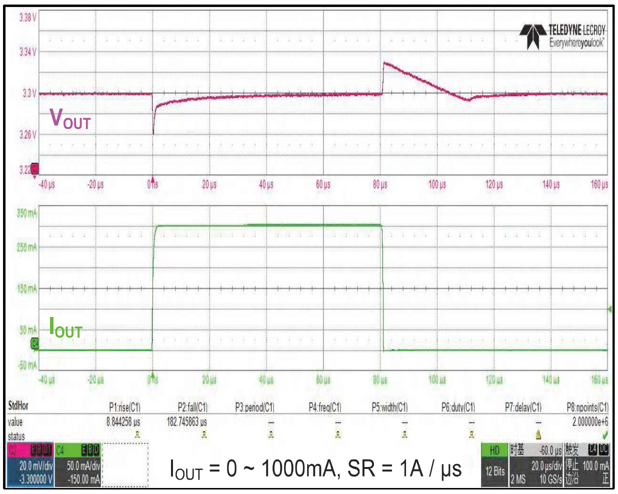
I_{OUT} = 0 ~ 300mA, SR = 1A / μs



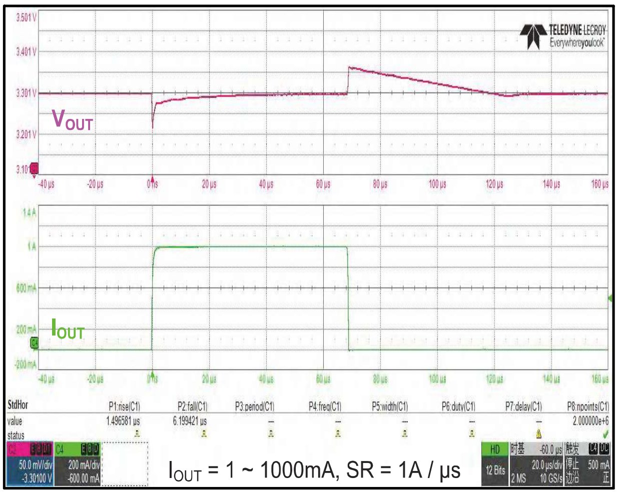
I_{OUT} = 1 ~ 300mA, SR = 1A / μs



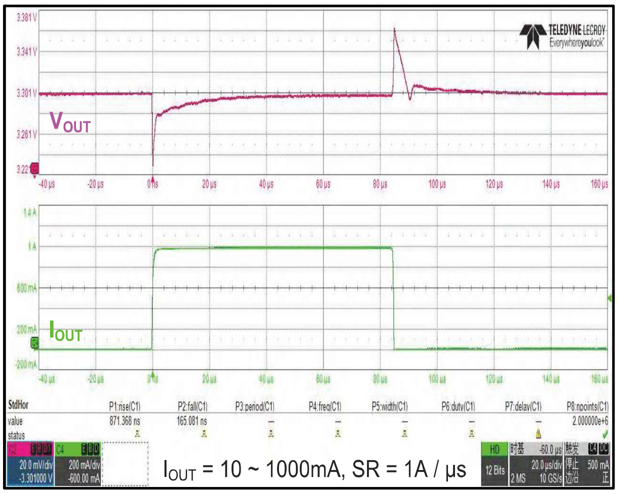
I_{OUT} = 10 ~ 300mA, SR = 1A / μs



I_{OUT} = 0 ~ 1000mA, SR = 1A / μs



I_{OUT} = 1 ~ 1000mA, SR = 1A / μs

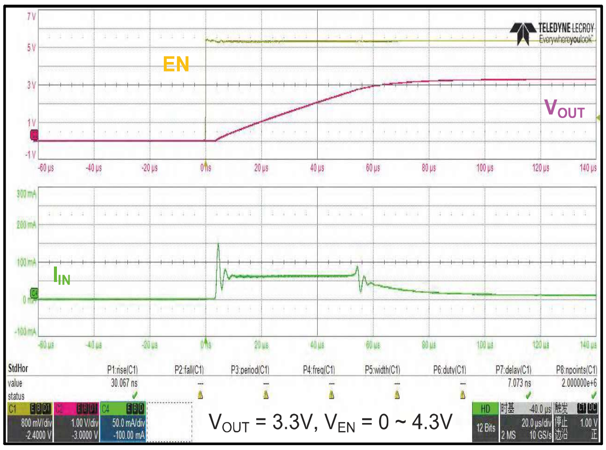


I_{OUT} = 10 ~ 1000mA, SR = 1A / μs

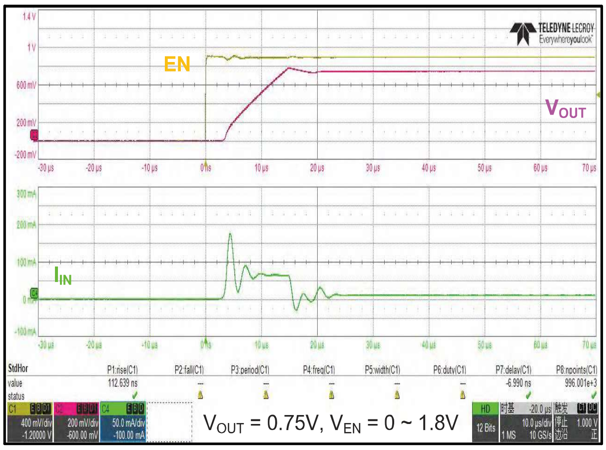
FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

Rating and characteristic curves (C_{IN} = 1μF, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

EN High (V_{IN} = V_{OUT}+1V, I_{OUT} = 10mA)



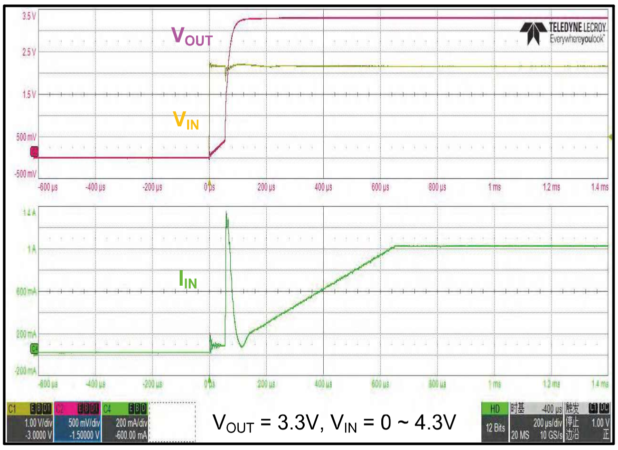
V_{OUT} = 3.3V, V_{EN} = 0 ~ 4.3V



V_{OUT} = 0.75V, V_{EN} = 0 ~ 1.8V

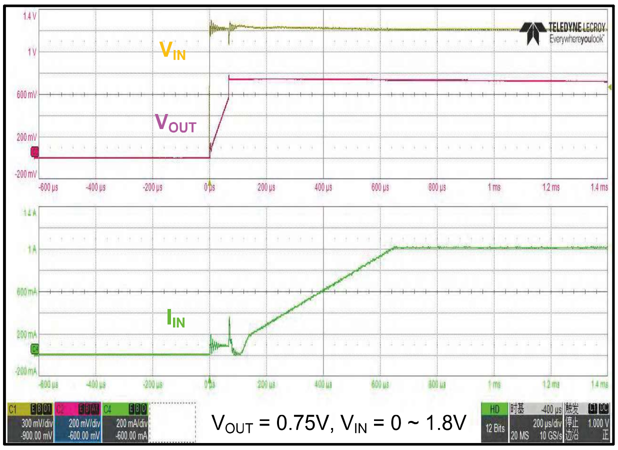
Power-up Response (V_{EN} = VIN, I_{OUT} = 1000mA)

(Using electronic load as output)



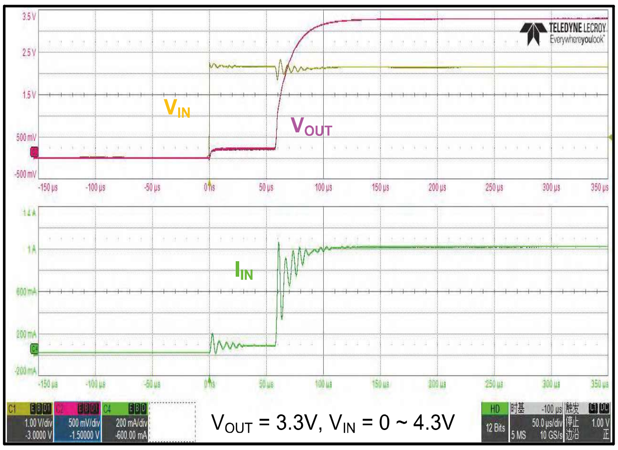
V_{OUT} = 3.3V, V_{IN} = 0 ~ 4.3V

(Using electronic load as output)



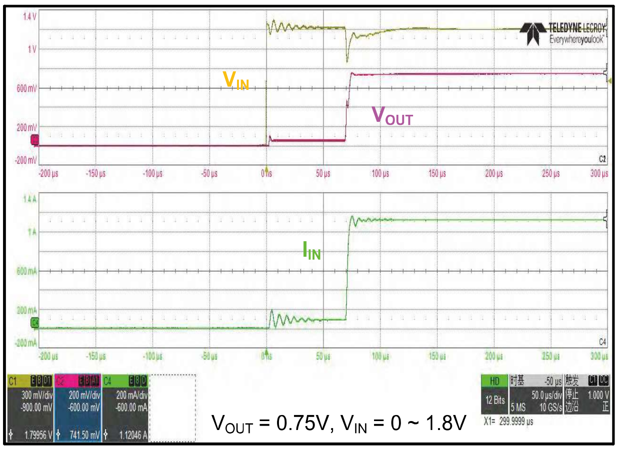
V_{OUT} = 0.75V, V_{IN} = 0 ~ 1.8V

(Using resistance as output)



V_{OUT} = 3.3V, V_{IN} = 0 ~ 4.3V

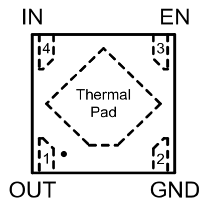
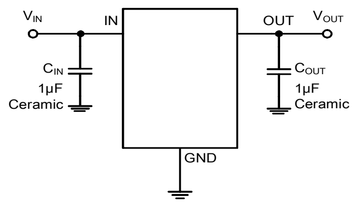
(Using resistance as output)



V_{OUT} = 0.75V, V_{IN} = 0 ~ 1.8V

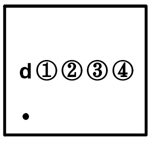
FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

Pinning information

Pin	Simplified outline	Symbol
Pin 1 OUT Pin 2 GND Pin 3 EN Pin4 IN		

1. GND : Regulator ground.
2. OUT : Output of the regulator. An output capacitor is required for stability and help device obtain the best transient response. Use the capacitor with the recommended value and place it as close as possible to the output.
3. IN : Input to the device. Use the recommended value of the input capacitor and place it as close to the input of the device as possible to reduce the impedance of the input supply.
4. EN : Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. Don't float this pin. If enable functionality is not required, this pin must be connected to IN.
5. Thermal Pad: Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

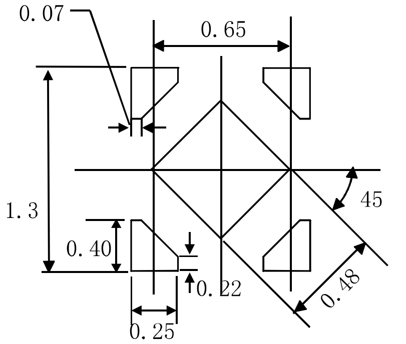
Marking



	Marking code	Description
①	Q	FMLDC0610A1V1AWH
	B	FMLDC0610A1V2AWH
	D	FMLDC0610A1V8AWH
	F	FMLDC0610A2V8AWH
	G	FMLDC0610A3V0AWH
	H	FMLDC0610A3V3AWH
②③	XX	Code, indicates weekly record information of wafer lot code
④	X	Code, special pin arrangement sequence. (blank): Normal

Suggested solder pad layout

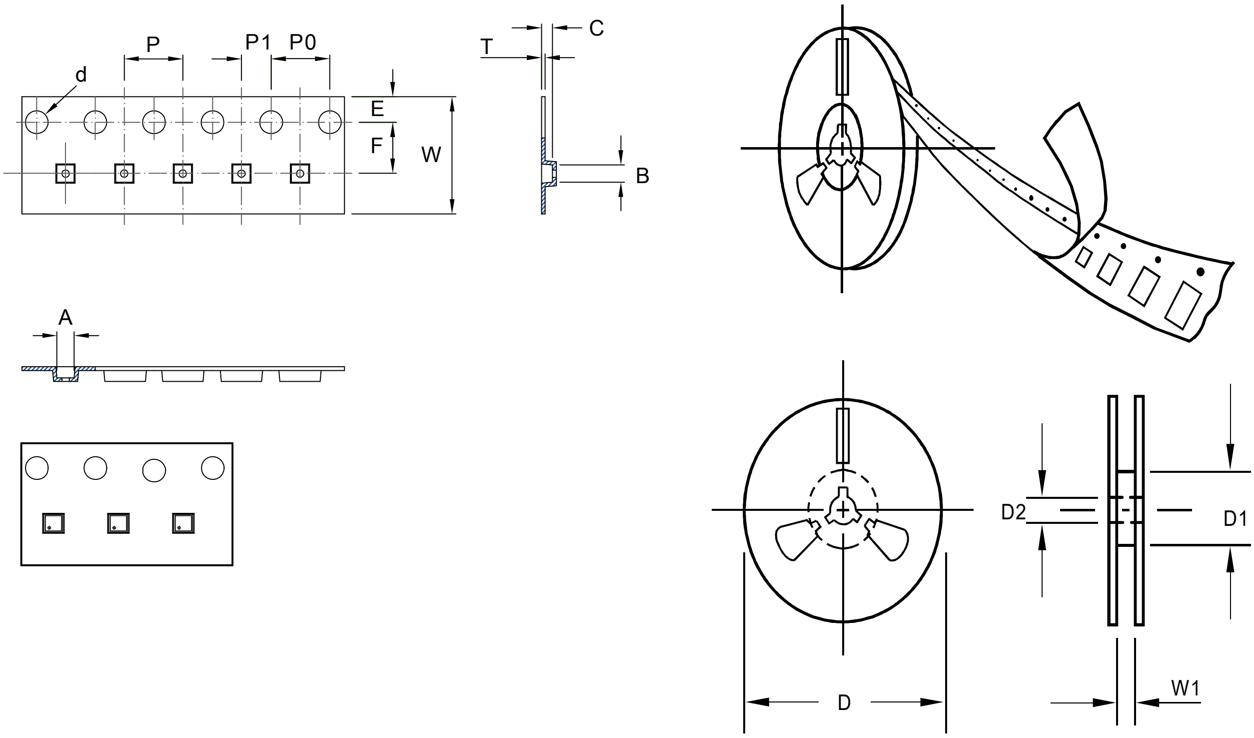
T1010P4



Dimensions in inches and (millimeters)

FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

Packing information



Unit : mm

Item	Symbol	Tolerance	T1010P4
Carrier width	A	±0.1	1.12
Carrier length	B	±0.1	1.13
Carrier depth	C	±0.1	0.50
Sprocket hole	d	±0.1	1.55
7" Reel outside diameter	D	±1.0	178.00
7" Reel inner diameter	D1	±0.5	54.50
Feed hole diameter	D2	±0.3	13.50
Sprocket hole position	E	±0.1	1.75
Punch hole position	F	±0.1	3.50
Punch hole pitch	P	±0.1	4.00
Sprocket hole pitch	P0	±0.1	4.00
Embossment center	P1	±0.1	2.00
Over all tape thinkness	T	±0.1	0.20
Tape width	W	±0.2	8.00
Reel width	W1	±0.2	9.60

Note : Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

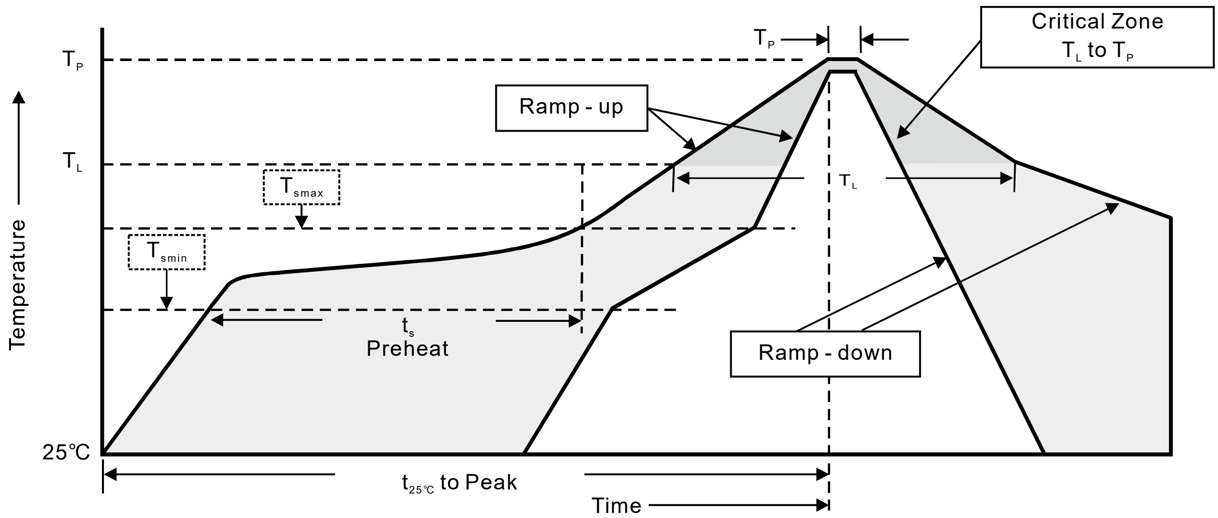
FMLDC0610A1V1AWH Thru FMLDC0610A3V3AWH

Reel packing

Package	Units (pcs)			Dimension (Unit : mm^3)		
	Reel	Inner Box	Outer Box	Reel DIA,	Inner Box	Outer Box
T1010P4	3,000	100,000	400,000	178 (7")	210 x 208 x 205	440 x 440 x 230

Suggested thermal profiles for soldering processes

1. Storage environment : Temperature = 5℃ ~ 40℃, Humidity = 55%, ±25%.
2. Reflow soldering of surface - Mount devices.



3.Reflow soldering

Profile feature	Soldering condition
Average ramp-up rate (T_L to T_P)	< 3 ℃/sec
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (Min to Max) (t_s)	150℃ 200℃ 60 ~ 120 sec
T_{smax} to T_L - Ramp-up rate	< 3 ℃ / sec
Time maintained above : - Temperature (T_L) - Time (T_L)	217℃ 60 ~ 260 sec
Peak temperature (T_P)	255 ℃ -0 / +5℃
Time with 5℃ of actual peak temperature (T_P)	10 ~ 30 sec
Ramp-down rate	< 6℃ / sec
Time 25℃ to peak temperature	< 6 minutes