

LL05BT1006A-Q1

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Ultra Low Capacitance Bi-Directional TVS For ESD Protection 5.0V

Features

- Package optimized for high-speed lines.
- Protects one data, control or power line.
- Each I/O pin can withstand over 1000 ESD strikes for $\pm 8\text{kV}$ contact discharge.
- Provide transient protection:
 - IEC 61000-4-2 (ESD) $\pm 25\text{kV}$ (Air), $\pm 20\text{kV}$ (Contact).
 - IEC 61000-4-4 (EFT) 40A (5/50ns).
 - Cable discharge event (CDE).
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen-free parts, ex. LL05BT1006A-Q1-H,

Applications

- Serial ATA.
- PCI Express.
- Desktops, servers, notebooks and cellular phones.
- MDDI ports, display ports, and digital visual interfaces (DVI).
- USB 2.0/3.0 Power and data line protection.
- HDMI 1.4/2.0.

Mechanical data

- Epoxy: UL94V-0 rated flame retardant.
- Case : Molded plastic, T1006P2.

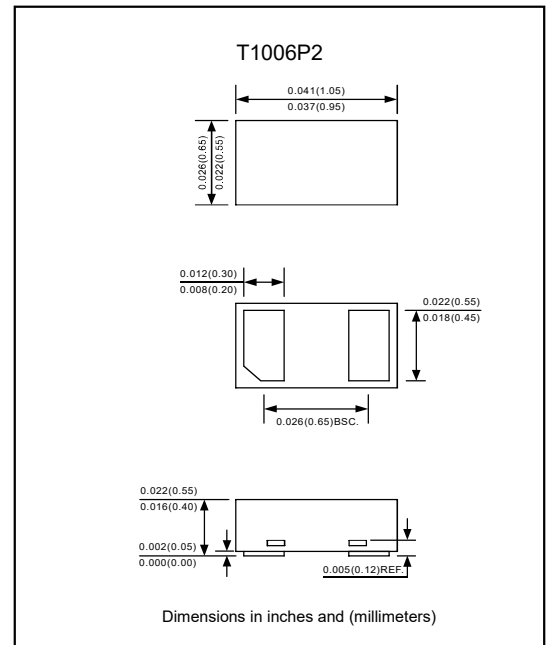
Maximum ratings (At $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak pulse current ($t_p=8/20\mu\text{s}$)	I_{PP}	4.5	A
ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 20	kV
ESD per IEC 61000-4-2 (Air)		± 25	
Operating temperature	T_{OPT}	+125	$^\circ\text{C}$
Storage temperature	T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical characteristics (At $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Reverse stand-off voltage		V_{RWM}			5	V
Reverse leakage current	$V_{RWM}=5.0\text{V}$, Between I/O and I/O	I_R		0.01	0.1	μA
Trigger voltage	$I_T=1\text{mA}$, Between I/O and I/O	V_{BR}	7		9	V
Clamping voltage	$I_{PP}=4.5\text{A}$, $t_p=8/20\mu\text{s}$, Between I/O and I/O	V_C			15	V
Junction capacitance	$V_R=0\text{V}$, $f=1.0\text{MHz}$, Between I/O and I/O	C_{ESD}		0.3		pF

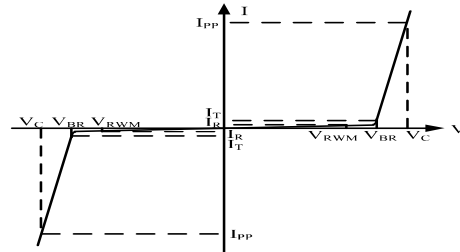
Package outline



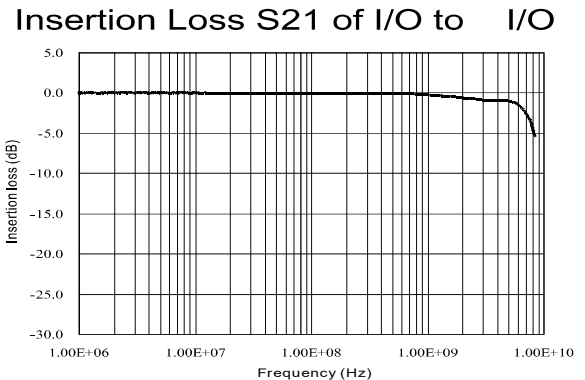
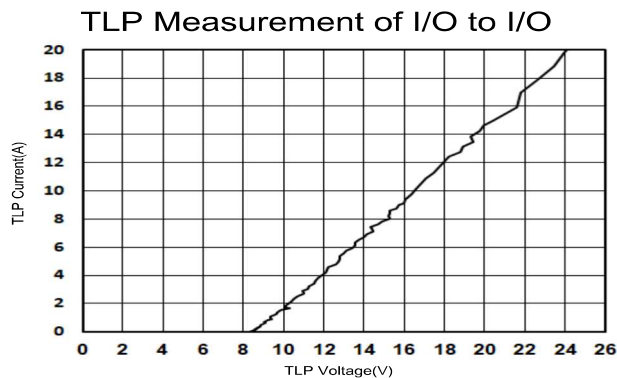
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Rating and characteristic curves

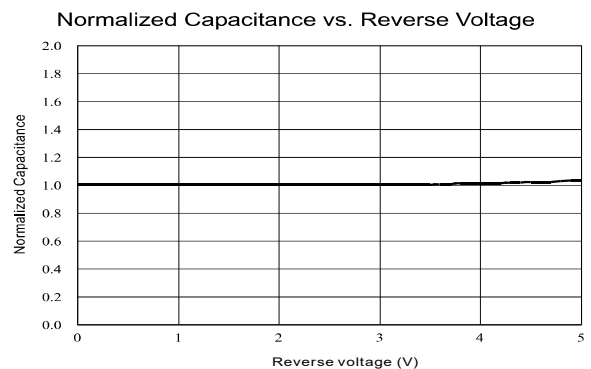
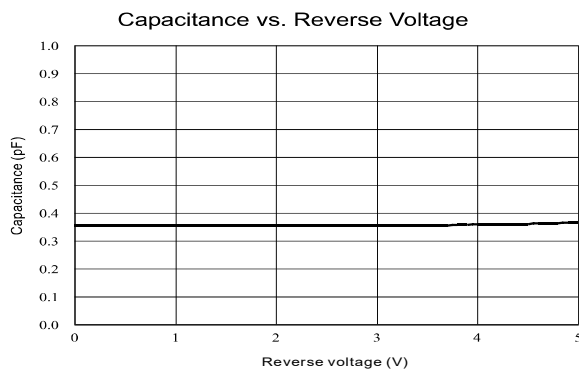
Symbol	Parameter
V_{RWM}	Nominal reverse working voltage
I_R	Reverse leakage current@ V_{RWM}
V_{BR}	Reverse breakdown voltage@ I_T
I_T	Test current for reverse breakdown
V_C	Clamping voltage @ I_{PP}
I_{PP}	Peak pulse current
C_{ESD}	Parasitic capacitance
V_R	Reverse voltage
f	Small signal frequency



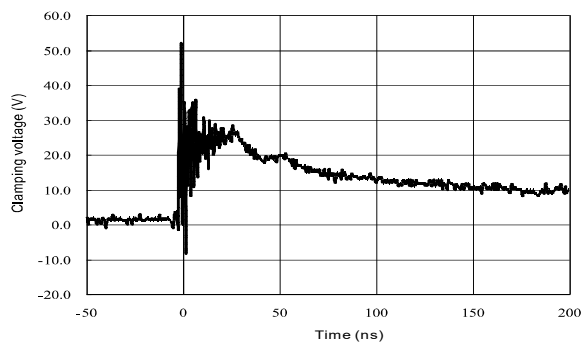
Bi-Directional TVS



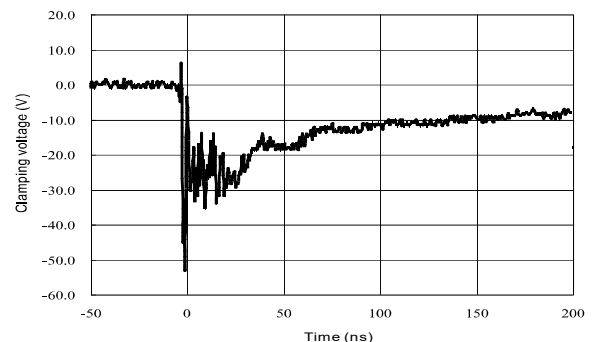
Capacitance vs. Voltage of I/O to I/O (f = 1MHz)



ESD Clamping of I/O to I/O (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to I/O (-8kV Contact per IEC 61000-4-2)



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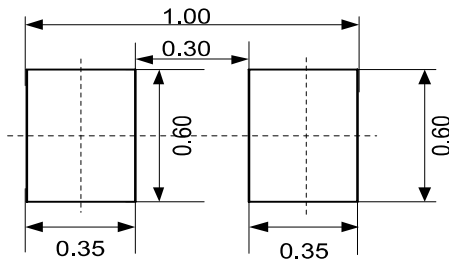
Pinning information

Pin	Simplified outline	Symbol
Bi-directional	1 2 Top view 2 1 Bottom view	

Marking

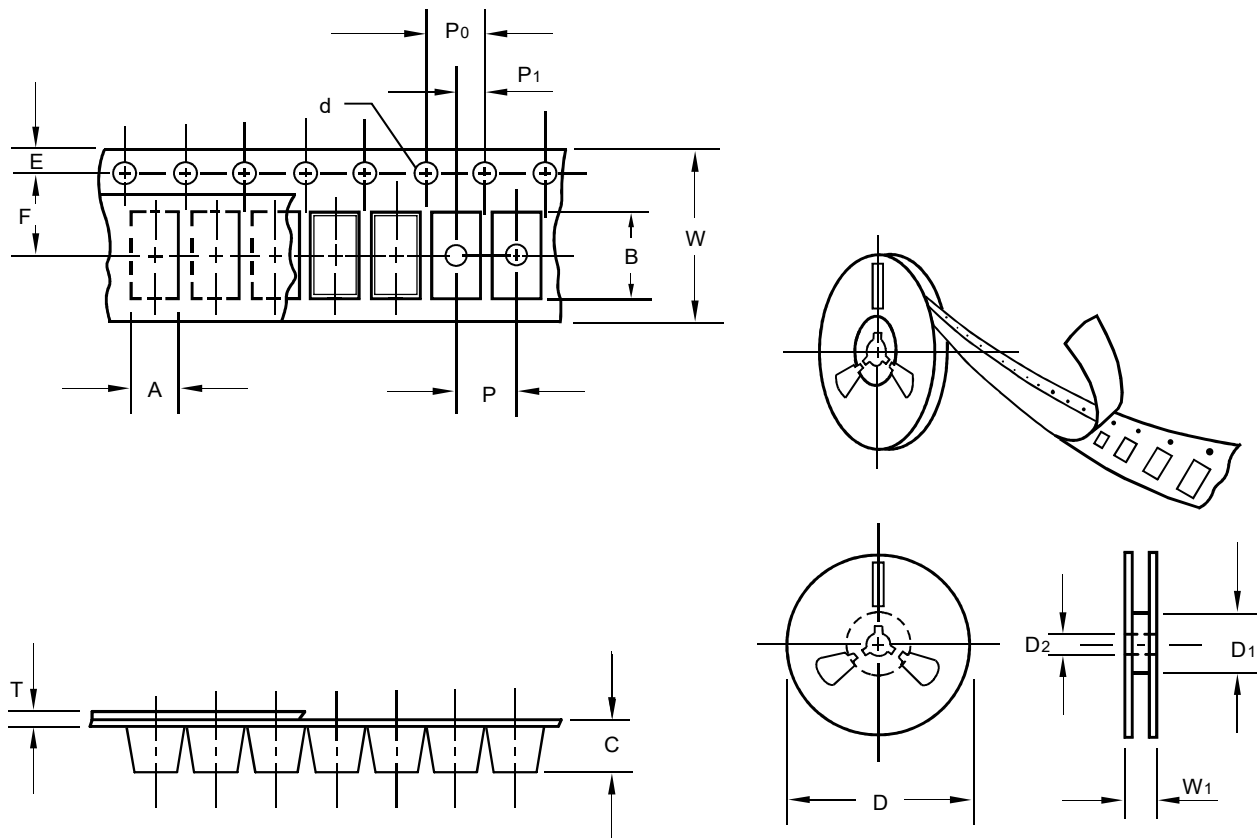
Type number	Marking code
LL05BT1006A-Q1	XS or S

Suggested solder pad layout



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Packing information



unit:mm

Item	Symbol	Tolerance	T1006P2
Carrier width	A	0.1	0.70
Carrier length	B	0.1	1.15
Carrier depth	C	0.1	0.55
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	55.00
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	2.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.20
Tape width	W	0.3	8.00
Reel width	W1	1.0	9.50

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

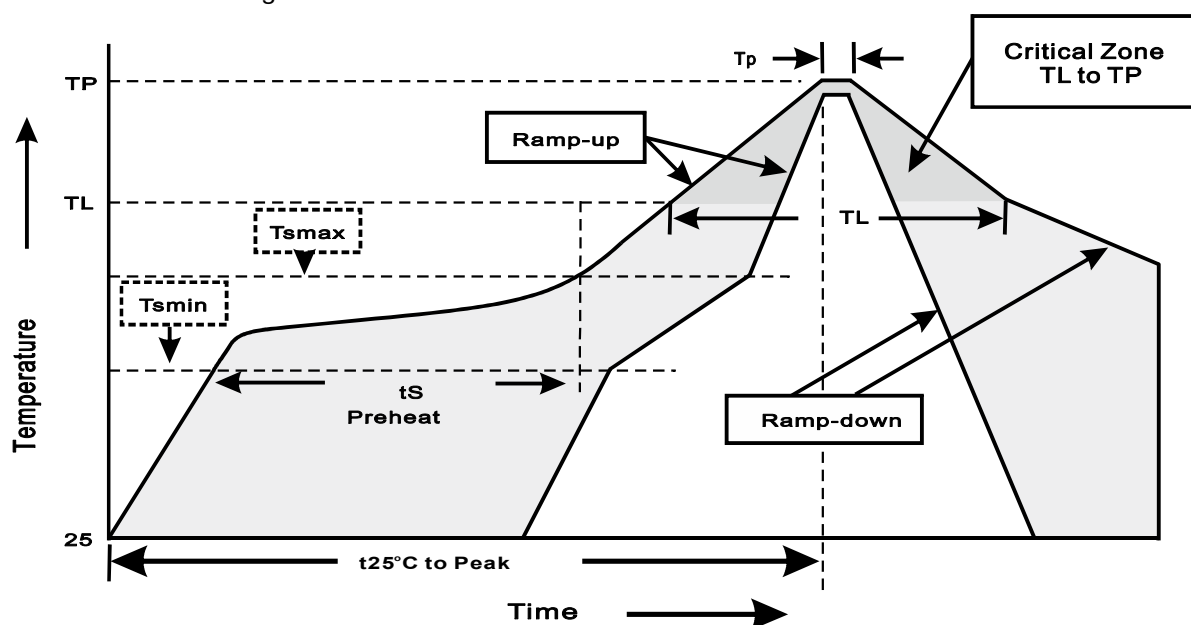
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
T1006P2	7"	10,000	4.0	100,000	183*123*183	178	382*257*387	800,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	$<3^{\circ}\text{C}/\text{sec}$
Preheat -Temperature Min(T_{min}) -Temperature Max(T_{max}) -Time(min to max)(t_s)	150°C 200°C $60\sim 120\text{sec}$
T_{max} to T_L -Ramp-upRate	$<3^{\circ}\text{C}/\text{sec}$
Time maintained above: -Temperature(T_L) -Time(t_L)	217°C $60\sim 260\text{sec}$
Peak Temperature(T_P)	$255^{\circ}\text{C}-0/+5^{\circ}\text{C}$
Time within 5°C of actual Peak Temperature(t_P)	$10\sim 30\text{sec}$
Ramp-down Rate	$<6^{\circ}\text{C}/\text{sec}$
Time 25°C to Peak Temperature	$<6\text{minutes}$