

LL05BT0603E-1

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Surface Mount TVS Bi-Directional For ESD Protection-5.0V

Features

- Transient protection for high-speed data line.
- Low capacitance : 0.3pF (Typical).
- Low reverse current : <100nA (@VR=5V).
- Solid-state silicon-avalanche technology.
IEC 61000-4-2 (ESD) ±25KV(Air), ±25KV(Contact).
- We declare that the material of product compliance with RoHS requirements.
- Suffix "-H" indicates Halogen-free parts, ex.LL05BT0603E-1-H.

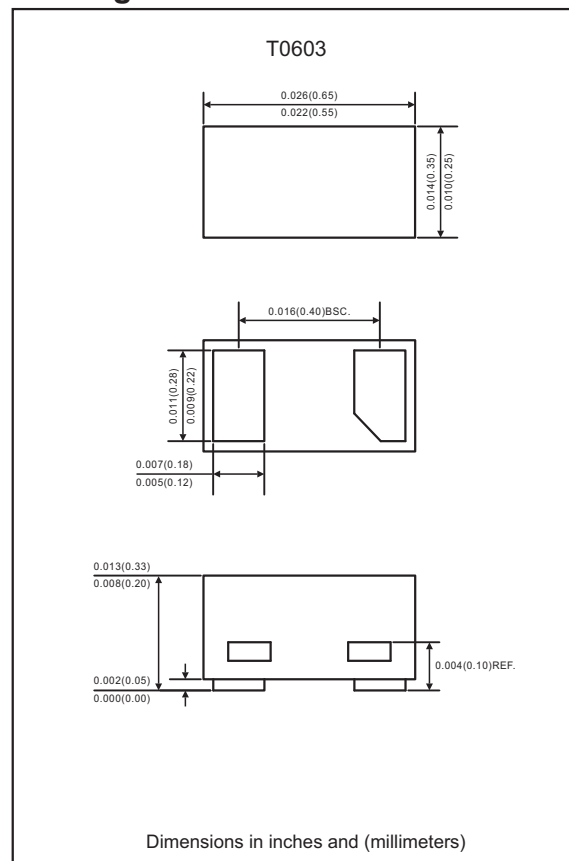
Applications

- HDMI 1.3 / 1.4 and HDMI 2.0.
- USB 2.0 and USB 3.0.
- LVDS Interfaces.
- FM Antenna.
- PCI Express.
- MHL.
- eSATA Interfaces.

Mechanical data

- T0603 package
- pb-Free, Halogen free. RoHS / WEEE compliant.
- Nominal dimensions : 0.6 x 0.3 x 0.25mm.
- Lead finish : NiAu.
- Molding compound flammability rating : UL 94V-0.
- Weight : Approximated 1 mg.

Package outline

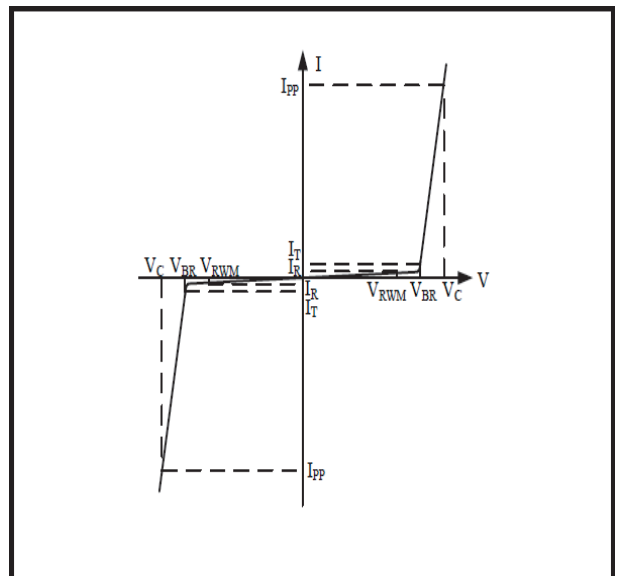


Maximum ratings (at T_A=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak pulse current (t _p =8/20μs)	I _{PP}	5	A
ESD per IEC 61000-4-2 (Contact)	V _{ESD}	±25	KV
ESD per IEC 61000-4-2 (Air)		±25	
Operating temperature	T _J	+125	°C
Storage temperature	T _{STG}	-55 to +150	°C

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Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current


Electrical characteristics (at $T_A=25^\circ\text{C}$ unless otherwise noted)

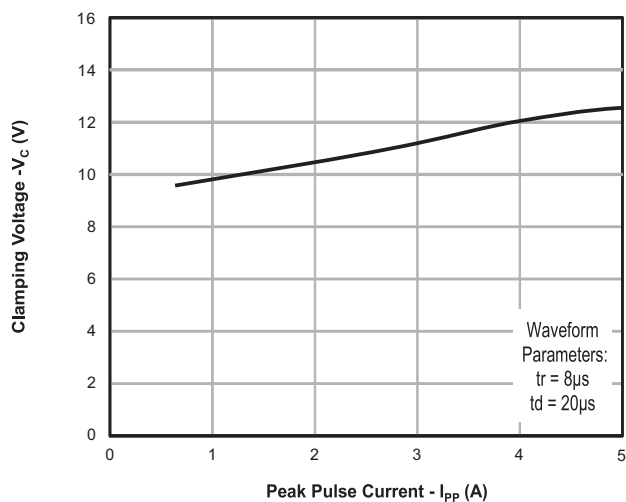
Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Reverse stand-off voltage		V_{RWM}			5.0	V
Reverse breakdown voltage	$I_T=1\text{mA}$	V_{BR}	7.0	8.5	10.0	V
Reverse leakage current	$V_{RWM}=5.0\text{V}$	I_R		0.01	0.1	μA
Clamping voltage @ I_{PP}	$I_{PP}=1\text{A}, t_p=8/20\mu\text{s}$	V_C		10.5	12	V
	$I_{PP}=5\text{A}, t_p=8/20\mu\text{s}$			13	15	
Dynamic resistance (Note 1)	$I_{PP}=12.0\text{A}, t_p=100\text{ns}$	R_D		0.37		Ω
Junction capacitance	$V_R=0\text{V}, f=1\text{MHz}$	C_J		0.3		pF

Note :

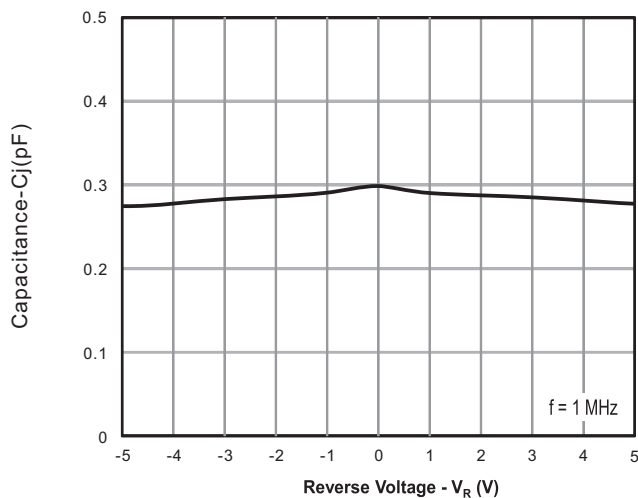
1. Measurements performed using a 100ns Transmission Line Pulse (TLP) system.

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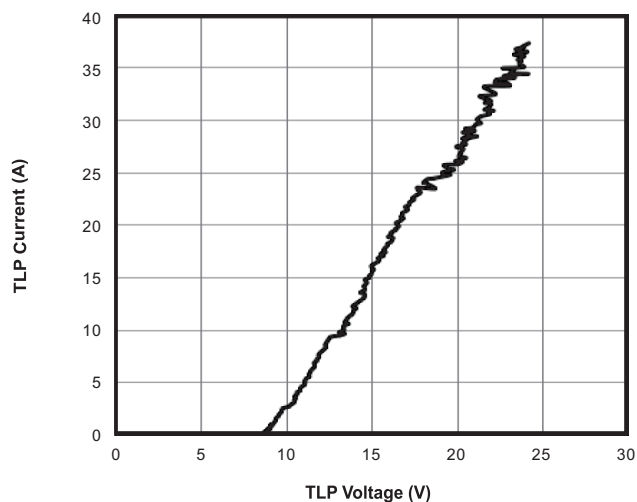
Clamping Voltage vs. Peak Pulse Current



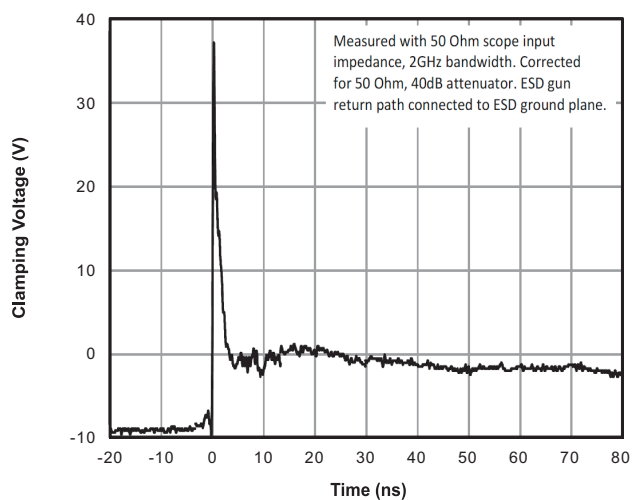
Typical Capacitance vs. Reverse Voltage



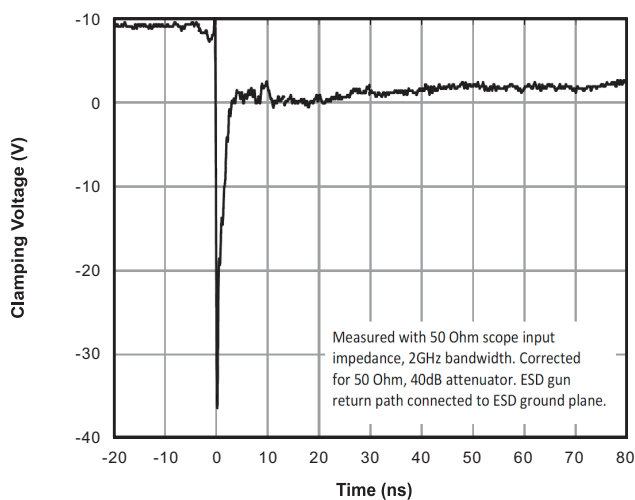
TLP Characteristic



ESD Clamping (+8kV Contact per IEC 61000-4-2)

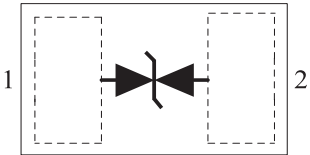


ESD Clamping (-8kV Contact per IEC 61000-4-2)



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Pinning information

Type Number	Simplified outline	Circuit Diagram
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Marking code

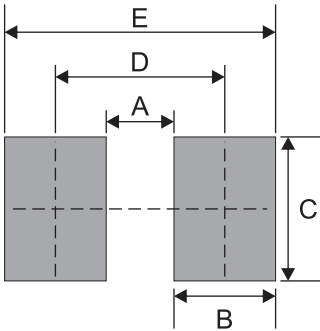


Note:

(1) “SA” is part number, fixed

Suggested solder pad layout

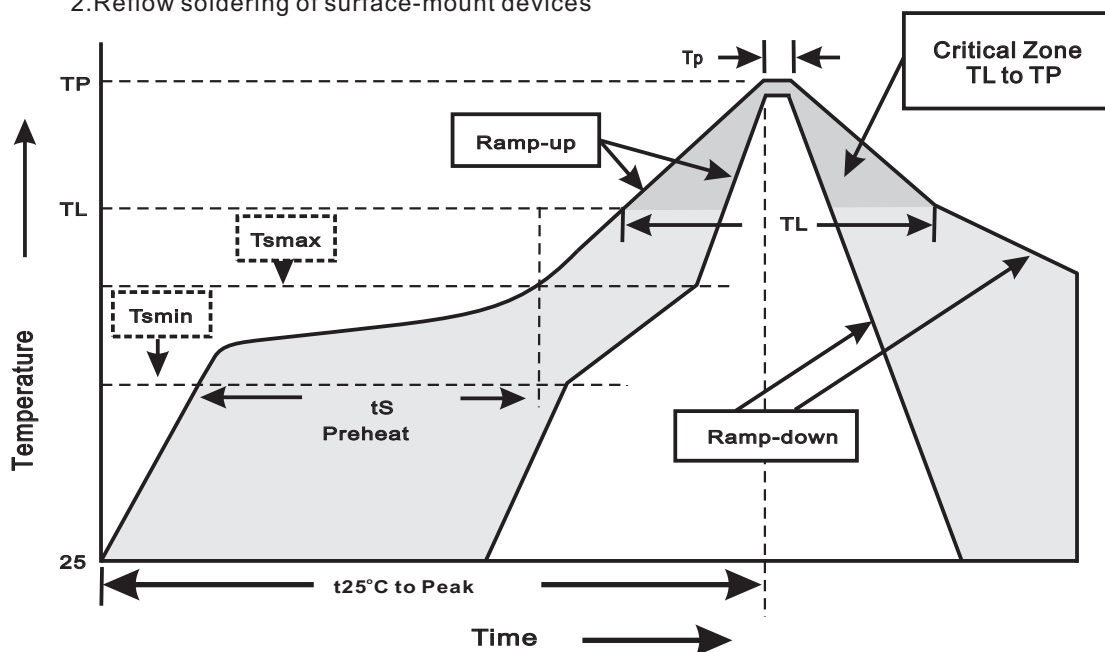
SIZE	T0603	
	(mm)	(inch)
A	0.16	0.006
B	0.24	0.009
C	0.34	0.013
D	0.40	0.016
E	0.64	0.025



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Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smin}) -Temperature Max(T _{smax}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smax} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes