

LL05AT723

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LL05AT723

Surface Mount Ultra Low Capacitance For ESD Protection Diode 5V

Features

- IEC61000-4-2 (ESD) $\pm 25\text{kV}$ (air), $\pm 17\text{kV}$ (contact)
- IEC61000-4-4 (EFT) 40A (5/50ns)
- Working voltages : 5V
- Low capacitance
- Low clamping voltage
- Low leakage current
- Lead-free parts meet RoHS requirements
- Suffix "-H" indicates Halogen-free part, ex.LL05AT723-H.

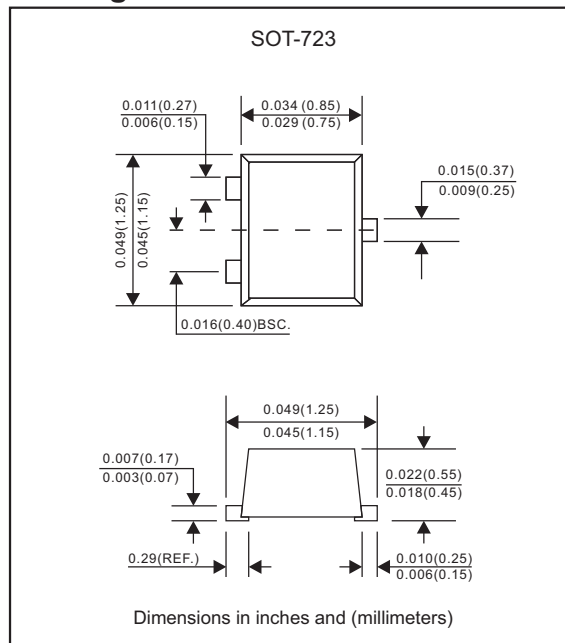
Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB2.0 Power and Data Line Protection
- Display Ports
- Digital Visual Interfaces(DVI)

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-723
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.001 gram

Package outline



Maximum ratings (at $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	Limit	UNIT
Peak pulse power (According to IEC 61000-4-5)	PP	50	Watt
Peak pulse current (According to IEC 61000-4-5)	IPP	5	A
IEC 61000-4-2 ESD air model contact model	VESD	± 25 ± 17	kV
Operating junction temperature range	TJ	-55 to +125	$^\circ\text{C}$
Storage temperature range	TSTG	-55 to +150	$^\circ\text{C}$

Electrical characteristics (at $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Reverse stand off voltage		VRWM			5.0	V
Reverse breakdown voltage	IT = 1mA,	VBR	6.0		10.0	V
Reverse leakage current	VRWM = 5V	IR			0.1	μA
Clamping voltage (Note 1)	IPP=1A, tp=8/20us, Between I/O and GND IPP=5A, tp=8/20us, Between I/O and GND	VC			9.0 11.0	V
Junction capacitance	VR=0V, f=1MHz, Between I/O and GND VR=0V, f=1MHz, Between I/O and I/O	CJ		0.7 0.35	0.8 0.4	pF

Note:

1. Non-repetitive current pulse 8/20 us exponential decay waveform according to IEC61000-4-5.

Rating and characteristic curves(LL05AT723)

Fig.1 VOLTAGE SWEEPING OF I/O TO GND

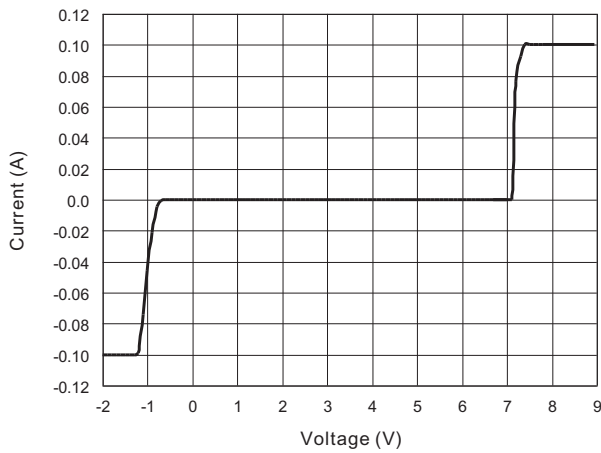


Fig.2 INSERTION LOSS S₂₁ of I/O to GND

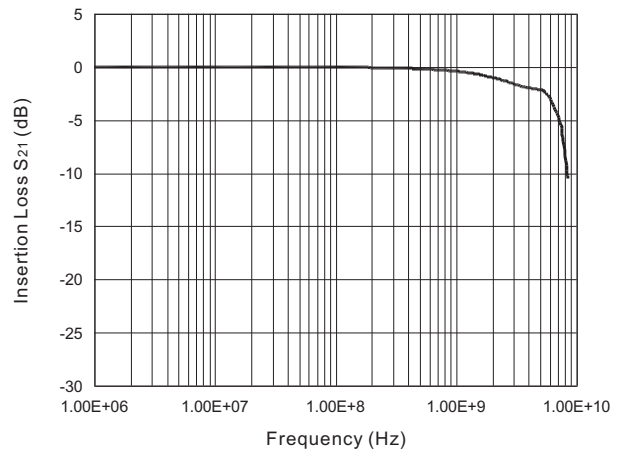


Fig.3 CAPACITANCE VS. REVERSE VOLTAGE

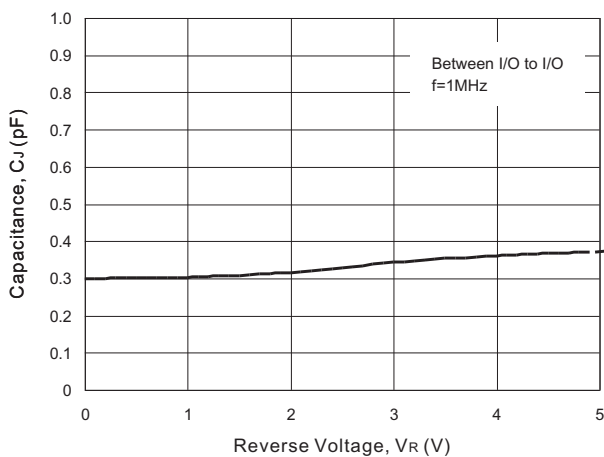


Fig.4 NORMALIZED CAPACITANCE VS. REVERSE VOLTAGE

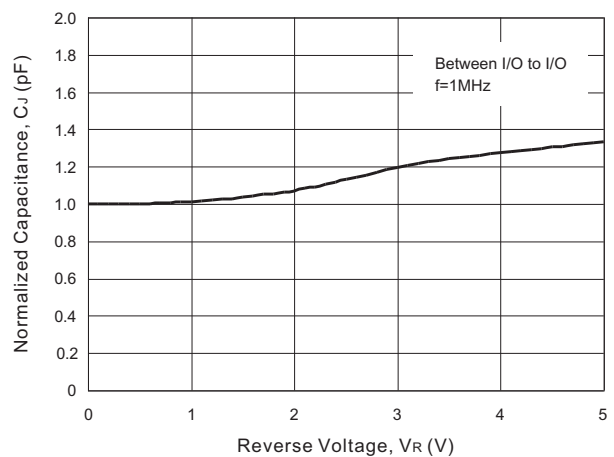


Fig.5 ESD CLAMPING OF I/O TO GND
(+8KV CONTACT PER IEC 61000-4-2)

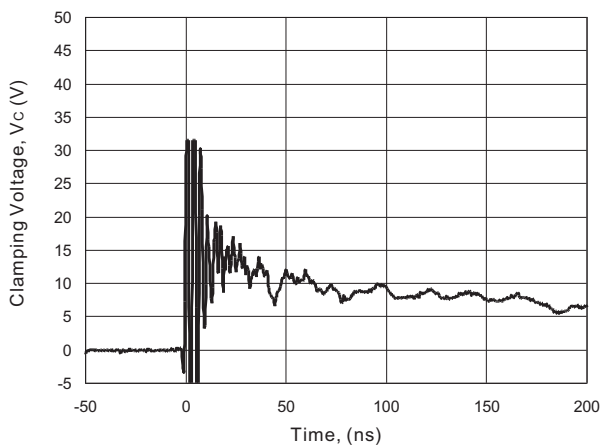
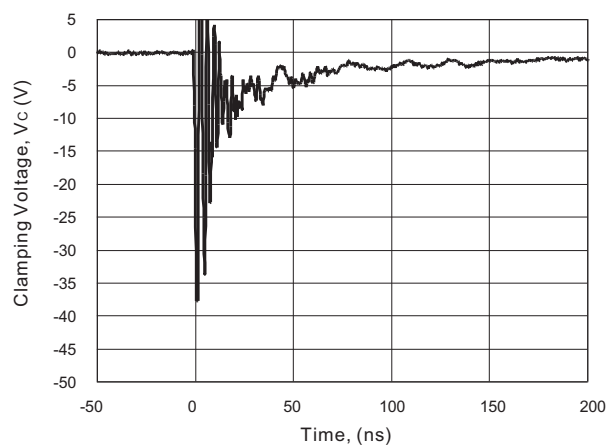
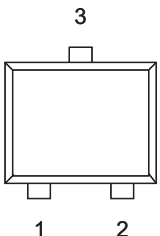
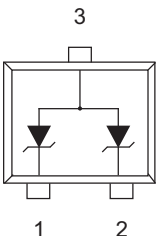


Fig.6 ESD CLAMPING OF I/O TO GND
(-8KV CONTACT PER IEC 61000-4-2)



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Pinning information

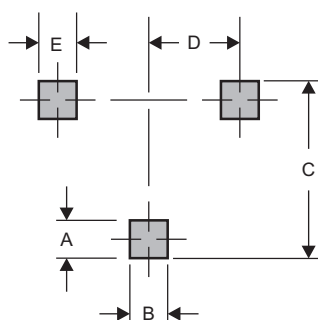
Pin Configuration	Circuit Diagram
 Diagram showing the pin configuration for the SOT-723 package. Pin 3 is at the top, pin 1 is at the bottom left, and pin 2 is at the bottom right.	 Diagram showing the internal circuit of the LL05AT723 TVS diode, which consists of two diodes connected in series between pins 1 and 2, with pin 3 connected to the common cathode/anode point.

Marking

Type number	Marking code
LL05AT723	5T

Suggested solder pad layout

SOT-723

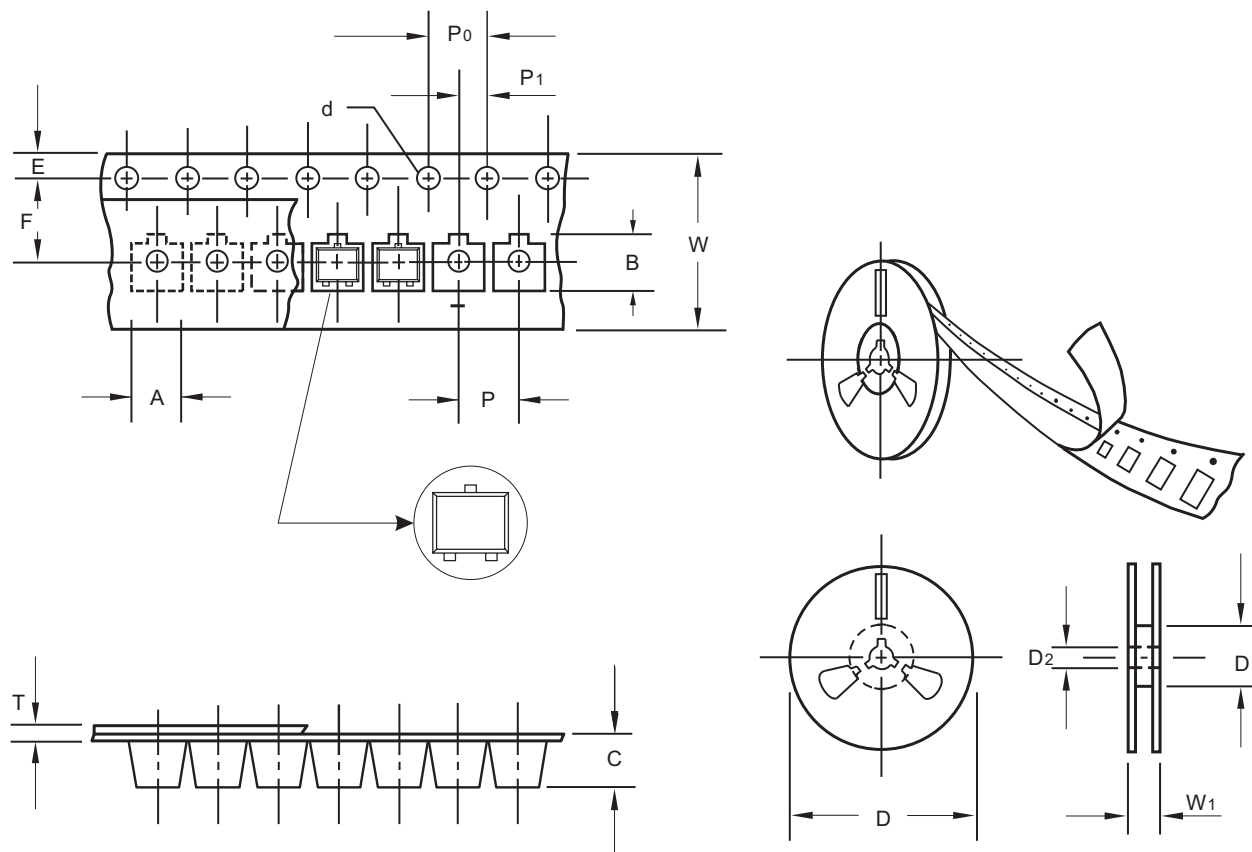


PACKAGE	A	B	C	D	E
SOT-723	0.021 (0.52)	0.014 (0.36)	0.059 (1.50)	0.016 (0.40)	0.011 (0.27)

Dimensions in inches and (millimeters)

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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-723
Carrier width	A	0.1	1.31
Carrier length	B	0.1	1.45
Carrier depth	C	0.1	0.61
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	54.40
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	2.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.20
Tape width	W	+0.3/-0.1	8.00
Reel width	W1	1.0	9.5

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

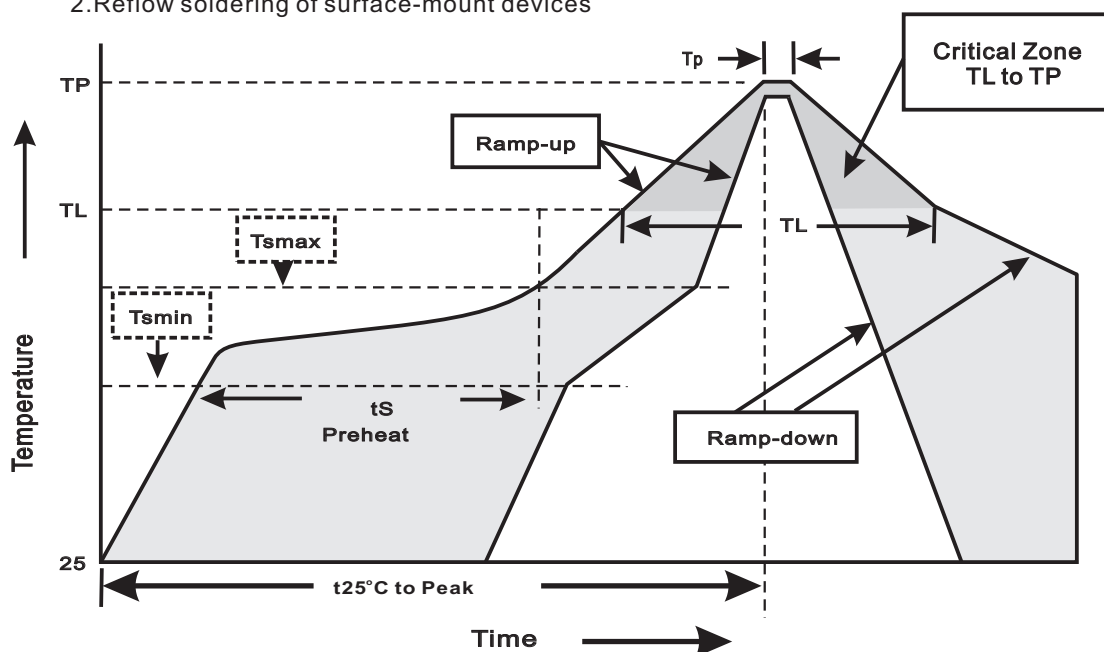
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
SOT-723	7"	3,000	4.0	30,000	183*123*183	178	383*257*387	240,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smmin}) -Temperature Max(T _{smmax}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smmax} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _p)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes

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High reliability test capabilities

Item Test	Conditions	Reference
1. Solder Resistance	at $260\pm5^{\circ}\text{C}$ for $10\pm2\text{sec.}$ immerse body into solder $1/16''\pm1/32''$	MIL-STD-750D METHOD-2031
2. Solderability	at $245\pm5^{\circ}\text{C}$ for 5 sec.	MIL-STD-202F METHOD-208
3. High Temperature Reverse Bias	$V_{\text{BR}} = V_{\text{BR Min}} * 80\%$ at $T_{\text{J}}=150^{\circ}\text{C}$ for 168 hrs.	MIL-STD-750D METHOD-1038
4. Pressure Cooker	$15P_{\text{SIG}}$ at $T_{\text{A}}=121^{\circ}\text{C}$ for 4 hrs.	JESD22-A102
5. Temperature Cycling	-55°C to $+125^{\circ}\text{C}$ dwelled for 30 min. and transferred for 5min. total 10 cycles.	MIL-STD-750D METHOD-1051
6. Humidity	at $T_{\text{A}}=85^{\circ}\text{C}$, RH=85% for 1000hrs.	MIL-STD-750D METHOD-1021
7. High Temperature Storage Life	at 175°C for 1000 hrs.	MIL-STD-750D METHOD-1031