

LL056BT4120

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LL056BT4120

Ultra Low Capacitance 6-Line ESD Protection

Array : 5.0V

Features

- Protects one power line and six data lines.
- Leadless flow-through package.
- Complies with following standards:
 - IEC 61000-4-2 (ESD) immunity test Air discharge : $\pm 25\text{kV}$
Contact discharge: $\pm 20\text{kV}$
 - IEC 61000-4-5 (Lightning) 4A (8/20 μs).
- RoHS compliant.
- Suffix "-H" indicates Halogen-free parts, ex. LL056BT4120-H.

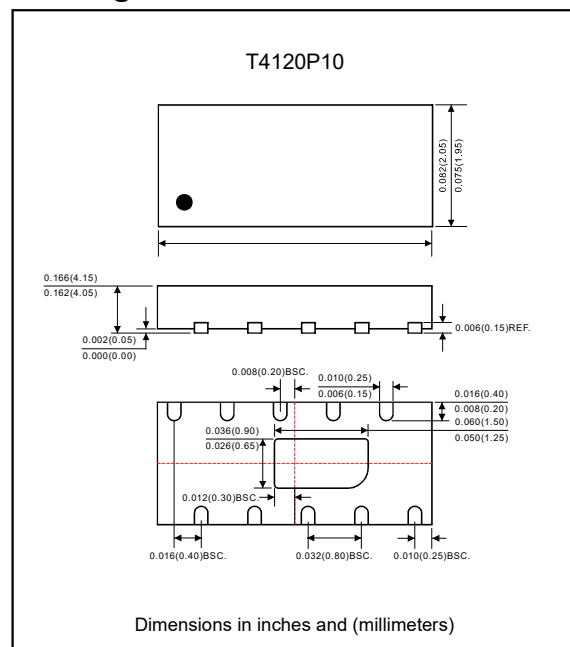
Applications

- USB 3.0.
- HDMI 1.4.
- High-Speed data lines.

Mechanical data

- Package : T4120P10 (4.1 x 2.0 x 0.55mm).
- Case material : "Green" Molding compound.
- Moisture sensitivity : Level 3 per J-STD-020.
- Terminal connections : See diagram below.

Package outline



Maximum ratings (at $T_A=25^\circ\text{C}$ unless otherwise noted)

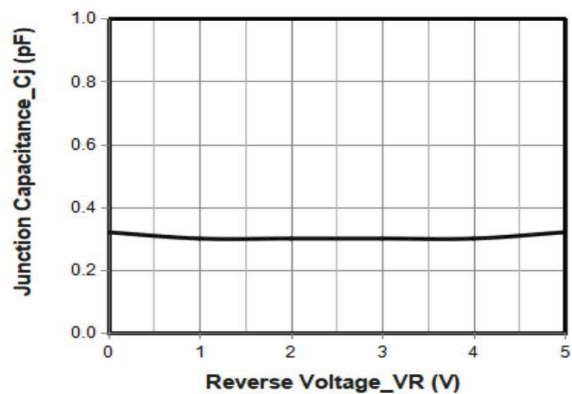
Parameter	Symbol	Value	Unit
Peak pulse power ($t_p=8/20\mu\text{s}$)	P_{PK}	100	W
Maximum peak pulse current ($t_p=8/20\mu\text{s}$)	I_{PP}	4	A
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 25	KV
ESD per IEC 61000-4-4 (Contact)		± 20	
Operating junction temperature	T_J	125	$^\circ\text{C}$
Storage temperature	T_{STG}	-55 to +150	$^\circ\text{C}$
Lead soldering temperature (10 sec)	T_L	260	$^\circ\text{C}$

Electrical characteristics (at $T_A=25^\circ\text{C}$ unless otherwise noted)

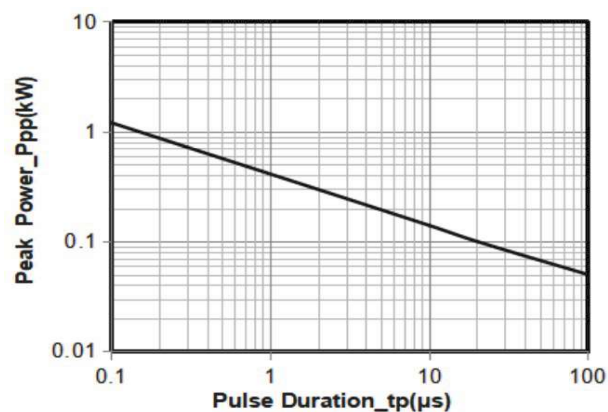
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse working voltage	V_{RWM}				5.0	V
Reverse breakdown voltage	V_{BR}	$I_T=1\text{mA}$ (Any I/O to ground)	6.0			V
Reverse leakage current	I_R	$V_{RWM}=5\text{V}$ (Any I/O to ground)			0.5	μA
Clamping voltage	V_C	$I_{PP}=1\text{A}$, $t_p=8/20\mu\text{s}$ (Any I/O to ground)			12	V
		$I_{PP}=4\text{A}$, $t_p=8/20\mu\text{s}$ (Any I/O to ground)			25	
Junction capacitance	C_J	$V_R=0\text{V}$, $f=1\text{MHz}$ (Any I/O to ground)		0.30	0.40	pF

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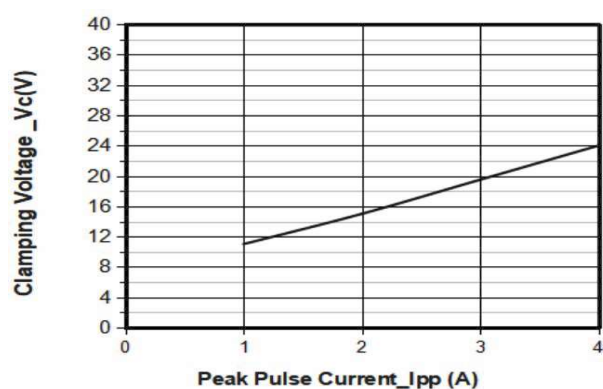
Rating and characteristic curves



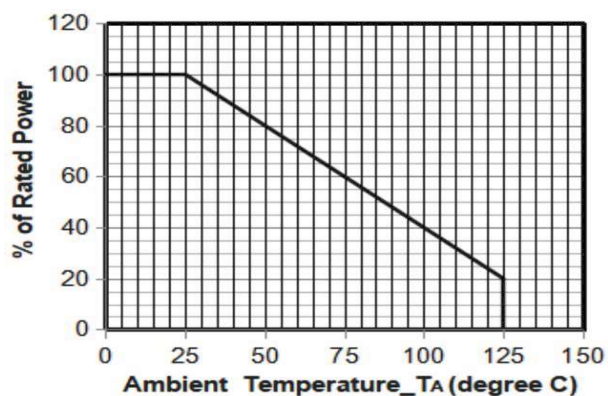
Junction Capacitance vs. Reverse Voltage



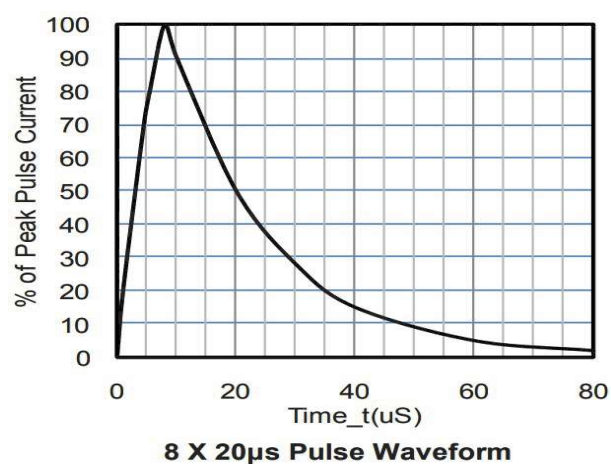
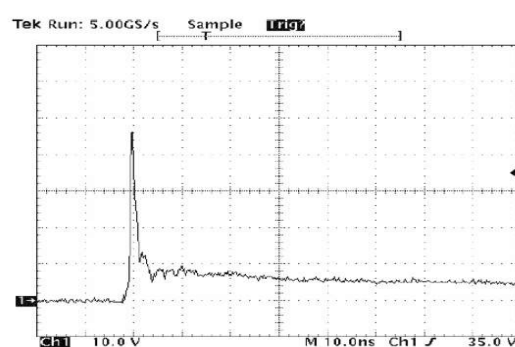
Peak Pulse Power vs. Pulse Time



Clamping Voltage vs. Peak Pulse Current



Power Derating Curve

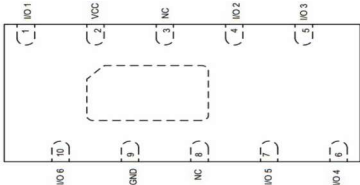
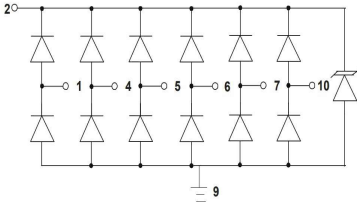
8 X 20 μ s Pulse Waveform

Note: Data is taken with a 10x attenuator
ESD Clamping Voltage

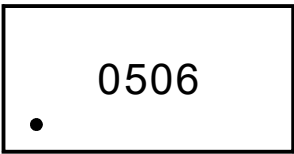
8 kV Contact per IEC61000-4-2

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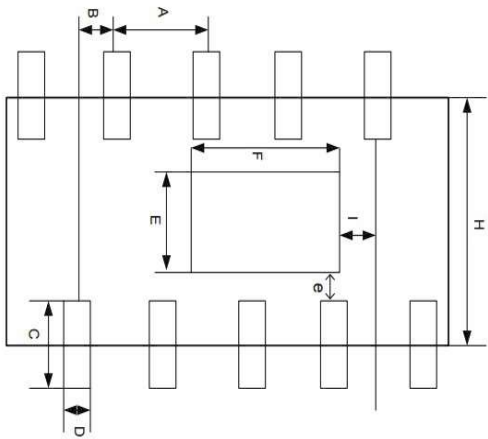
Pinning information

Pin Configuration	Simplified outline	Circuit Diagram
I/O Lines : 1, 4, 5, 6, 7, 10 NC : 3, 8 VCC : 2 Ground : 9		

Marking



Suggested solder pad layout

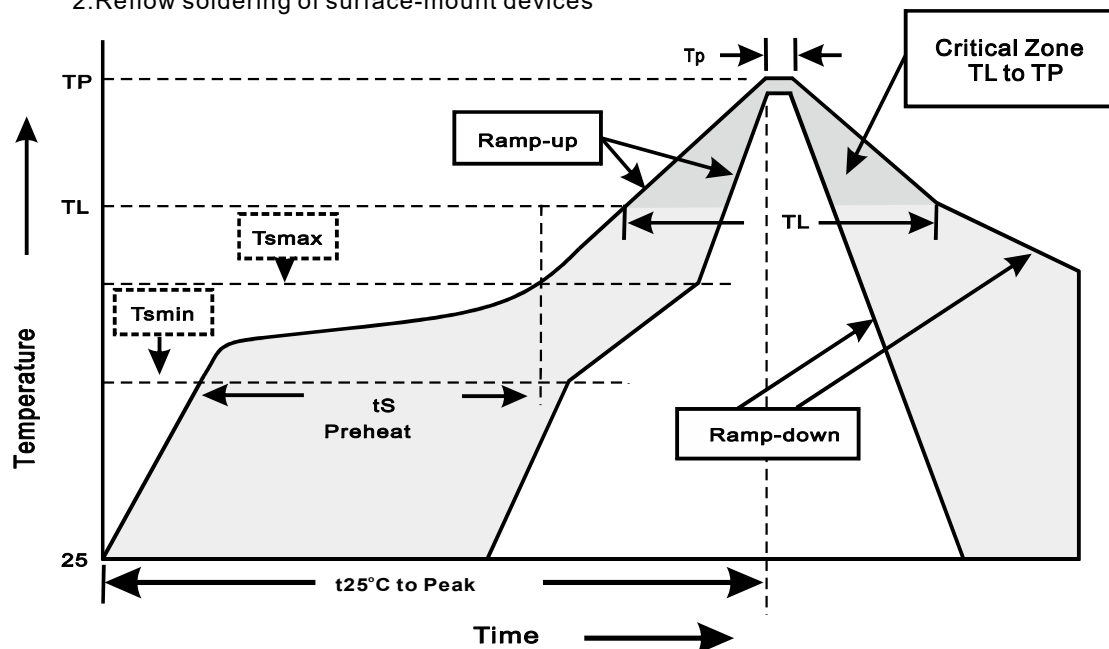


SYM	DIMENSIONS	
	MILLIMETERS	INCHES
A	0.800	0.032
B	0.400	0.016
C	0.600	0.024
D	0.200	0.008
E	0.800	0.032
F	1.400	0.056
H	2.000	0.080
I	0.300	0.012
e	0.200	0.008

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Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smin}) -Temperature Max(T _{smax}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smax} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _p)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes