

LL054BT2510-1

List

List.....	1
Package outline.....	2
Features.....	2
Mechanical data.....	2
Maximum ratings	2
Electrical characteristics.....	2
Rating and characteristic curves.....	3
Pinning information.....	4
Marking.....	4
Suggested solder pad layout.....	4
Packing information.....	5
Reel packing.....	6
Suggested thermal profiles for soldering processes.....	6
High reliability test capabilities.....	7

LL054BT2510-1

4-Channel Ultra Low Capacitance ESD Protection Diodes Array 5.0V

Features

- Solid-state silicon-avalanche technology
- Low operating and clamping voltage
- Up to four I/O line of protection
- Ultra low capacitance : 0.3pF typical (I/O to I/O)
- IEC61000-4-2 (ESD) $\pm 22\text{kV}$ (Contact), $\pm 25\text{kV}$ (Air)
- IEC61000-4-2 (EFT) 40A (5/50ns)
- IEC61000-4-5 (Lightning) 4.5A (8/20 μs)
- Low leakage
- Low operating voltage 5V
- Flow - through design
- RoHS compliant
- Suffix "-H" indicates Halogen-free parts, ex. LL054BT2510-1-H

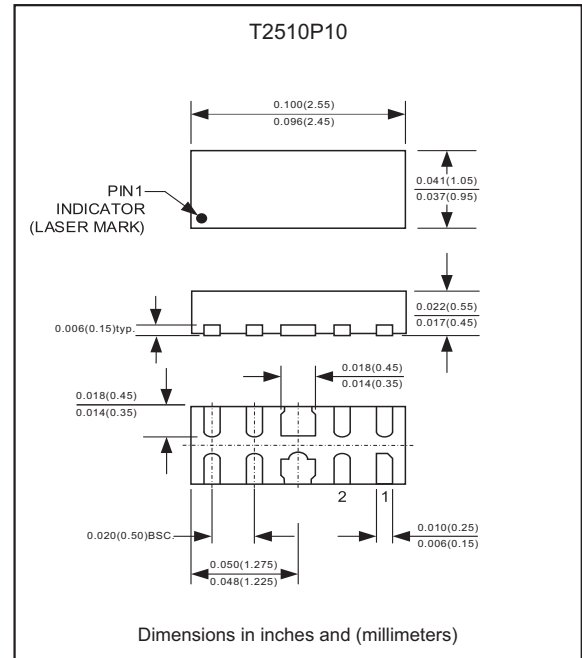
Applications

- Digital visual interface
- MDDI ports
- Display port TM interface
- PCI express
- High definition multi - media interface (HDMI)
- eSATA Interfaces

Mechanical data

- Flammability Rating: UL 94V-0
- Terminal: Matte tin plated
- Case : Molded plastic, T2510P10
- Mounting Position : Any
- Weight : 3.6 Milligrams (Approximate)

Package outline



Maximum ratings (at $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak pulse power ($t_p=8/20\mu\text{s}$)	PPP	68	W
Peak pulse current ($t_p=8/20\mu\text{s}$)	I _{PP}	4.5	A
ESD per IEC 61000-4-2 (Contact)	V _{ESD}	± 22	kV
ESD per IEC 61000-4-2 (Air)		± 25	
Operating junction temperature range	T _J	-55 to +125	$^\circ\text{C}$
Storage temperature range	T _{STG}	-55 to +150	$^\circ\text{C}$

Electrical characteristics (at $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Reverse stand-off voltage	Any I/O pin to ground	V _{RWM}			5.0	V
Reverse breakdown voltage	I _T =1mA, Any I/O pin to ground	V _{BR}	6.0			V
Reverse leakage current	V _{RWM} =5V, Any I/O pin to ground	I _R			0.5	μA
Clamping voltage	I _{PP} =1A, $t_p=8/20\mu\text{s}$ Any I/O pin to ground	V _C			9	V
	I _{PP} =4.5A, $t_p=8/20\mu\text{s}$ Any I/O pin to ground				15	
Dynamic resistance (Note 1,2)	T _L P=0.2/100ns	R _{DYN}		0.5		Ω
ESD Clamping voltage (Note 1)	I _{PP} =4A, $t_p=0.2/100\text{ns}$ (T _L P)	V _C		10		V
	I _{PP} =16A, $t_p=0.2/100\text{ns}$ (T _L P)			16		
Junction capacitance	V _R =0V, f=1MHz, I/O pin to GND	C _J			0.8	pF
	V _R =0V, f=1MHz, Between I/O pins			0.3	0.4	

Notes:

1. T_LP Setting: $t_p=100\text{ns}$, $t_r=0.2\text{ns}$, I_{TLP} and V_{TLP} sample window: $t_1=70\text{ns}$ to $t_2=90\text{ns}$
2. Dynamic resistance calculated from I_{PP}=4A to I_{PP}=16A using "Best Fit"

Rating and characteristic curves(LL054BT2510-1)

Fig.1 Peak Pulse Power vs. Pulse Time

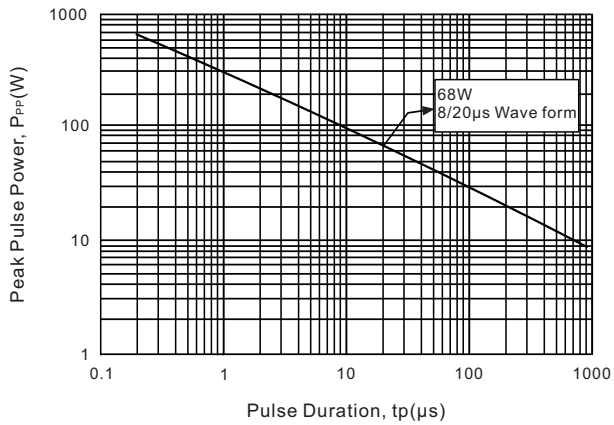


Fig.2 Power Derating Curve

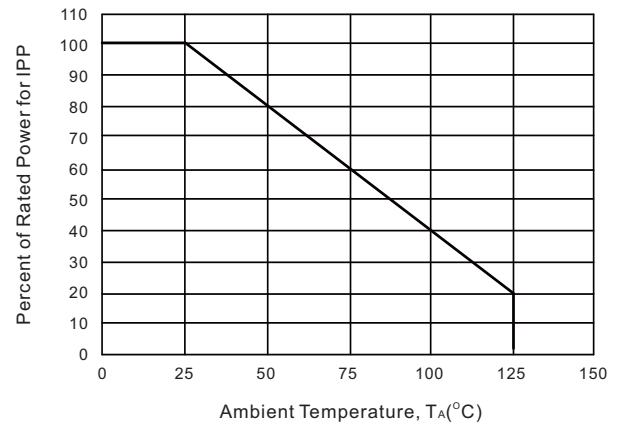


Fig.3 Clamping Voltage vs. Peak Pulse Current

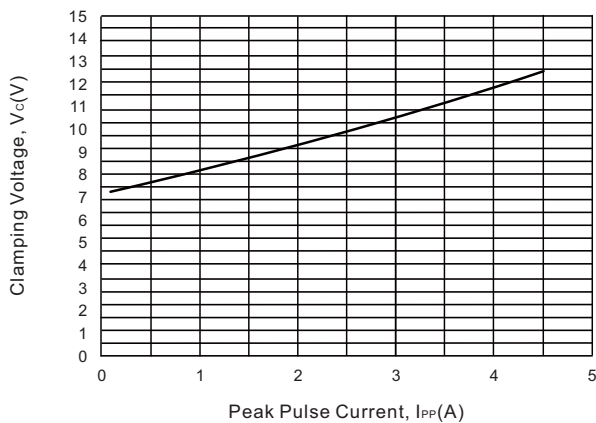


Fig.4 Normalized Junction Capacitance vs Reverse Voltage

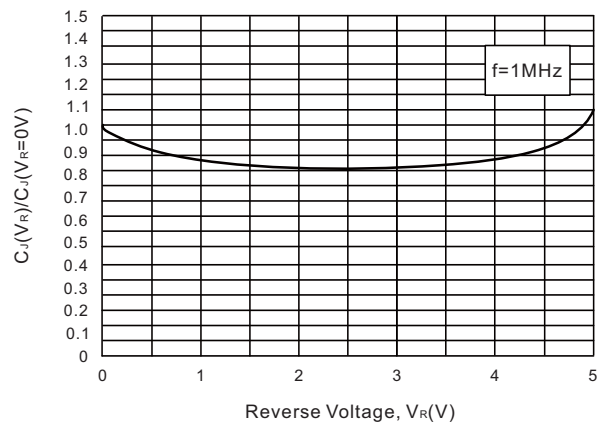


Fig.5 Pulse Waveform

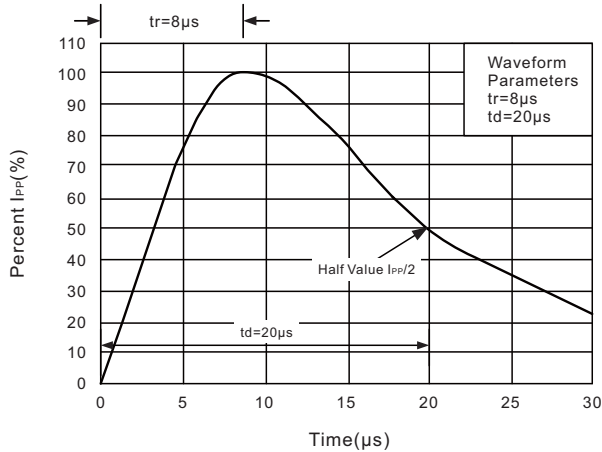
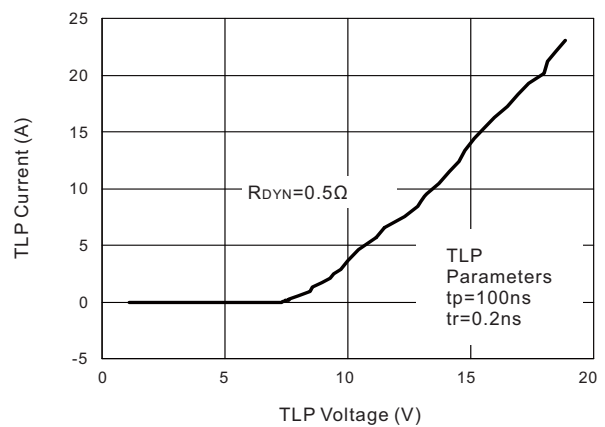


Fig.6 TLP I-V Curve



LL054BT2510-1

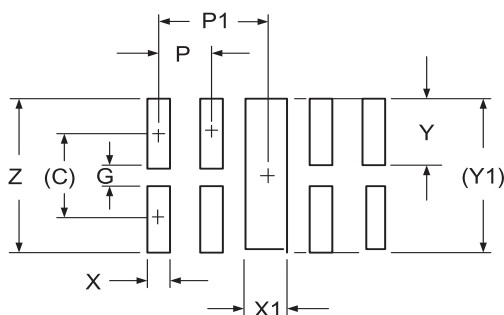
Pinning information

Pin	Simplified outline	Symbol
1,2,4,5 Input Lines 6,7,9,10 Out Lines (No Internal Connection) 3,8 Ground		

Marking

Type number	Marking code
LL054BT2510-1	

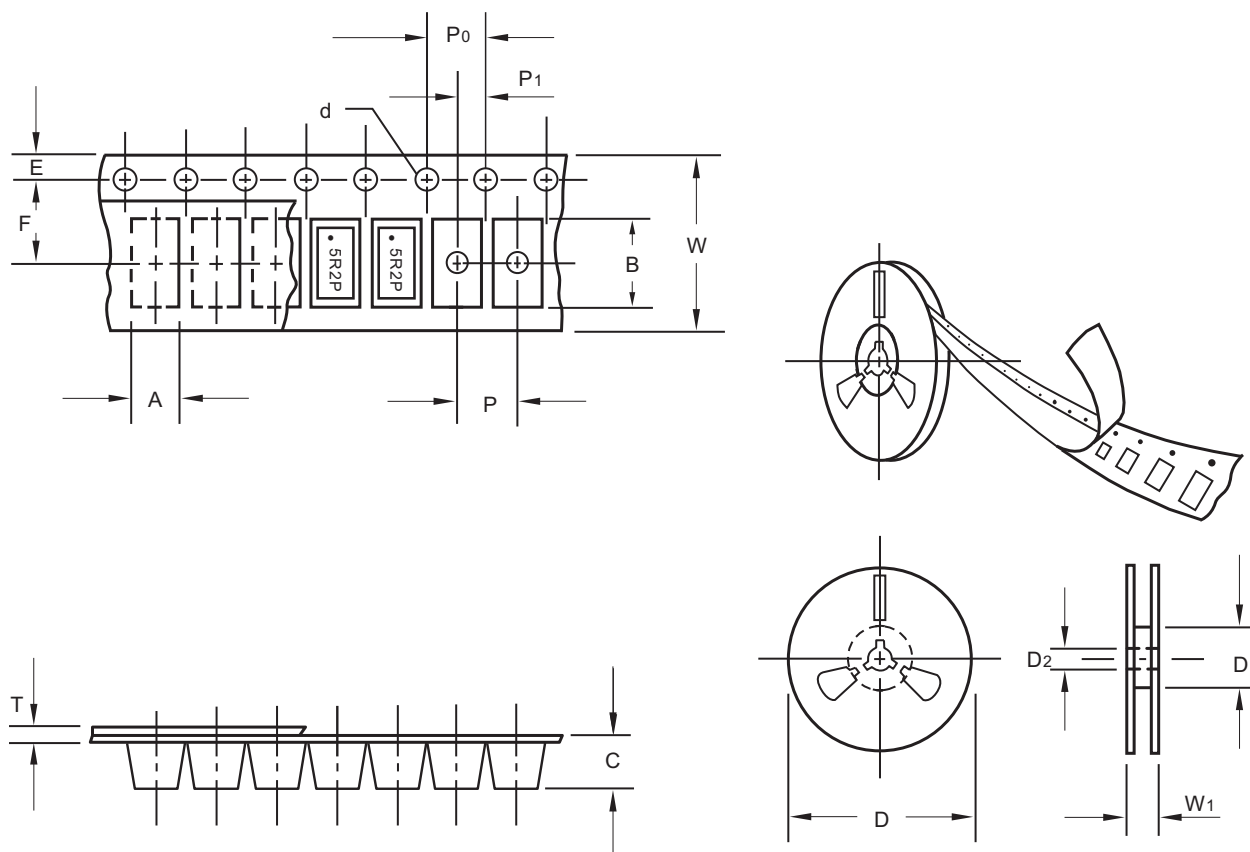
Suggested solder pad layout



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.034)	(0.875)
G	.008	0.20
P	.020	0.50
P1	.039	1.00
X	.010	0.25
X1	.018	0.45
Y	.027	0.675
Y1	(.061)	(1.55)
Z	.061	1.55

LL054BT2510-1

Packing information



unit:mm

Item	Symbol	Tolerance	T2510P10
Carrier width	A	0.05	1.20
Carrier length	B	0.05	2.70
Carrier depth	C	0.05	0.70
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	60.00
Feed hole diameter	D2	0.2	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.05	2.00
Overall tape thickness	T	0.1	0.20
Tape width	W	0.3	8.00
Reel width	W1	1.0	13.1

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

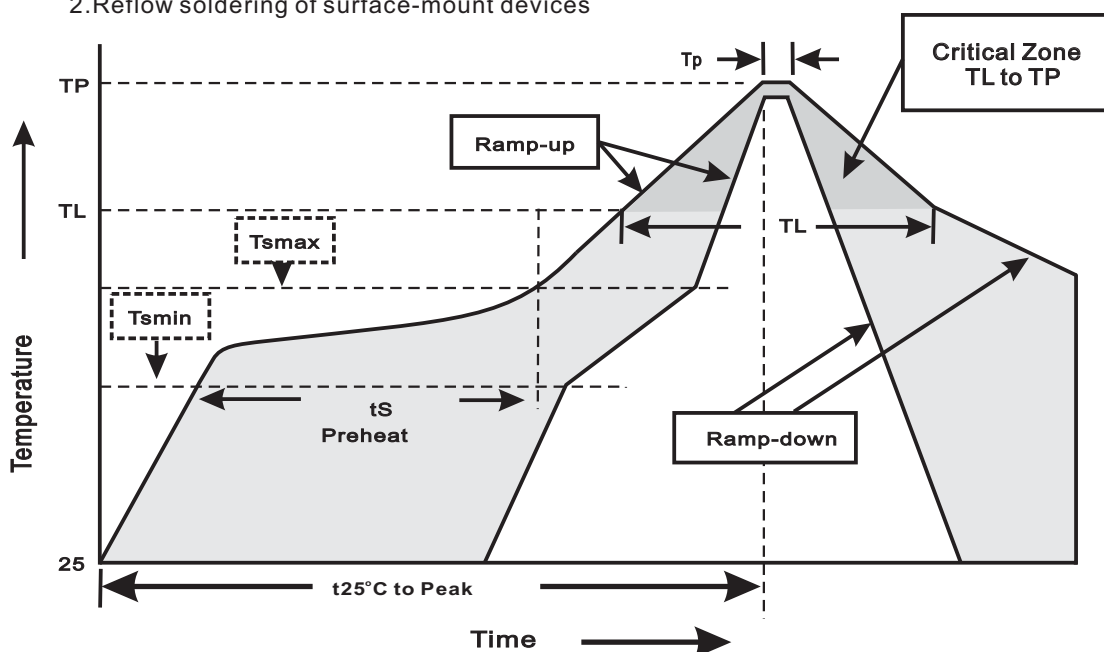
LL054BT2510-1

Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
T2510P10	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smmin}) -Temperature Max(T _{smmax}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smmax} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes

LL054BT2510-1

High reliability test capabilities

Item Test	Conditions	Reference
1. Solder Resistance	at $260 \pm 5^{\circ}\text{C}$ for $10 \pm 2\text{sec.}$	MIL-STD-750D METHOD-2031
2. Solderability	at $245 \pm 5^{\circ}\text{C}$ for 5 sec.	MIL-STD-202F METHOD-208
3. High Temperature Reverse Bias	$V_{\text{BR}} = V_{\text{BR MIN}} * 80\%$ at $T_{\text{J}} = 125^{\circ}\text{C}$ for 168 hrs.	MIL-STD-750D METHOD-1038
4. Pressure Cooker	$15P_{\text{SIG}}$ at $T_{\text{A}} = 121^{\circ}\text{C}$ for 4 hrs.	JESD22-A102
5. Temperature Cycling	-55°C to $+125^{\circ}\text{C}$ dwelled for 30 min. and transferred for 5min. total 10 cycles.	MIL-STD-750D METHOD-1051
6. Humidity	at $T_{\text{A}} = 85^{\circ}\text{C}$, RH=85% for 1000hrs.	MIL-STD-750D METHOD-1021
7. High Temperature Storage Life	at 175°C for 1000 hrs.	MIL-STD-750D METHOD-1031