LL053BT1210

List

LL053BT1210

2-Channel Ultra Low Capacitance ESD Protection Diodes Array 5.0V

Features

- Ultra-small package (1.2mm x 1.0mm x 0.50mm).
- Protects two data lines.
- Low capacitance : 0.2pF Typical (I/O to GND)
- IEC61000-4-2 (ESD) ±25KV(Air), ±17KV(Contact)
- IEC61000-4-2 (EFT) 40A (5/50ns)
- Cable discharge event (CDE).
- Low leakage current : 0.1μA @V_{RWM} (Typical)
- Each I/O pin can withstand over 1000 ESD strikes for ±8KV contact discharge.
- RoHS compliant.
- Suffix "-H" indicates Halogen-free parts, ex. LL053BT1210-H.

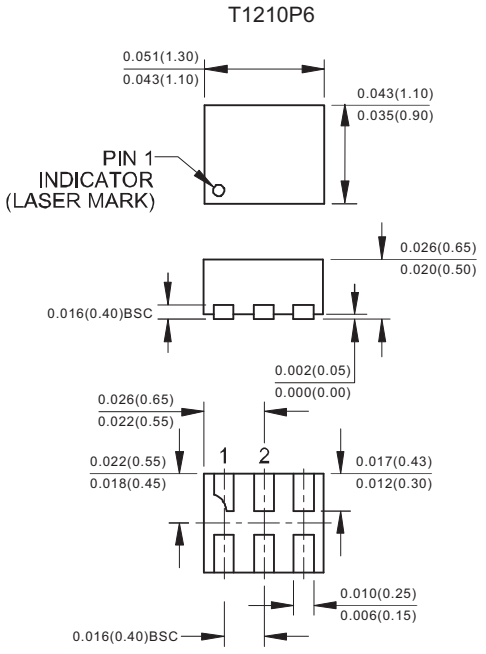
Applications

- Serial ATA.
- PCI Express.
- USB2.0 and data line protection.
- High definition multi-media interface (HDMI).

Mechanical data

- Flammability Rating: UL 94V-0.
- Terminal: Matte tin plated.
- Case : Molded plastic, T1210P6.
- Mounting Position : Any.

Package outline



Dimensions in inches and (millimeters)

Maximum ratings (at T_A=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak pulse power (tp=8/20μs)	P_{PP}	60	W
Peak pulse current (tp=8/20μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±17	KV
ESD per IEC 61000-4-2 (Air)		±25	
Operating temperature	T_{OPT}	+125	℃
Storage temperature	T_{STG}	-55 to +150	℃

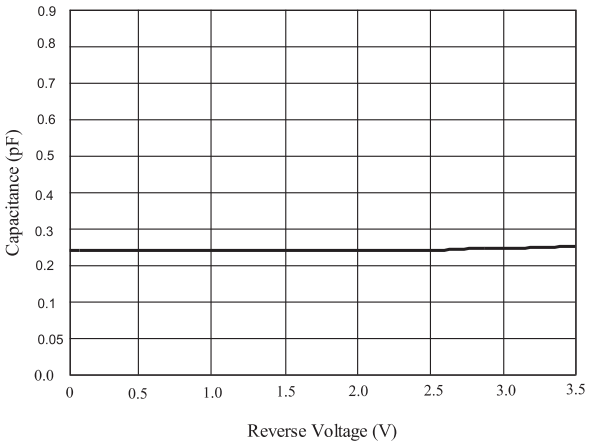
Electrical characteristics (at T_A=25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Reverse stand-off voltage		V_{RWM}			5.0	V
Reverse leakage current	V_{RWM}=5.0V	I_R		0.1	1.0	μA
Reverse Breakdown voltage	I_T=1mA	V_{BR}	6.0		9.0	V
Clamping voltage	I_{PP}=5A, t_p=8/20μs (I/O and GND)	V_C			12	V
Junction capacitance	V_R=0V, f=1MHz, (I/O and GND)	C_{ESD}		0.2	0.5	pF

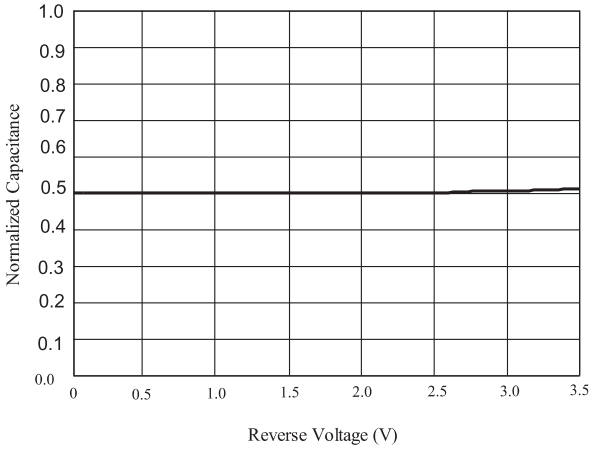
Note : 1. Measurements performed using a 100ns transmission line pulse (TLP) system.

Rating and characteristic curves(LL053BT1210)

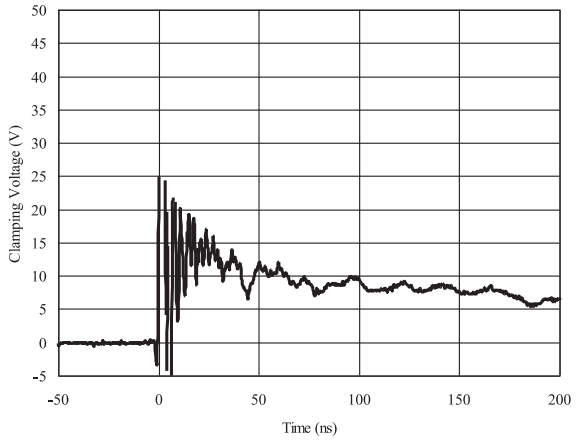
Capacitance *vs.* Reverse Voltage



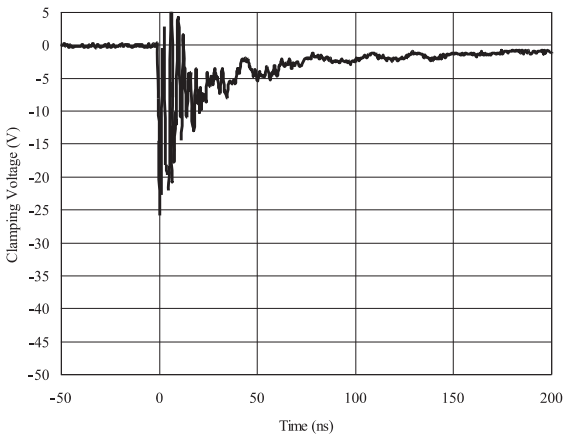
Normalized Capacitance *vs.* Reverse Voltage



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



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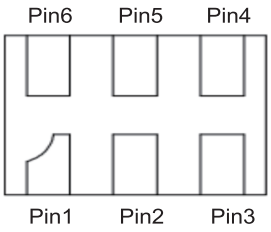
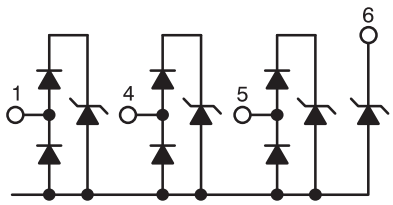
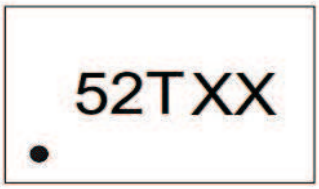
Pinning information

Pin Configuration	Simplified outline	Circuit Diagram
1 GND 2, 3, NC 4, 5 I/O Line 6 VCC		

Marking

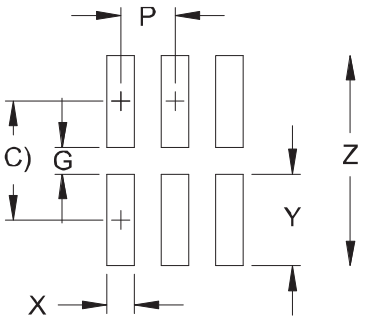


Note:

(1) " 52T " is part number, fixed.

(2) "XX" is the internal code.

Suggested solder pad layout



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.034)	(0.875)
G	.008	0.20
P	.016	0.40
X	.008	0.20
Y	.027	0.675
Z	.061	1.55

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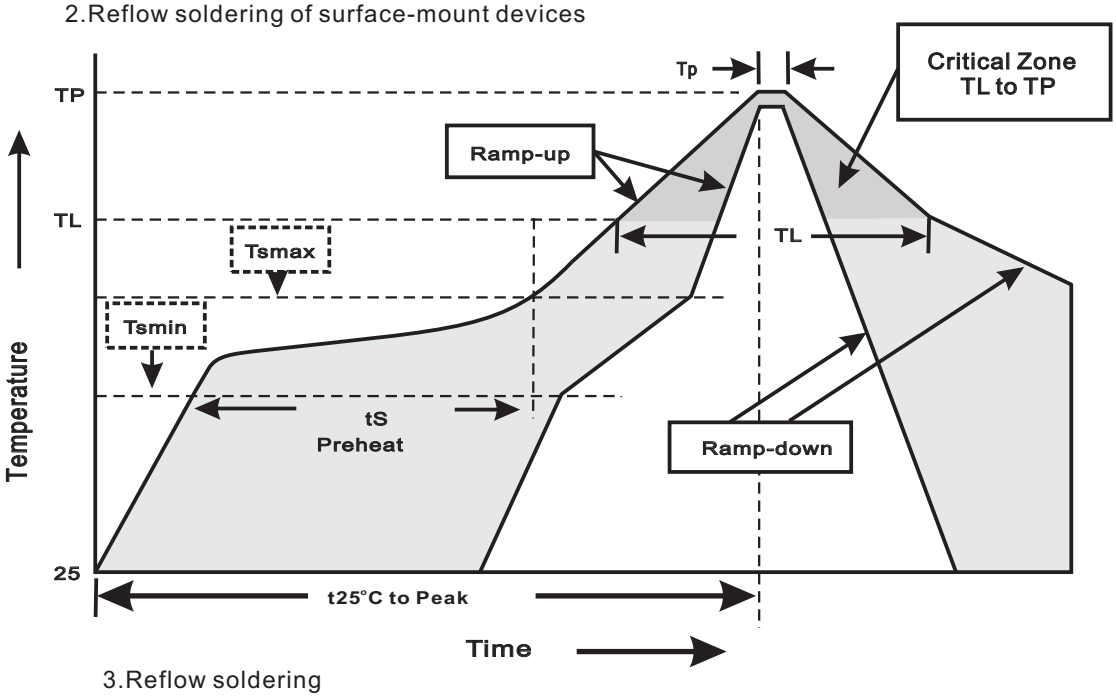
Suggested thermal profiles for soldering processes

1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	<3°C/sec
Preheat -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time(min to max)(t_s)	 150°C 200°C 60~120sec
Tsmax to T_L -Ramp-upRate	 <3°C/sec
Time maintained above: -Temperature(T_L) -Time(t_L)	 217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes