L702BT143

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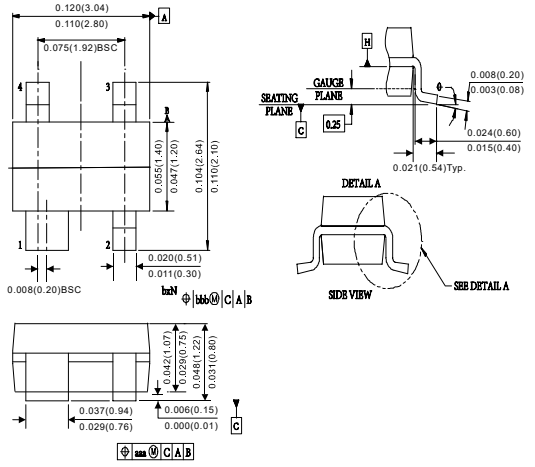
Low Capacitance ESD Protection Diodes Array

Features

- Transient protection for high speed data lines to
  – IEC 61000-4-2 (ESD) immunity test Air discharge: ±15kV, Contact discharge: ±8kV.
  – IEC61000-4-4 (EFT) 40A (5/50ns).
  – IEC61000-4-5 (Lightning)1kV, 21A (8/20μs).
- Array of surge rated, low capacitance diodes.
- Protects two I/O lines.
- Low capacitance (1.5pF typical) for high-speed interfaces.
- Low clamping voltage.
- Suffix "-H" for Halogen-free part, ex. L702BT143-H.

Package outline

SOT-143



Dimensions in inches and (millimeters)

Applications

- ADSL Lines.
- I²C BUS Protection.
- Video Line Protection.
- T1/E1 secondary IC Side Protection.
- WAN/LAN Equipment.

Mechanical data

- Epoxy : UL94-V0 rated flame retardant.
- Case : Molded plastic, SOT-143.
- Lead Finish : Lead free.
- Mounting Position : Any.
- Weight : Approximated 0.010 gram.

Absolute maximum ratings (At T_A=25°C, RH=45% ~ 75%, unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Peak pulse current (t_p=8/20μs)	I_{PP}	21	A
ESD per IEC 61000-4-2 (Air discharge)	ESD	±15	KV
ESD per IEC 61000-4-2 (Contact discharge)		±8	KV
Operating junction temperature range	T_J	-55 ~ 125	℃
Storage temperature range	T_{STG}	-55 ~ 150	℃

Electrical characteristics (At T_A=25°C, unless otherwise noted)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Reverse working voltage	V_{RWM}				70	V
Punch-trough voltage	V_{BR}	I_T=50μA	85			V
Reverse leakage current	I_R	V_{RWM}=70V			0.5	μA
Clamping voltage-1	V_{c1}	I_{PP}=1A, t_p=8/20μs			3.0	V
Clamping voltage-2	V_{c2}	I_{PP}=10A, t_p=8/20μs			9.0	V
Clamping voltage-3	V_{c3}	I_{PP}=10A, t_p=8/20μs			16.0	V
Junction capacitance	C_{j1}	V_R=0V, f=1MHz (Between I/O pins and ground)		1.5		pF
Junction capacitance	C_{j2}	V_R=0V, f=1MHz (Between I/O pins)		1.0		pF

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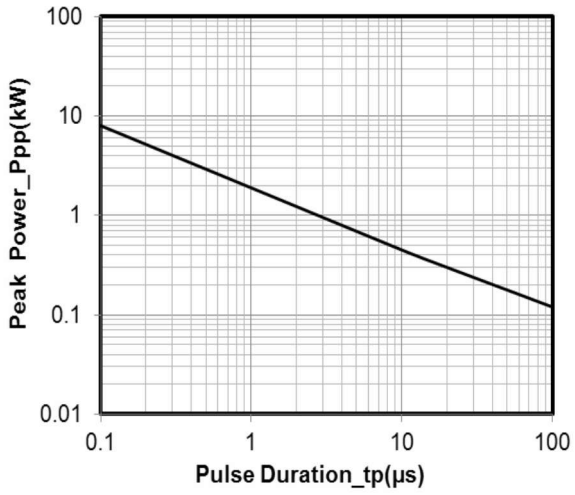
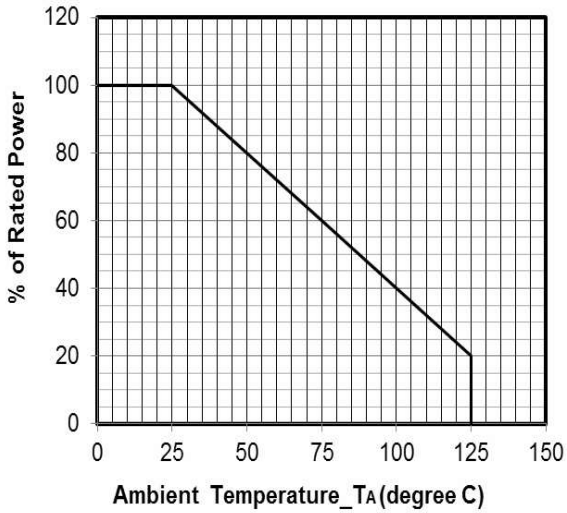
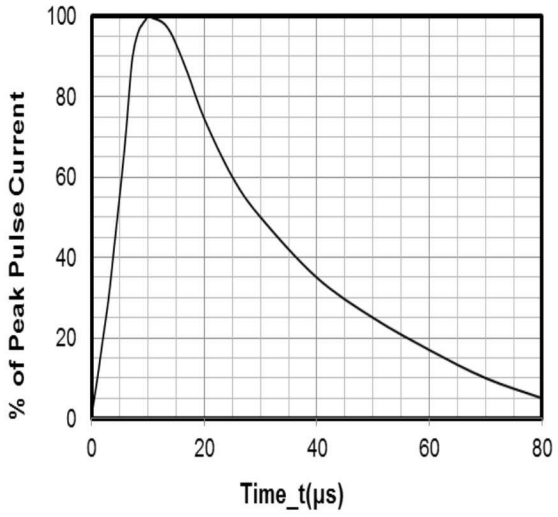
Rating and characteristic curves



Peak Pulse Power vs. Pulse Time



Power Derating Curve



8 X 20μs Pulse Waveform

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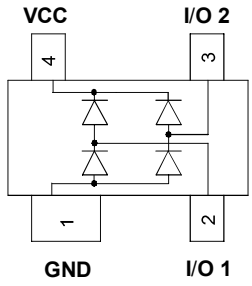
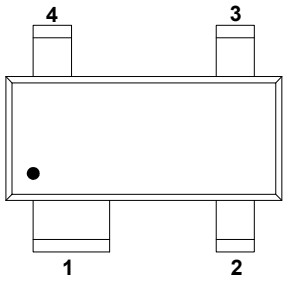
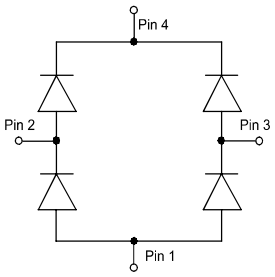
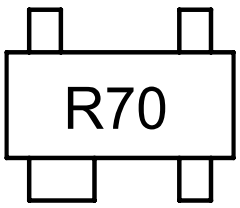
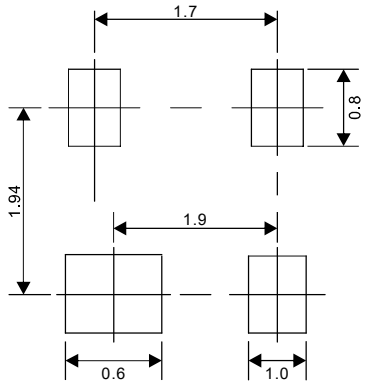
Pinning information

Pin Configuration	Simplified outline	Circuit Diagram
		

Marking

Type number	Marking code
L702BT143	

Suggested solder pad layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: 0.05mm.
3. The pad layout is for reference purposes only.

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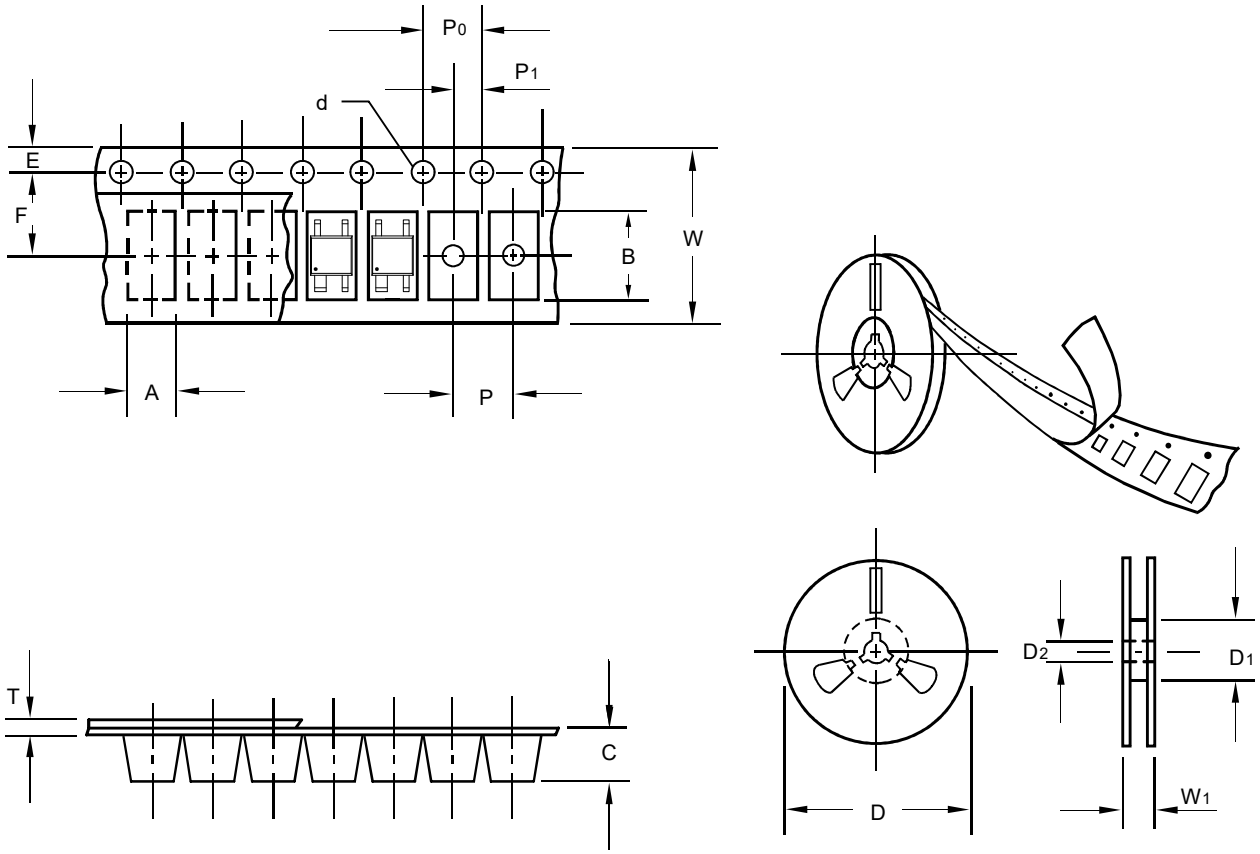
Packing information



unit:mm

Item	Symbol	Tolerance	SOT-143
Carrier width	A	0.1	3.19
Carrier length	B	0.1	2.80
Carrier depth	C	0.1	1.31
Sprocket hole	d	0.1	1.50
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D_1	min	54.40
Feed hole diameter	D_2	0.2	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P_0	0.1	4.00
Embossment center	P_1	0.1	2.00
Overall tape thickness	T	0.1	0.22
Tape width	W	0.3	8.00
Reel width	W_1	1.0	9.50

Note:Devices are packed in accor dance with EIA standar RS-481-A and specifications listed above.

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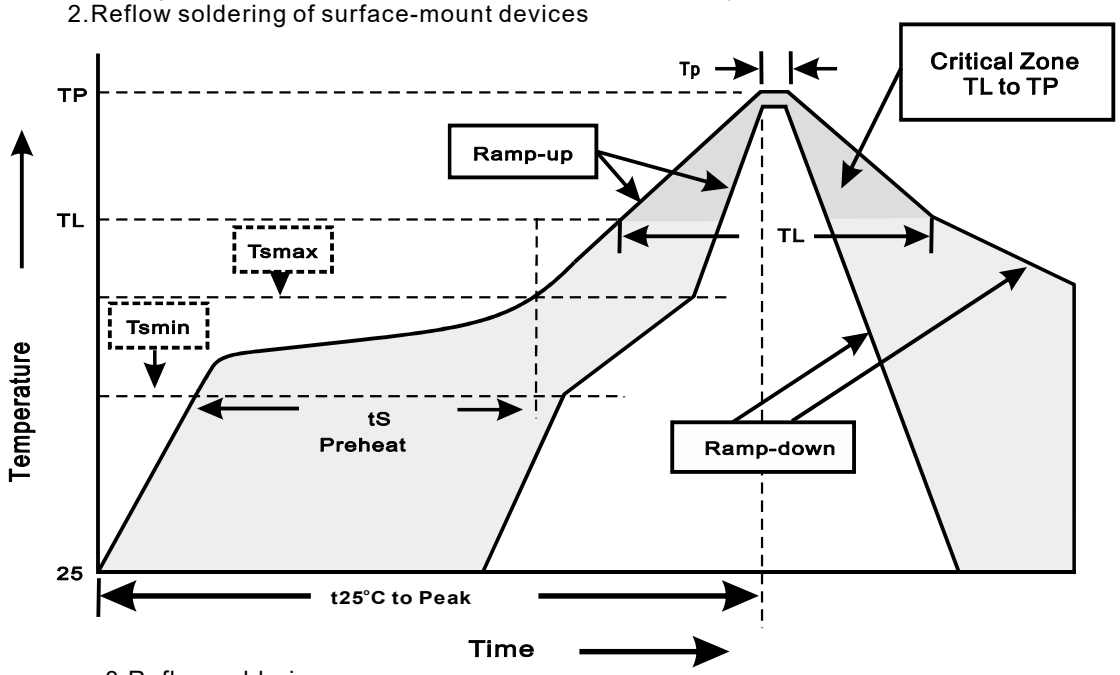
Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
SOT-143	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000

Suggested thermal profiles for soldering processes

1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	<3°C/sec
Preheat -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time(min to max)(t_s)	 150°C 200°C 60~120sec
Tsmax to T_L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T_L) -Time(t_L)	 217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes