

L054AT553

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50W TVS Diode Array For ESD And Latch -Up Protection

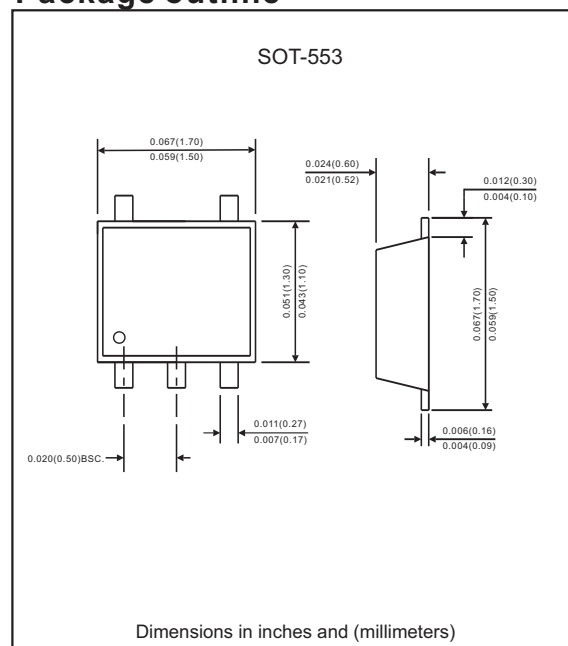
Features

- Protects four I/O lines
- Low capacitance
- IEC61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
- IEC61000-4-4 (EFT) 40A (5/50ns)
- Low operating and clamping voltages
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen free parts, ex. L054AT553-H.

Mechanical data

- Molding compound flammability rating : UL 94V-0.
- Pb-Free, Halogen Free, RoHS/WEEE compliant.
- Case : Molded plastic, T0603
- Terminals : Solder plated, solder able per J-STD-002.
- Polarity : Indicated by cathode band.
- Mounting Position : Any.
- Weight : Approximated 3milligrams.

Package outline



Maximum ratings (At $T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Peak pulse power dissipation at $t_p = 8/20\mu\text{s}$ waveform	P_{PP}	50	W
Peak pulse current ($t_p = 8/20\mu\text{s}$)	I_{PP}	2.5	A
ESD per IEC 61000-4-2 (Air discharge)	ESD	± 15	KV
ESD per IEC 61000-4-2 (Contact discharge)		± 8	KV
Lead soldering temperature	T_L	260 (10 sec.)	$^\circ\text{C}$
Operating junction temperature range	T_J	150	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 ~ 150	$^\circ\text{C}$

Electrical characteristics (At $T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Test condition	Symbol	Min.	Typ.	Max.	Unit
Nominal reverse working voltage		V_{RWM}			5.0	V
Reverse breakdown voltage	$I_T = 1\text{mA}$	V_{BR}	6.0			V
Reverse leakage current	$V_{RWM} = 5\text{V}$	I_R			0.1	μA
Diode forward voltage	$I_F = 15\text{mA}$	V_F		0.85	1.2	V
Clamping voltage	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$	V_C			10	V
	$I_{PP} = 2.5\text{A}$, $t_p = 8/20\mu\text{s}$				13	V
Peak pulse current	$t_p = 8/20\mu\text{s}$	I_{PP}			2.5	A
Parasitic capacitance	$V_R = 0\text{V}$, $f = 1\text{MHz}$ (I/O - GND)	C_{ESD}		8		pF

Rating and characteristic curves (L054AT553)

Fig.1 Pulse Waveform

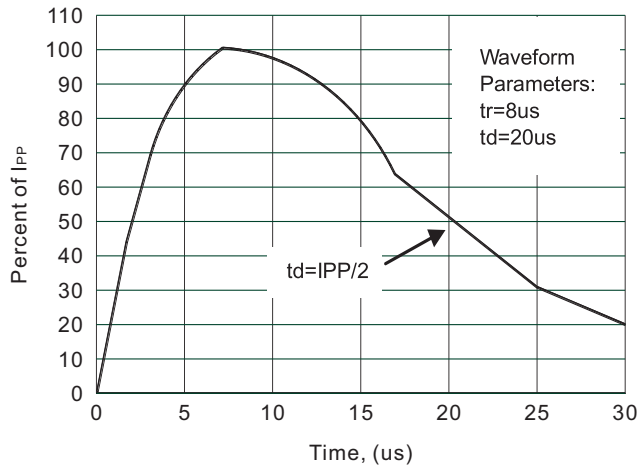


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse time

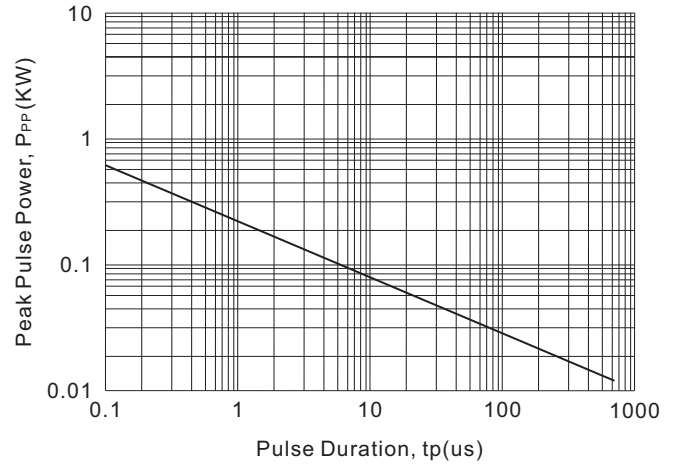


Fig.3 Power Derating Curve

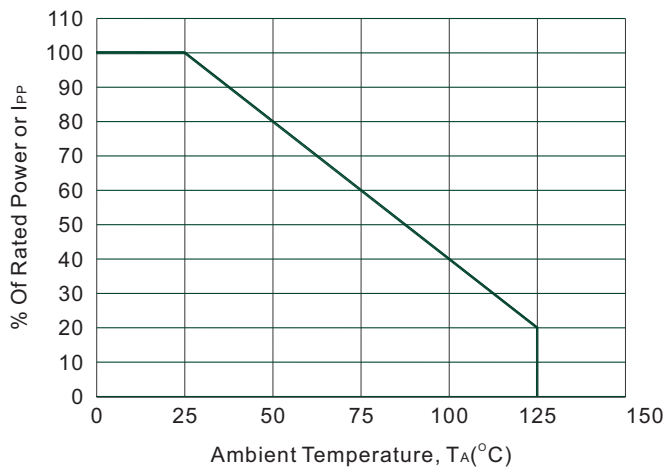
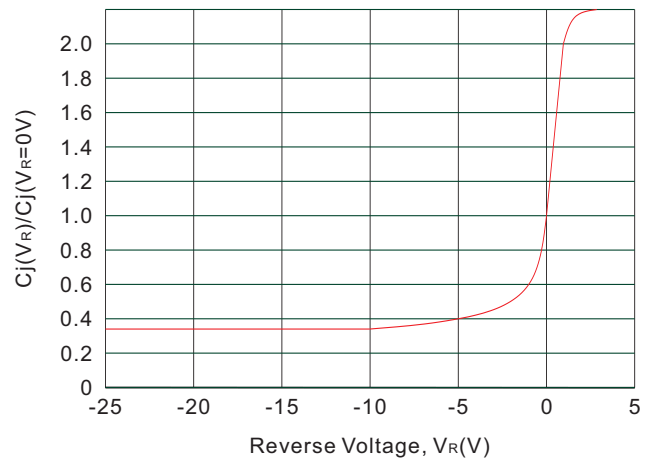
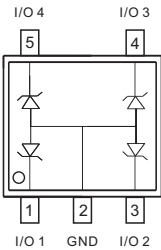


Fig.4 Junction Capacitance vs. Reverse Voltage

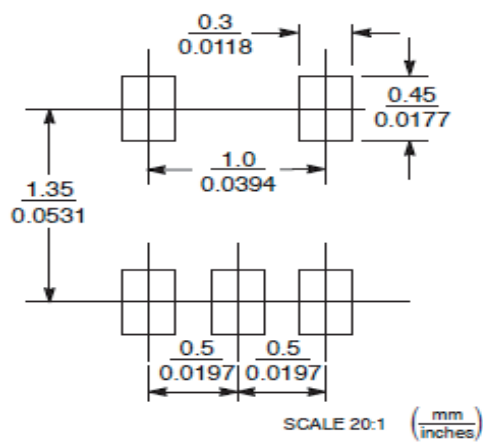


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Pinning and Marking information

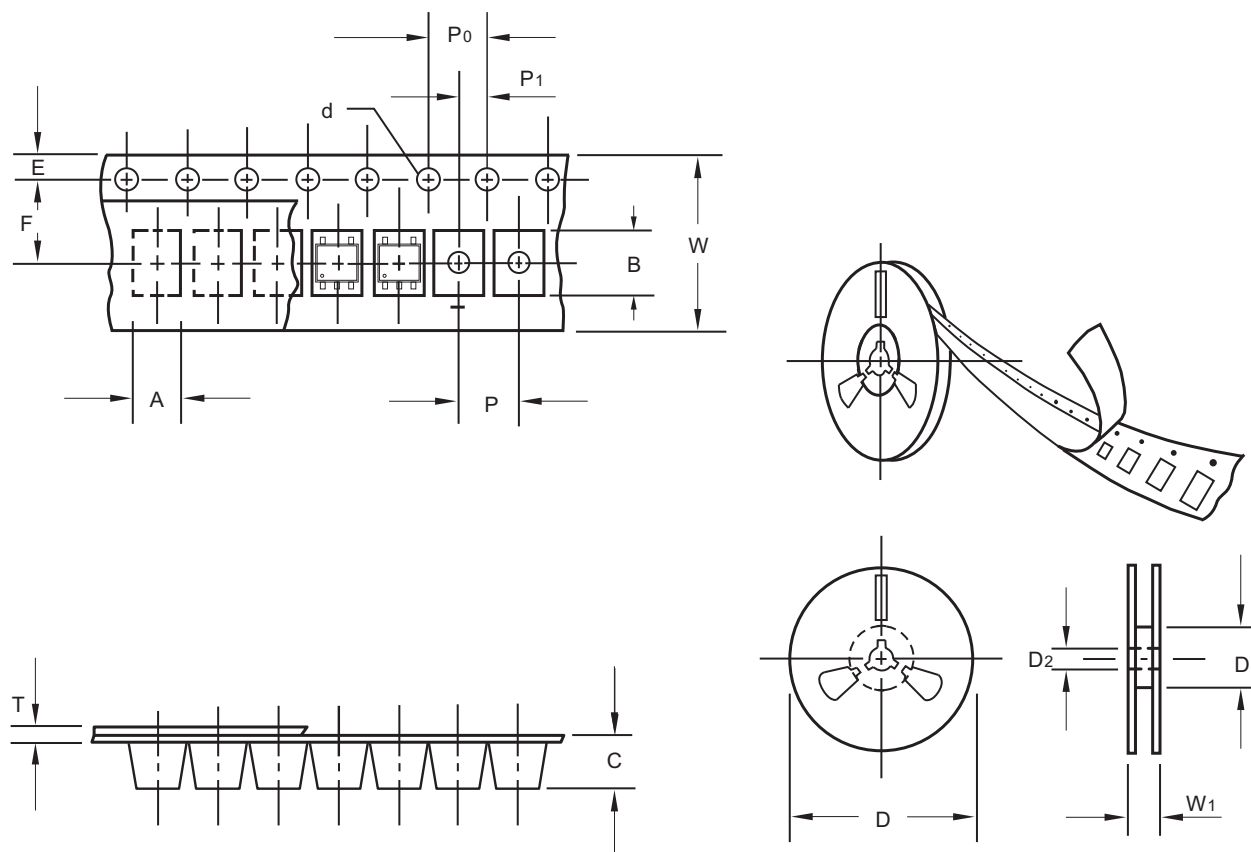
Pin	Simplified outline	Marking
Uni-Directional		E5T, U5

Suggested solder pad layout



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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-553
Carrier width	A	0.1	1.78
Carrier length	B	0.1	1.78
Carrier depth	C	0.1	0.69
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	62.00
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W1	1.0	12.30

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

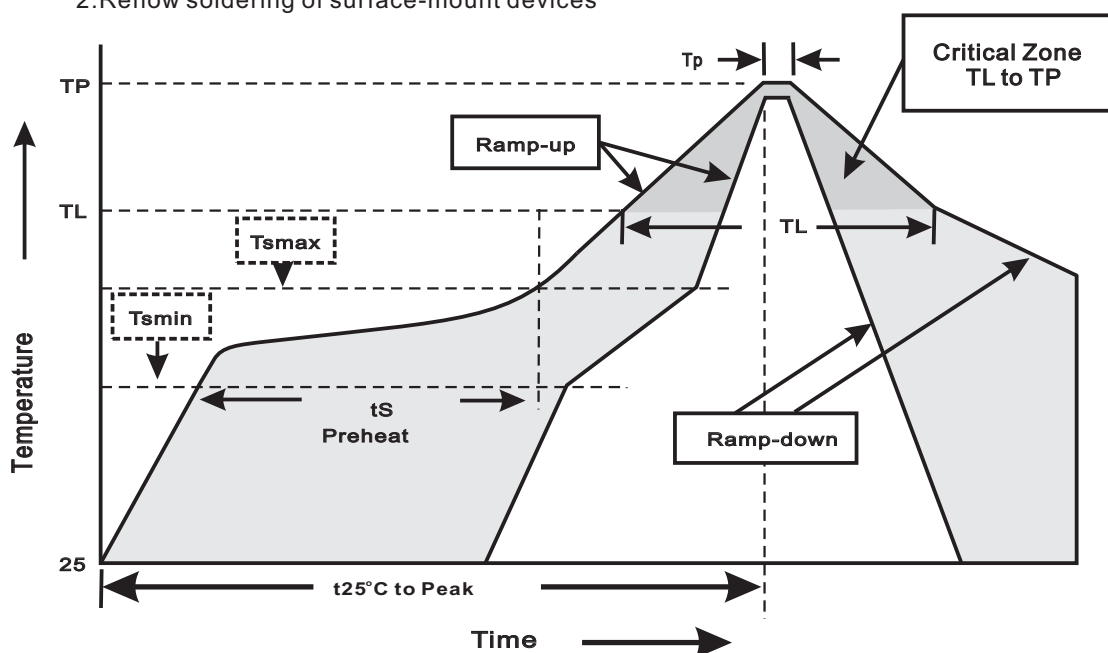
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
SOT-553	7"	3,000	4.0	30,000	183*123*183	178	383*257*387	240,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smin}) -Temperature Max(T _{smax}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smax} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(tp)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes