

FMBTRA107SS

List

List.....	1
Package outline.....	2
Features.....	2
Mechanical data.....	2
Maximum ratings	2
Electrical characteristics.....	2
Rating and characteristic curves.....	3
Pinning information.....	4
Marking.....	4
Suggested solder pad layout.....	4
Suggested thermal profiles for soldering processes.....	5

FMBTRA107SS

PNP Silicon Epitaxial Planar Digital Transistor

Features

- With built-in bias resistors.
- Simplify circuit design.
- Reduce a quantity of parts and manufacturing process.
- We declare that the material of product compliance with RoHS requirements.
- Suffix "-H" indicates Halogen free parts, ex. FMBTRA107SS-H.

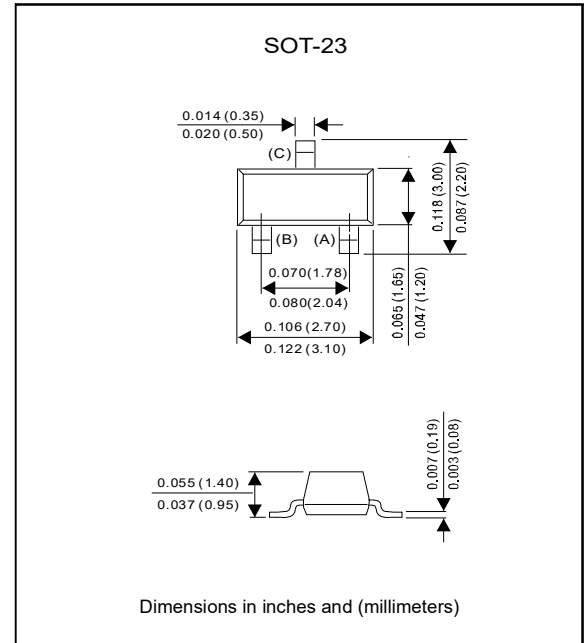
Applications

- Inverter, Interface, Driver

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-23
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.008 gram

Package outline



Maximum ratings (At $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Output voltage	$-V_o$	50	V
Input voltage	V_i	-30 to +6	V
Output current	$-I_o$	100	mA
Total power dissipation	P_{tot}	200	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 to +150	$^\circ\text{C}$

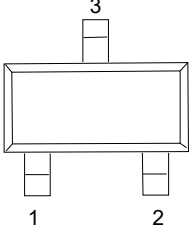
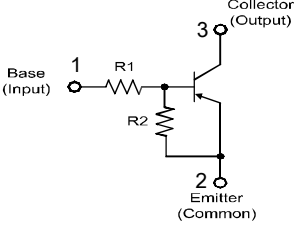
Electrical characteristics (At $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
DC current gain	$-V_o=5\text{V}$, $-I_o=10\text{mA}$	h_{FE}	80			
Output cutoff current	$-V_o=50\text{V}$	$-I_{O(OFF)}$			500	nA
Input current	$-V_i=5\text{V}$	$-I_i$			0.88	mA
Output voltage	$-I_o=10\text{mA}$, $-I_i=0.5\text{mA}$	$-V_{O(ON)}$			0.3	V
Input on voltage (ON)	$-V_o=0.2\text{V}$, $-I_o=5\text{mA}$	$-V_{I(ON)}$			1.8	V
Input off voltage (OFF)	$-V_o=5\text{V}$, $-I_o=0.1\text{mA}$	$-V_{I(OFF)}$	0.5			V
Transition frequency	$-V_o=10\text{V}$, $-I_o=5\text{mA}$	$f_T^{(1)}$		200		MHZ
Input resistance		R_1	7	10	13	K Ω
Resistance ratio		R_1 / R_2	0.17		0.25	

(1)Characteristic of transistor only.

FMBTRA107SS

Pinning information

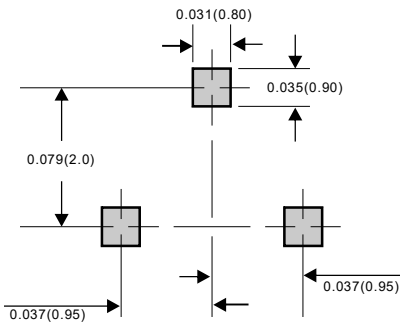
Pin	Simplified outline	Symbol
Pin1 Base Pin2 Emitter Pin3 Collector		

Marking and resistor values

Type number	Marking code
FMBTRA107SS	C7S

Suggested solder pad layout

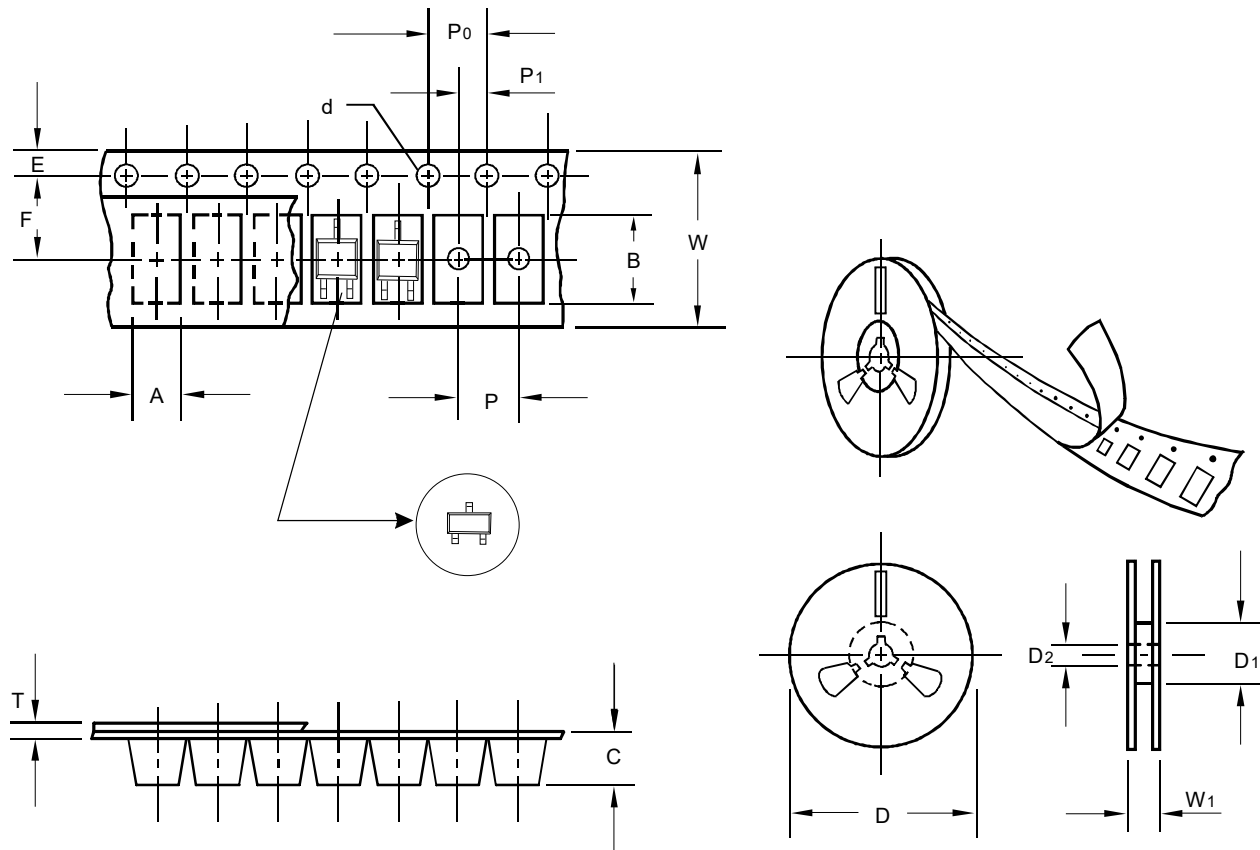
SOT-23



Dimensions in inches and (millimeters)

FMBTRA107SS

Packing information



unit:mm

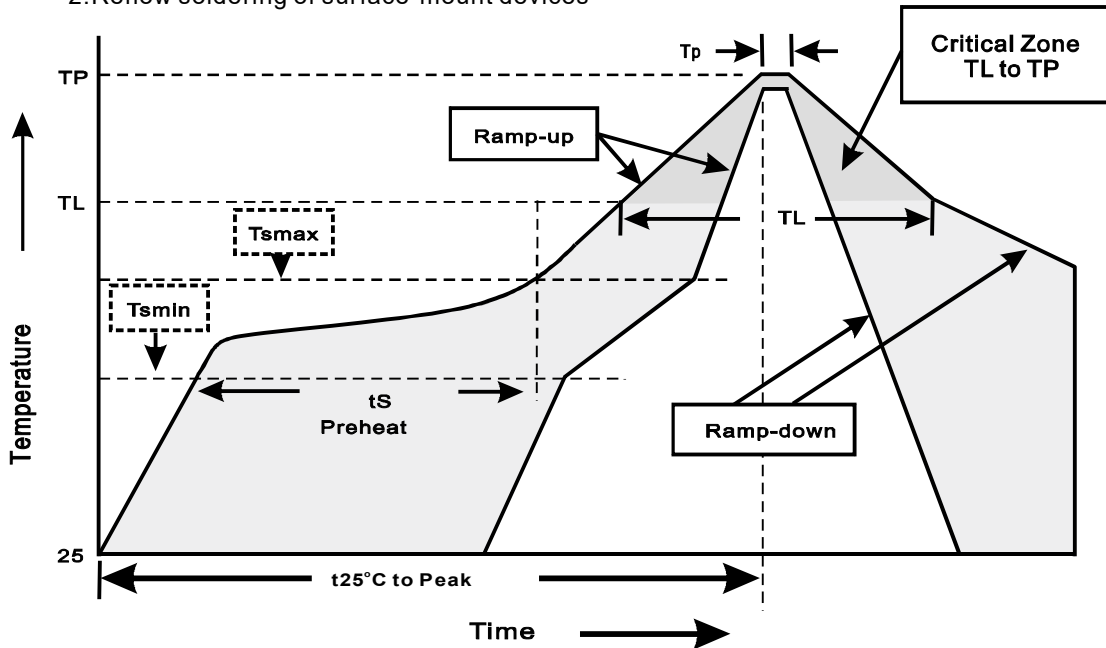
Item	Symbol	Tolerance	SOT-23
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	55.00
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W1	1.0	12.0

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

FMBTRA107SS

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smIn}) -Temperature Max(T _{smax}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smax} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _p)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes