

FMBTRA105SS

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FMBTRA105SS

PNP Silicon Epitaxial Planar Digital Transistor

Features

- With built-in bias resistors.
- Simplify circuit design.
- Reduce a quantity of parts and manufacturing process.
- We declare that the material of product compliance with RoHS requirements.
- Suffix "-H" indicates Halogen free parts, ex. FMBTRA105SS-H.

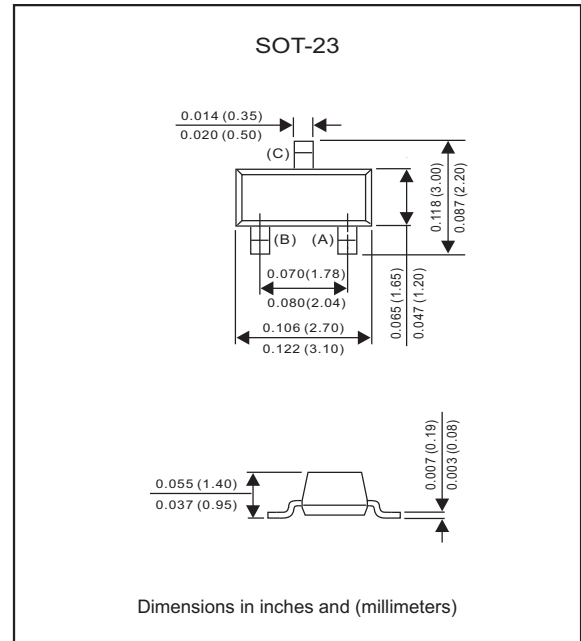
Applications

- Inverter, Interface, Driver

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-23
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.008 gram

Package outline



Maximum ratings (AT $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Output voltage	$-V_o$	50	V
Input voltage	$-V_i$	12, -5	V
Output current	$-I_o$	100	mA
Power dissipation	P_{tot}	200	mW
Junction temperature	T_j	150	$^{\circ}\text{C}$
Storage temperature range	T_{stg}	-55 to +150	$^{\circ}\text{C}$

Electrical characteristics (AT $T_A=25^{\circ}\text{C}$ unless otherwise noted)

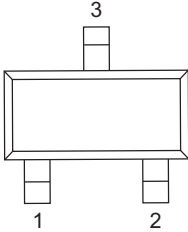
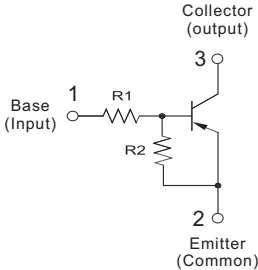
Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
DC current gain	$-V_o=5\text{V}$, $-I_o=10\text{mA}$	h_{FE}	80			
Output cut-off current	$-V_o=50\text{V}$	$-I_{O(OFF)}$			500	nA
Input current	$-V_i=5\text{V}$	I_i			3.6	mA
Output voltage	$-I_o=10\text{mA}$, $-I_i=0.5\text{mA}$	$-V_{O(ON)}$			0.3	V
Input voltage (ON)	$-V_o=0.2\text{V}$, $-I_o=5\text{mA}$	$-V_{I(ON)}$			1.1	V
Input voltage (OFF)	$-V_o=5\text{V}$, $-I_o=0.1\text{mA}$	$-V_{I(OFF)}$	0.5			V
Transition frequency	$-V_o=10\text{V}$, $-I_o=5\text{mA}$ (Note 1)	f_T		200		MHZ
Input resistance		R_i		2.2		K Ω
Resistance ratio		R_1 / R_2		0.047		

Note :

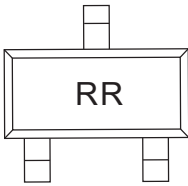
1.Characteristic of transistor only.

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Pinning information

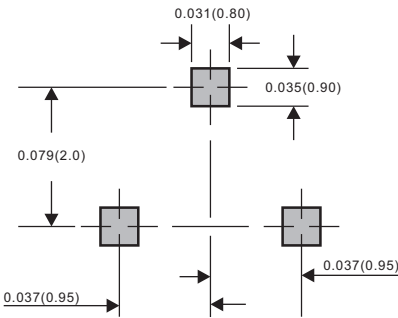
Pin	Simplified outline	Symbol
Pin1 Base Pin2 Emitter Pin3 Collector		

Marking

Type numbe	Marking code
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Suggested solder pad layout

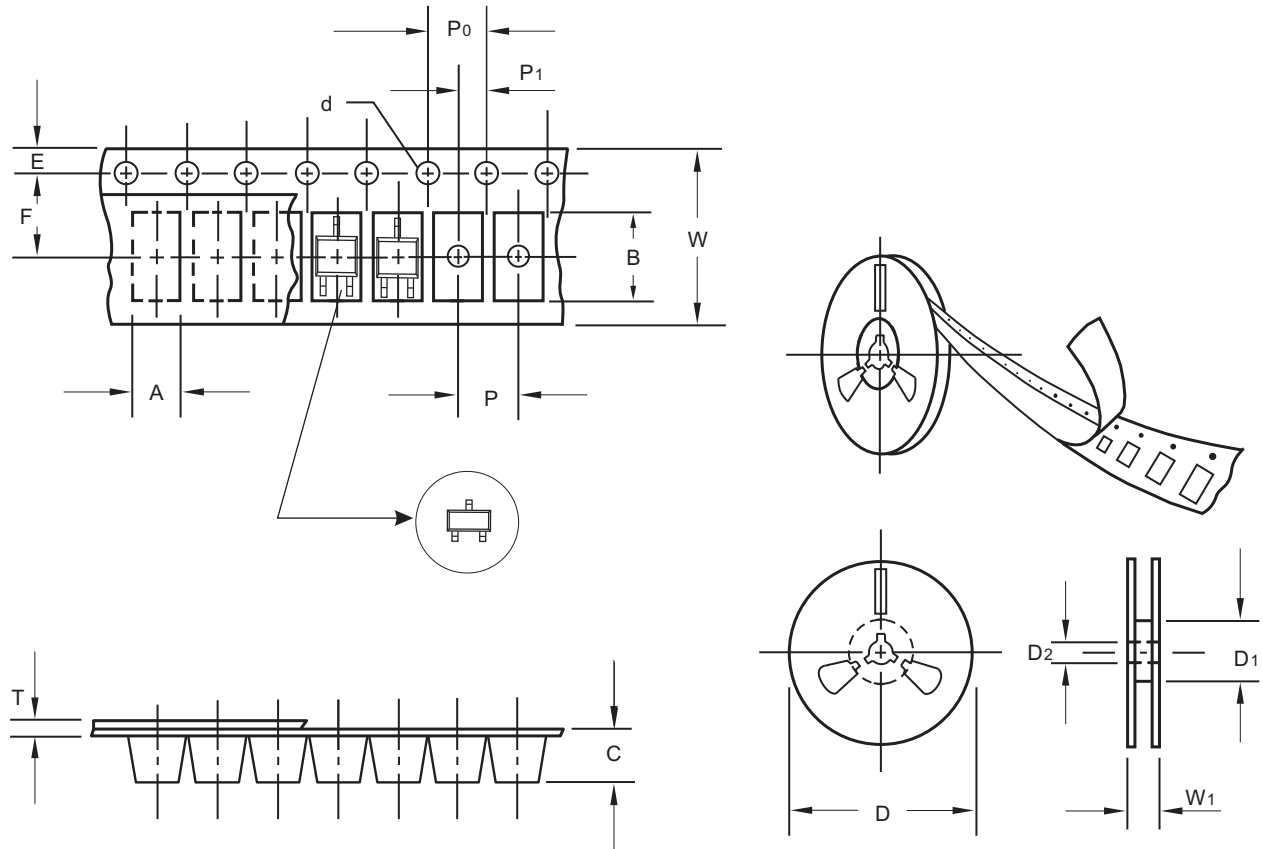
SOT-23



Dimensions in inches and (millimeters)

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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-23
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D ₁	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D ₁	min	55.00
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W ₁	1.0	12.0

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

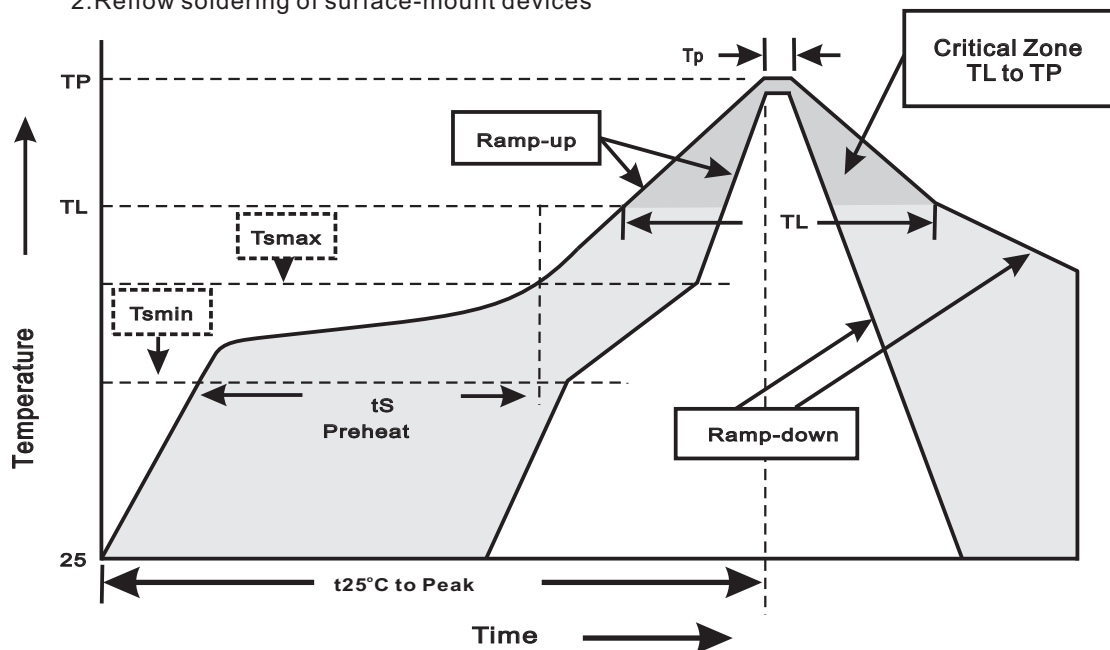
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-23	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000	11.6

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{smmin}) -Temperature Max(T _{smmax}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{smmax} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _p)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes