

FMBT114DW-Q1

List

List.....1

Package outline.....2

Features.....2

Mechanical data.....2

Maximum ratings2

Electrical characteristics.....3

Rating and characteristic curves.....4~5

Pinning information.....6

Marking.....6

Suggested solder pad layout.....6

Packing information.....7

Reel packing.....8

Suggested thermal profiles for soldering processes.....8

High reliability test capabilities.....9

FMBT114DW-Q1

Dual Digital Transistors (Built-in Resistors) NPN+PNP Silicon

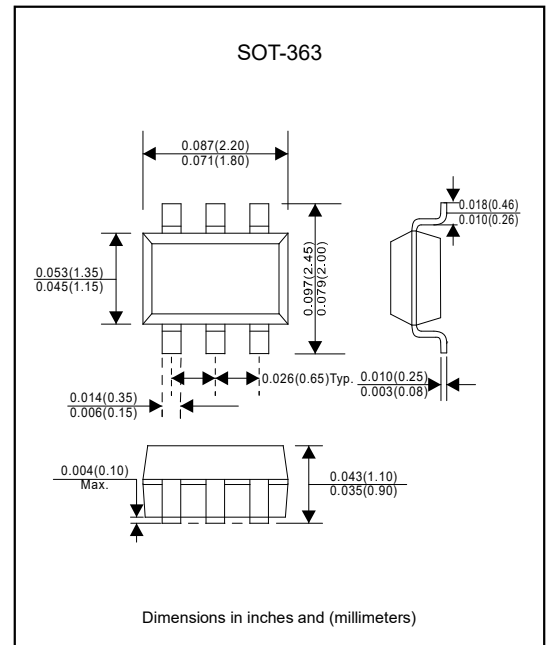
Features

- Transistor elements are independent, eliminating interference.
- Mounting cost and area can be cut in half.
- Qualified to AEC-Q101 standards for high reliability.
- Lead-free parts meet RoHS requirements.
- Suffix "-H" indicates Halogen free-part, ex.FMBT114DW-Q1-H.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant.
- Case : Molded plastic, SOT-363.
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026.
- Mounting Position : Any.

Package outline



Maximum ratings of TR1 (At $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	50	V
Input voltage	V_I	-10 to +40	V
Output current	I_O	50	mA
	$I_{C(MAX)}$	100	
Power dissipation	P_D	150	mW
Operating junction temperature	T_J	+150	$^{\circ}\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^{\circ}\text{C}$

Maximum ratings of TR2 (At $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Supply voltage	$-V_{CC}$	50	V
Input voltage	V_I	-40 to +10	V
Output current	$-I_O$	50	mA
	$-I_{C(MAX)}$	100	
Power dissipation	P_D	150	mW
Operating junction temperature	T_J	+150	$^{\circ}\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^{\circ}\text{C}$

Note 1: 150mW per element must not be exceeded.

FMBT114DW-Q1**Electrical characteristics of TR1** (At $T_A=25^{\circ}\text{C}$ unless otherwise)

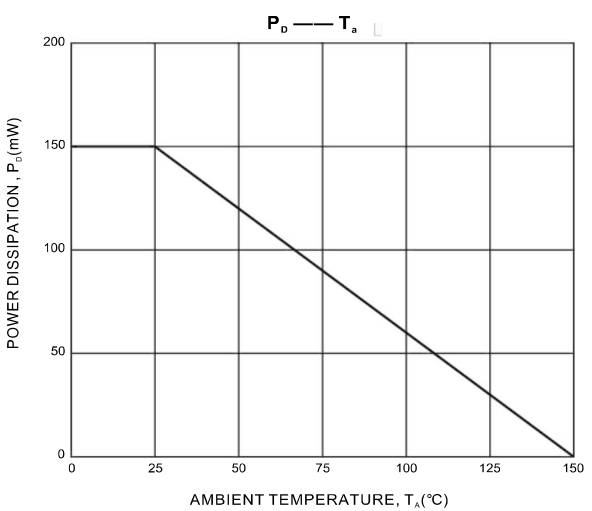
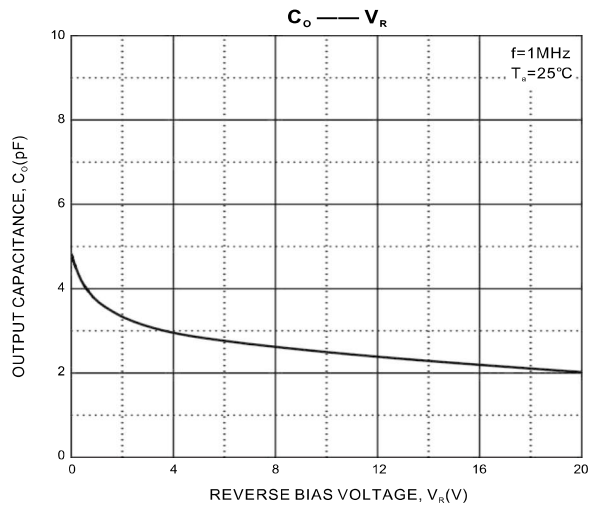
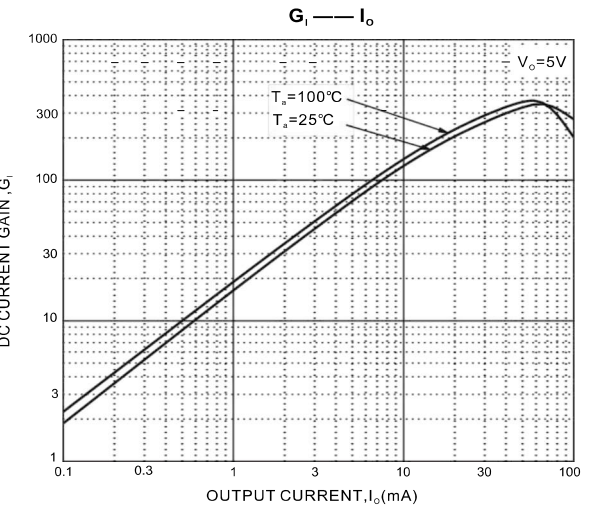
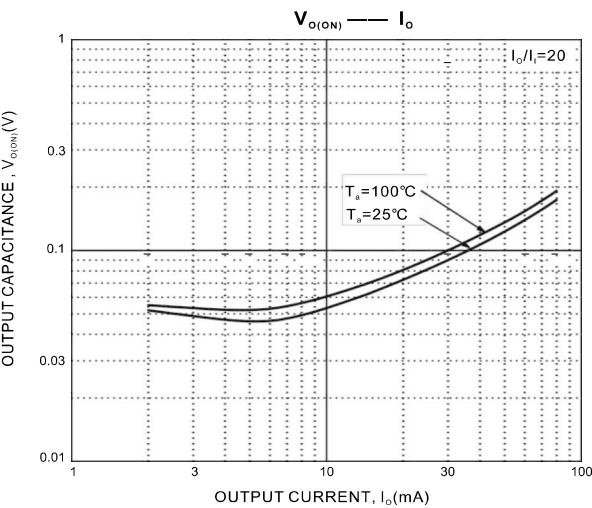
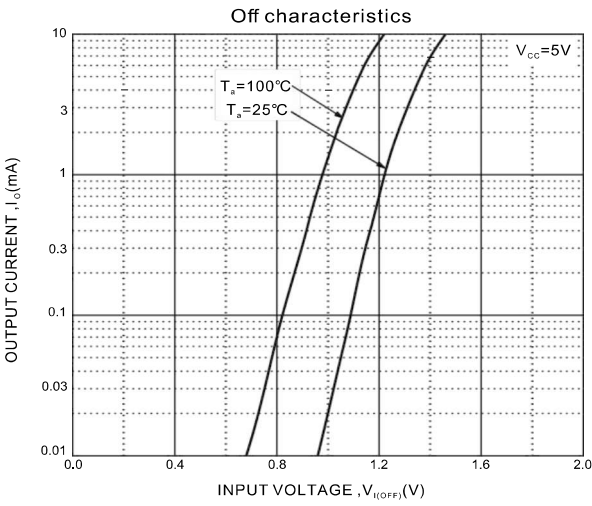
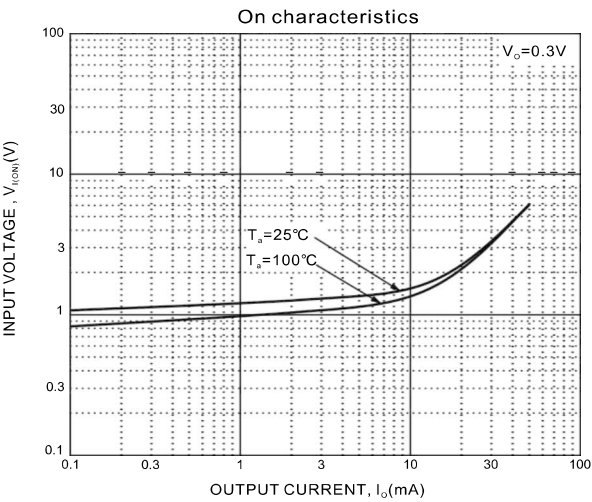
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	$V_{I(\text{off})}$	$V_{CC}=5\text{V}, I_O=100\mu\text{A}$	0.5			V
	$V_{I(\text{on})}$	$V_O=0.3\text{V}, I_O=10\text{mA}$			3	
Output voltage	$V_{O(\text{on})}$	$I_O / I_I=10\text{mA} / 0.5\text{mA}$			0.3	V
Input current	I_I	$V_I=5\text{V}$			0.88	mA
Output current	$I_{O(\text{off})}$	$V_{CC}=50\text{V}, V_I=0$			0.5	μA
DC current gain	G_I	$V_O=5\text{V}, I_O=5\text{mA}$	30			
Input resistance	R_1		7	10	13	$\text{K}\Omega$
Resistance ratio	R_2 / R_1		0.8	1.0	1.2	
Transition frequency	f_T	$V_{CE}=10\text{V}, I_E=5\text{mA}, f=100\text{MHz}$		250		MHz

Electrical characteristics of TR2 (At $T_A=25^{\circ}\text{C}$ unless otherwise)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	$-V_{I(\text{off})}$	$-V_{CC}=5\text{V}, -I_O=100\mu\text{A}$	0.5			V
	$-V_{I(\text{on})}$	$-V_O=0.3\text{V}, -I_O=10\text{mA}$			3	
Output voltage	$-V_{O(\text{on})}$	$-I_O / -I_I=10\text{mA} / 0.5\text{mA}$			0.3	V
Input current	$-I_I$	$-V_I=5\text{V}$			0.88	mA
Output current	$-I_{O(\text{off})}$	$-V_{CC}=50\text{V}, V_I=0$			0.5	μA
DC current gain	$-G_I$	$-V_O=5\text{V}, -I_O=5\text{mA}$	30			
Input resistance	R_1		7	10	13	$\text{k}\Omega$
Resistance ratio	R_2 / R_1		0.8	1.0	1.2	
Transition frequency	f_T	$-V_{CE}=10\text{V}, -I_E=5\text{mA}, f=100\text{MHz}$		250		MHz

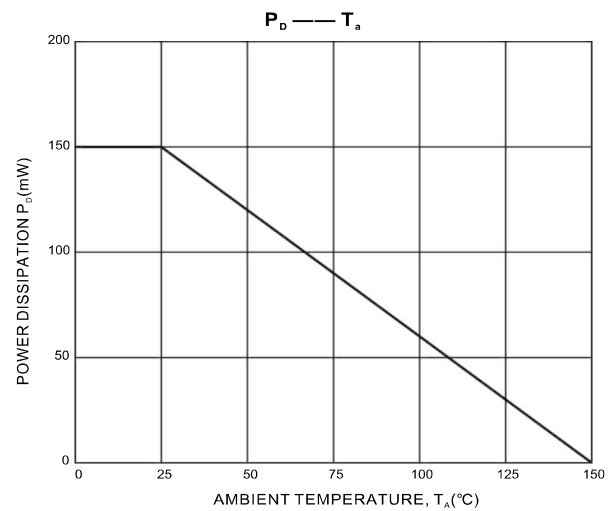
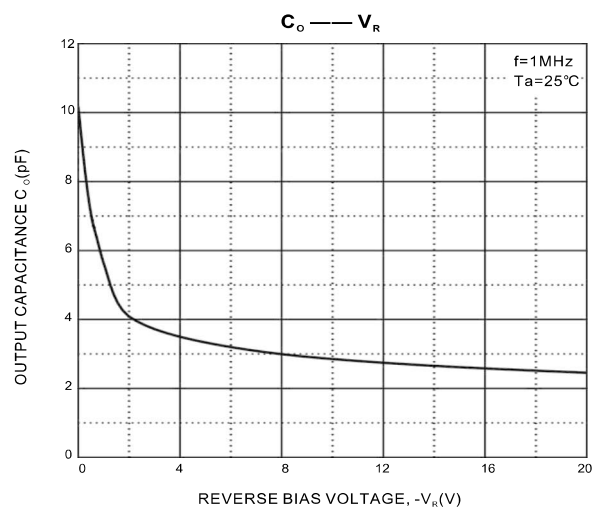
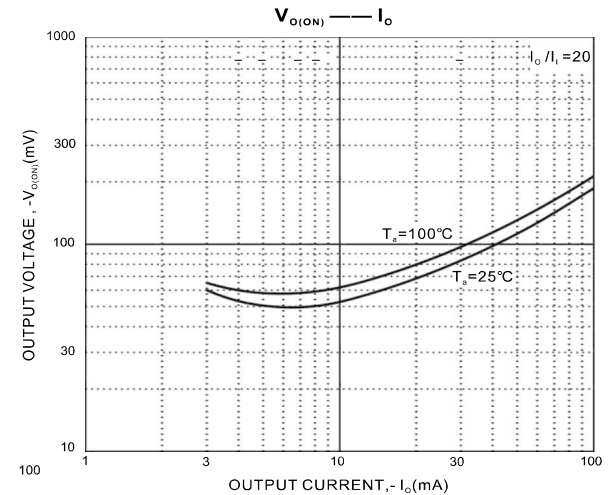
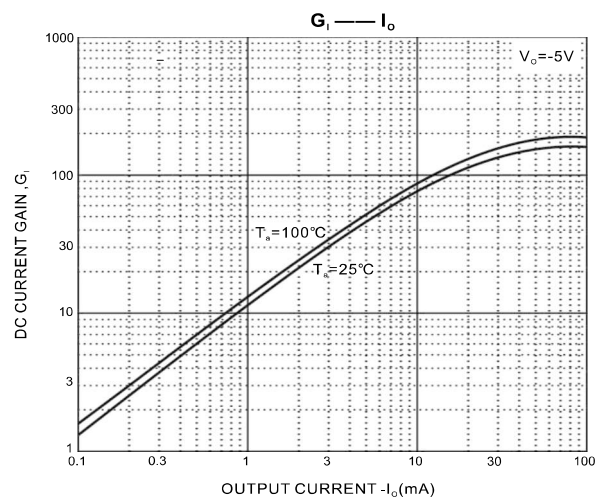
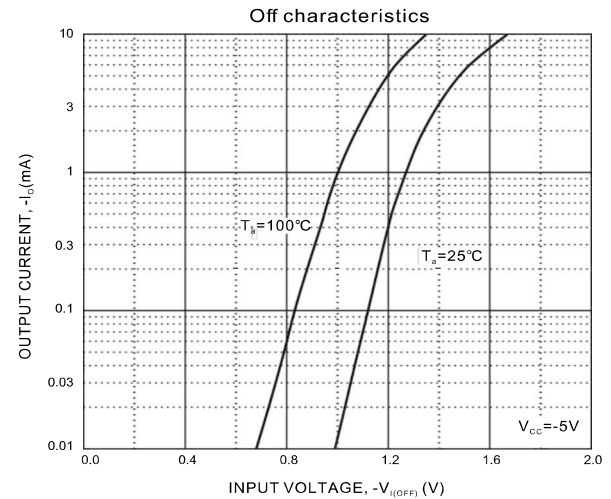
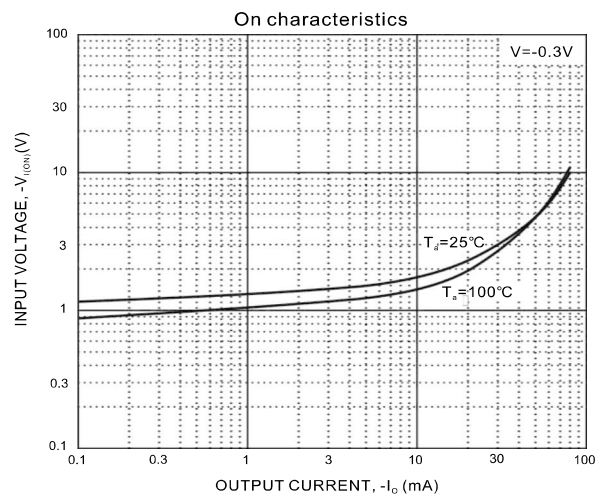
FMBT114DW-Q1

Rating and characteristic curves (NPN)



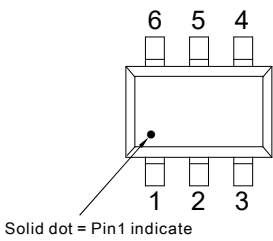
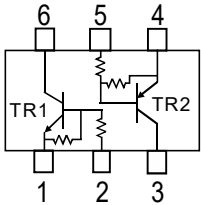
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Rating and characteristic curves (PNP)



FMBT114DW-Q1

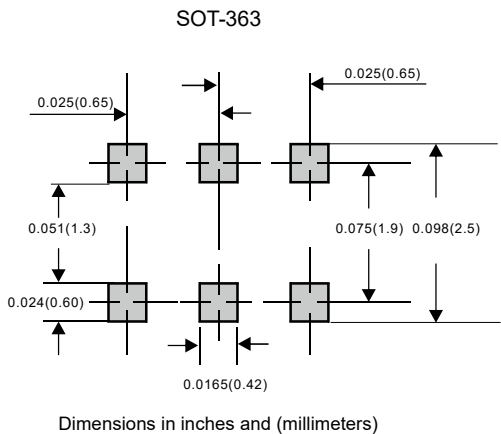
Pinning information

Pin	Simplified outline	Symbol
Pin 1 GND (Emitter) TR1 Pin 2 Input (Base) TR1 Pin 3 Output (Collector) TR2 Pin 4 GND (Emitter) TR2 Pin 5 Input (Base) TR2 Pin 6 Output (Collector) TR1	 Solid dot = Pin1 indicate	

Marking

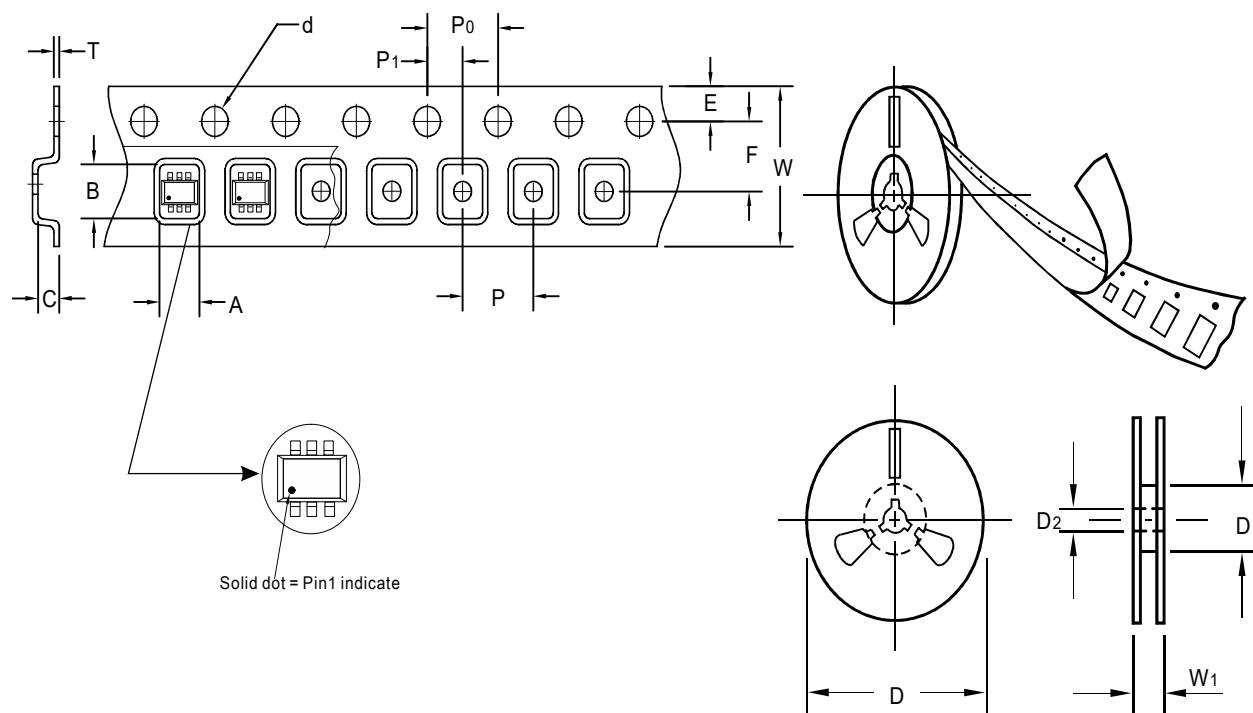
Type number	Marking code
FMBT114DW-Q1	D3

Suggested solder pad layout



FMBT114DW-Q1

Packing information



unit:mm

Item	Symbol	Tolerance	SOT-363
Carrier width	A	0.1	2.25
Carrier length	B	0.1	2.55
Carrier depth	C	0.1	1.20
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D ₁	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D ₁	min	54.40
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W ₁	1.0	12.3

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

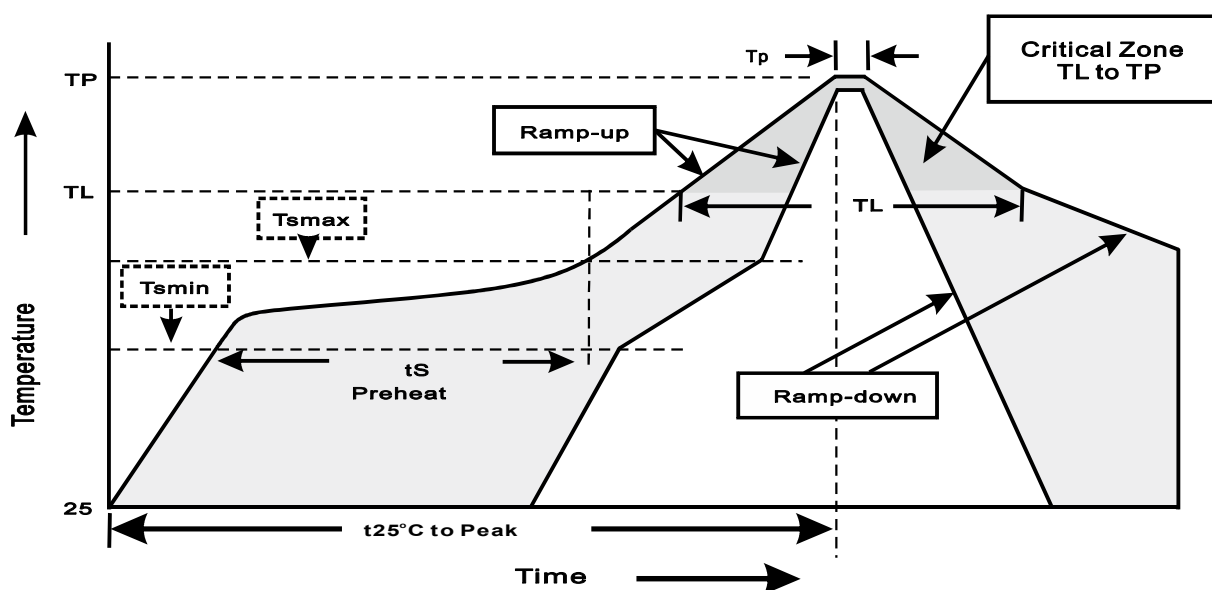
FMBT114DW-Q1

Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)
SOT-363	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	$< 3^\circ\text{C/sec}$
Preheat - Temperature Min(T_{smin}) - Temperature Max(T_{smax}) - Time(min to max)(t_s)	150°C 200°C 60~120sec
T_{smax} to T_L - Ramp-upRate	$< 3^\circ\text{C/sec}$
Time maintained above: - Temperature(T_L) - Time(t_L)	217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	$< 6^\circ\text{C/sec}$
Time 25°C to Peak Temperature	$< 6\text{minutes}$

FMBT114DW-Q1**High reliability test capabilities**

Item Test	Conditions	Reference
1. MSL Preconditioning	24hr bake@125°C+168hrs@85°C /85%RH+3xIR@260°C+1flux immersion+alcohol+DI H2O rinse	JESD22-A113
2. Intermittent Operating Life	Ta=25°C, $\Delta T_j \geq 100^\circ\text{C}$ On/Off=2min Test Duration:1000hrs	MIL-STD-750E METHOD 1037
3. High Temperature Reverse Bias	VCE=80%B _{VCE0} (T _J =T _J max.) Test Duration:1000hrs	JESD22-A108
4. High Temperature Storage Life	Ta=150°C Test Duration:1000hrs	JESD22 A-103
5. Temperature Cycle	-55°C(15min) to 150°C(15min) Test Cycles:1000cycles	JESD22 A-104
6. Autoclave	P=2atm Ta=121°C RH=100% Test Duration:96hrs	JESD22 A-102
7. Solderability	245±5°C for 5sec	J-STD-002
8. Moisture Resistance		MIL-STD-750E METHOD 1021.2
9. Resistance To Solder Heat	Ta=85°C/85%Relative humidity Test Duration:1000hrs	JESD22 B-106
10. High Temperature High Humidity Reverse Bias	260±5°C for 10sec	JESD22-A101
	Ta=85°C, 85%RH, VCE=80%B _{VCE0} Test Duration: 1000hrs	