

DTA114EUA

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DTA114EUA

PNP Silicon Epitaxial Planar Digital Transistor

Features

- Built-in bias resistors enable the configuration of an inverter circuit Without connecting external input resistors(see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, marking device design easy.
- We declare that the material of product compliance with RoHS requirements.
- Suffix "-H" indicates Halogen free parts, ex. DTA143EUA-H.

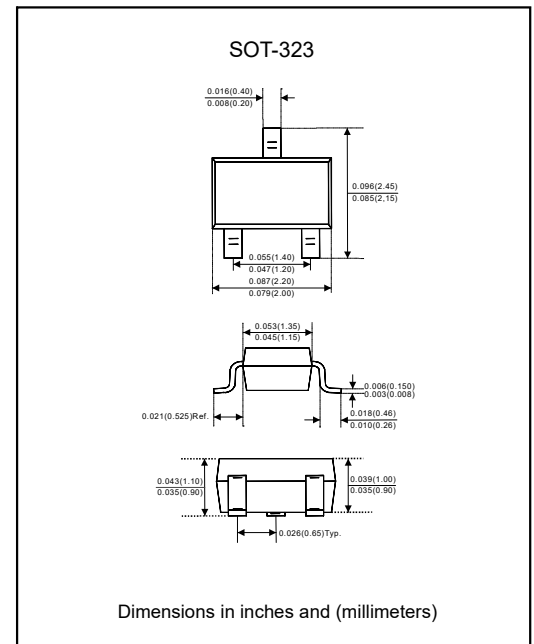
Applications

- Inverter, Interface, Driver

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-323
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any

Package outline



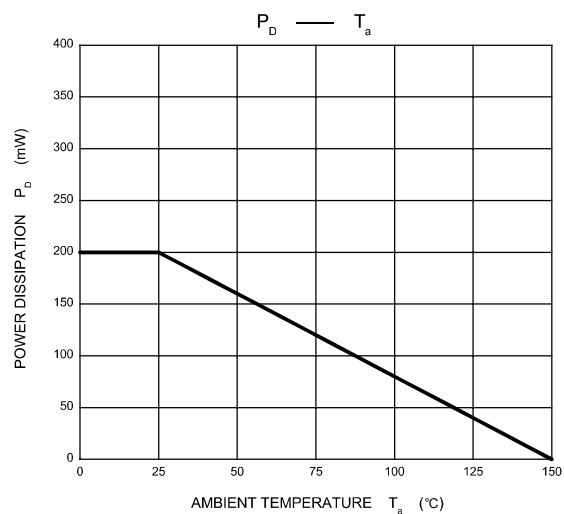
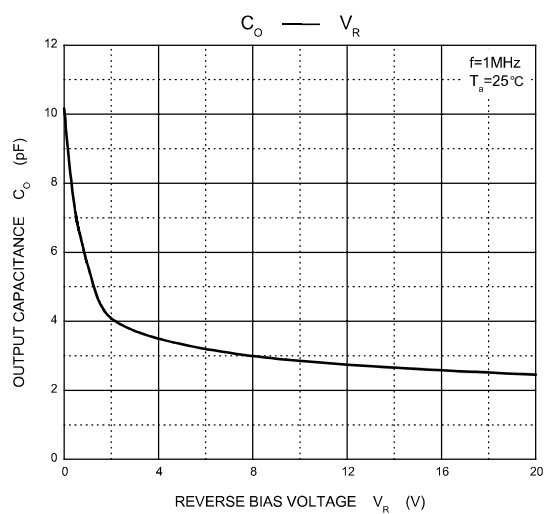
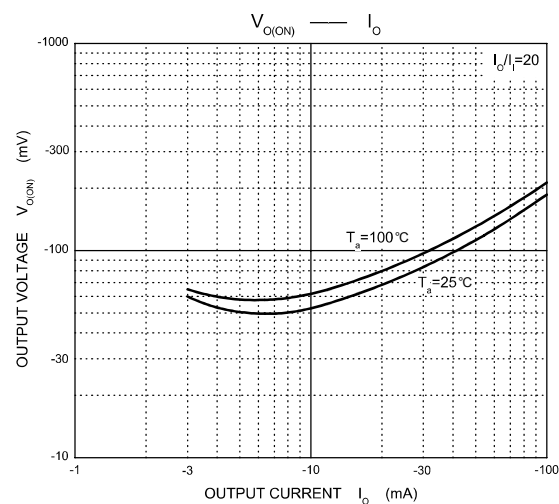
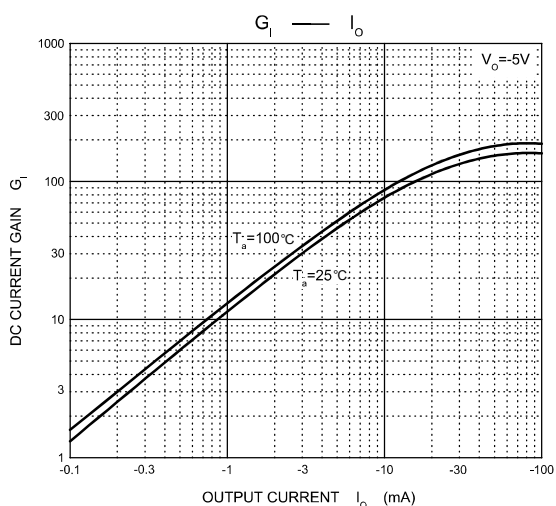
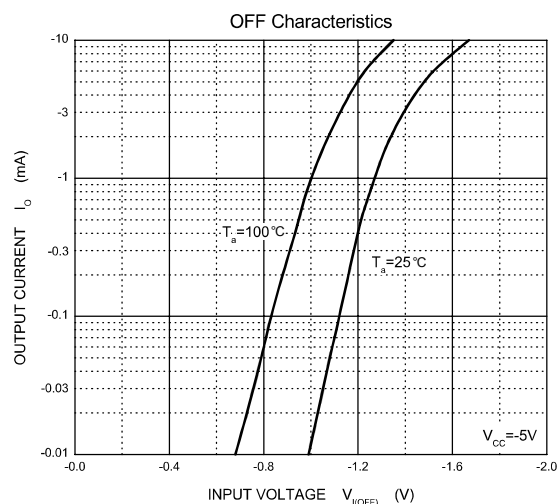
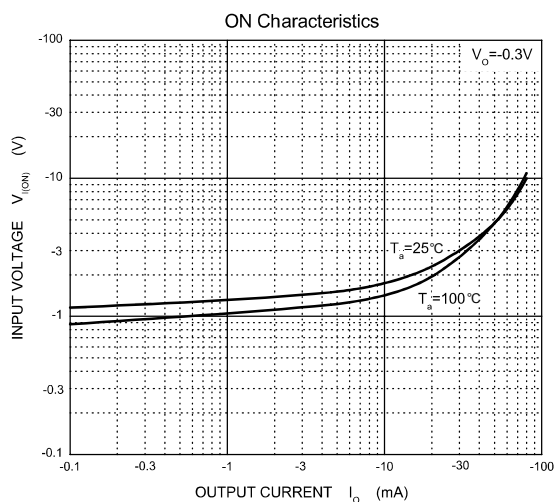
Maximum ratings (At $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Collector to emitter voltage	$-V_{CEO}$	50	V
Input voltage	V_I	-40 to +10	V
Collector current	$-I_C$	50	mA
Peak collector current	$-I_{CM}$	100	mA
Power dissipation	P_D	200	mW
Junction temperature	T_J	150	$^{\circ}\text{C}$
Storage temperature range	T_{stg}	-55 to +150	$^{\circ}\text{C}$

Electrical characteristics (At $T_A=25^{\circ}\text{C}$ unless otherwise noted)

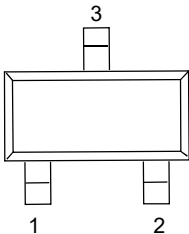
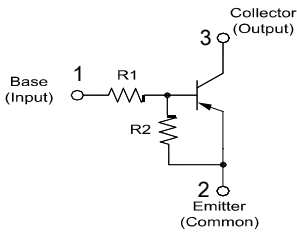
Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Input voltage	$-V_{CE}=5V, -I_C=100\mu A$	$-V_{I(off)}$	0.5			V
	$-V_o=0.3V, I_o=10mA$	$-V_{I(off)}$			3	V
Output voltage	$-I_o/-I_i=10mA/0.5mA$	$-V_{O(on)}$			0.3	V
Input current	$-V_I=5V$	$-I_i$			0.88	mA
Output current	$-V_{CE}=50V, V_I=0V$	$-I_{O(off)}$			0.5	μA
DC current gain	$-V_o=5V, -I_o=5mA$	h_{FE}	30			
Transition frequency	$-V_{CE}=10V, -I_o=5mA, f=100MHz$	f_T		250		MHz
Input resistance		R_i	7	10	13	K Ω
Resistance ratio		R_2 / R_1	0.8	1	1.2	

Rating and characteristic curves (DTA114EUA)



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Pinning information

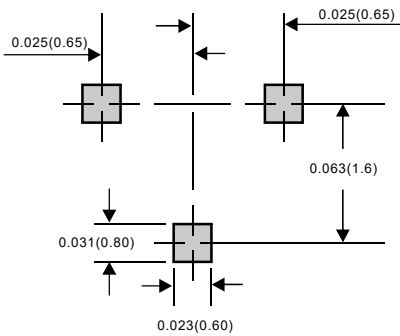
Pin	Simplified outline	Symbol
Pin1 BASE Pin2 EMITTER Pin3 COLLECTOR		

Marking and resistor values

Type Number	Marking Code
DTA114EUA	14

Suggested solder pad layout

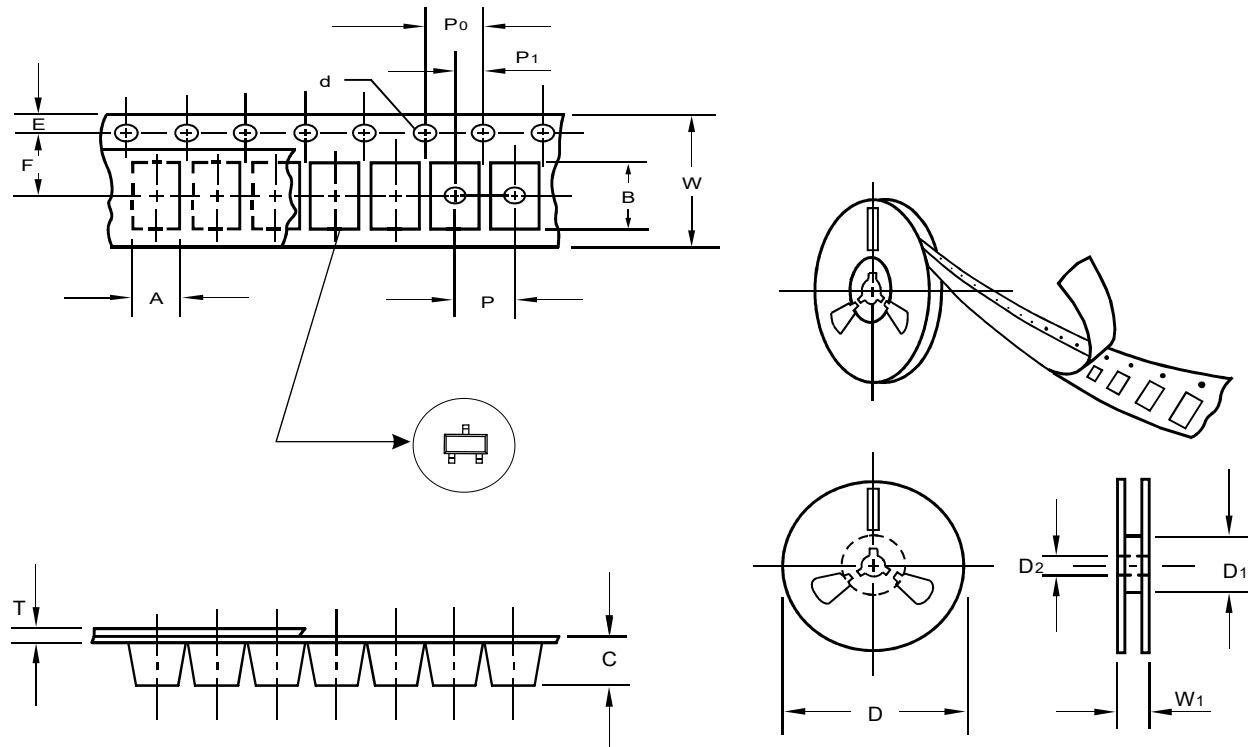
SOT-323



Dimensions in inches and (millimeters)

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Packing information



unit:mm

Item	Symbol	Tolerance	SOT-323
Carrier width	A	0.1	1.47
Carrier length	B	0.1	2.95
Carrier depth	C	0.1	1.15
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D ₁	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D ₁	min	62.00
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W ₁	1.0	11.40

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

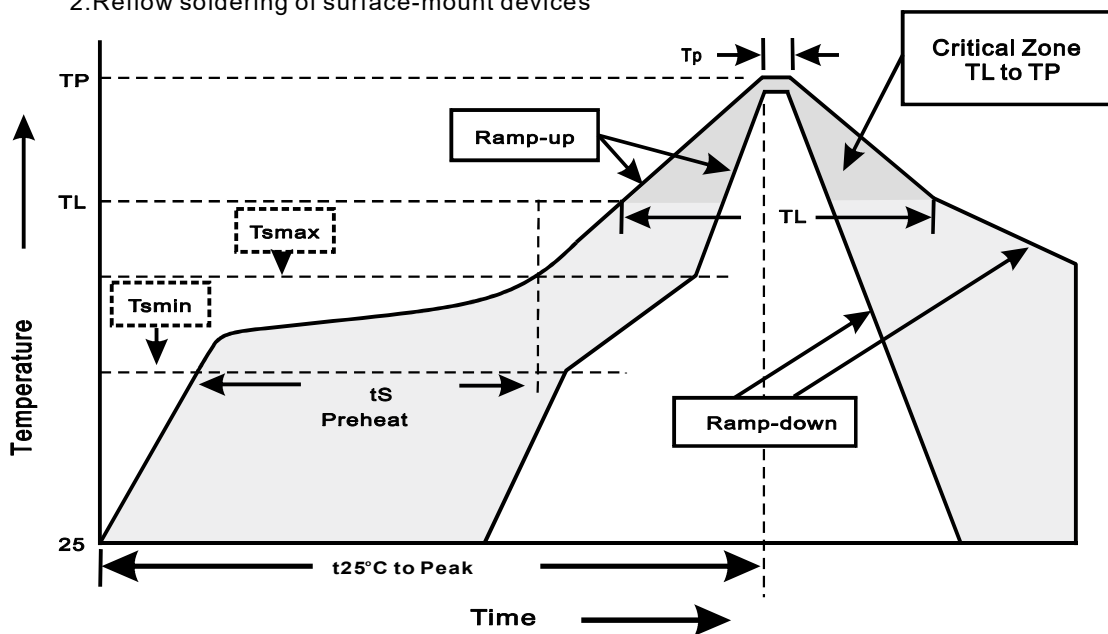
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-323	7"	3,000	4.0	30,000	183*183*123	178	382*262*387	240,000	9.5

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	<3°C/sec
Preheat -Temperature Min(T_{smin}) -Temperature Max(T_{smax}) -Time(min to max)(t_s)	150°C 200°C 60~120sec
T_{smax} to T_L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T_L) -Time(t_L)	217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes