

FMOS3134KDW

List

List..... 1

Package outline..... 2

Features..... 2

Mechanical data..... 2

Maximum ratings 2

Electrical characteristics..... 3

Rating and characteristic curves..... 4

Pinning information..... 5

Marking..... 5

Suggested solder pad layout..... 5

Packing information..... 6

Reel packing..... 7

Suggested thermal profiles for soldering processes..... 7

FMOS3134KDW

20V Dual N-Channel Enhancement Mode MOSFET-ESD Protection

Features

- Lead free product is acquired
- Surface mount package
- N-channel switch with low $R_{DS(on)}$
- Operated at low logic level gate drive
- ESD Protected gate HBM 2kV
- Lead-free parts meet RoHS requirements
- Suffix "-H" indicates Halogen-free part, ex. FMOS3134KDW-H

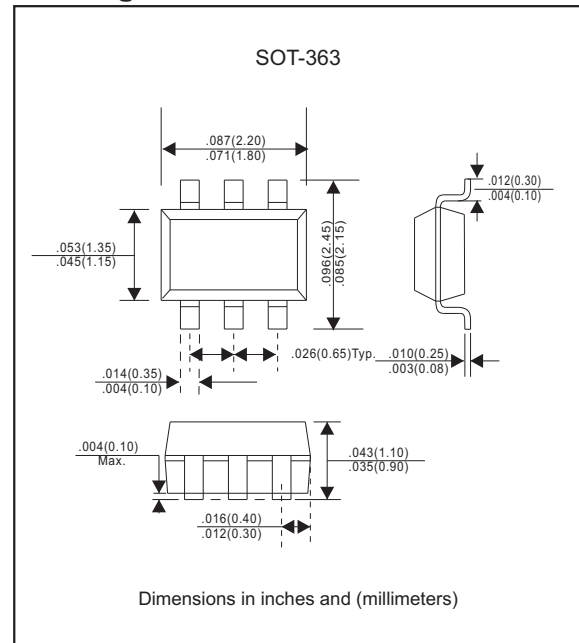
Application

- Load/power switching
- Interfacing switching
- Battery management for ultra small portable electronics
- Logic level shift

Mechanical data

- Epoxy: UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-363
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Polarity : See Diagram
- Mounting Position : Any
- Weight : Approximated 0.006 gram

Package outline



Maximum ratings (AT $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	Symbol	MIN.	TYP.	MAX.	UNIT
Drain-source voltage	V_{DS}			20	V
Continuous drain current($t \leq 10s$)	I_D			0.75	A
Gate-source voltage	V_{GS}			± 12	V
Power dissipation (note 1)	P_D			150	mW
Thermal resistance junction to ambient	$R_{\theta JA}$		833		$^\circ\text{C/W}$
Operation junction temperature range	T_J	-55		+150	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55		+150	$^\circ\text{C}$

Note 1: Repetitive rating : Pulse width limited by junction temperature.

FMOS3134KDW

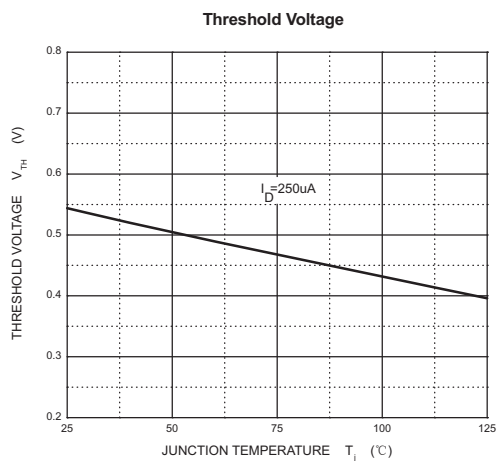
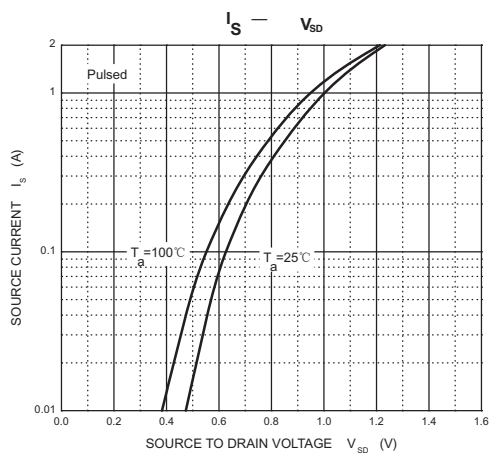
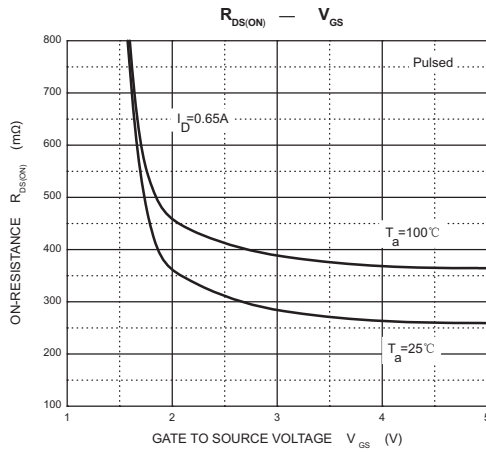
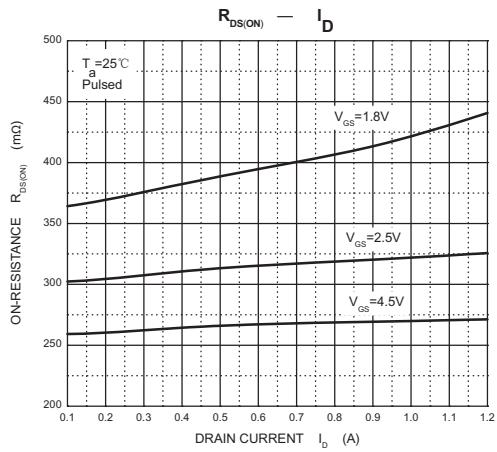
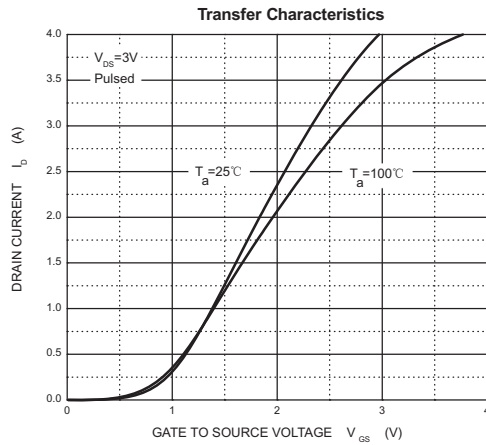
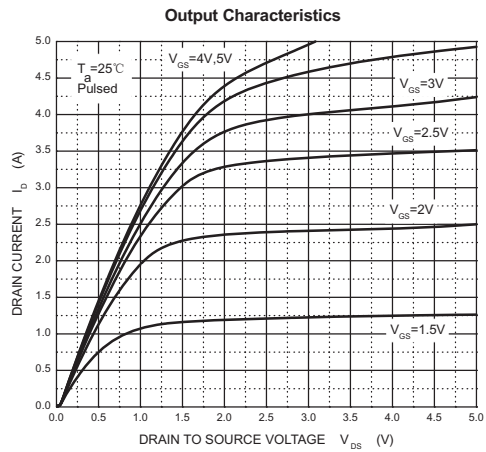
Electrical characteristics (At $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	Symbol	MIN.	TYP.	MAX.	UNIT
Static characteristics						
Drain-source breakdown voltage	$V_{GS} = 0V, I_D = 250\mu A$	$V_{(BR)DSS}$	20			V
Zero gate voltage drain current	$V_{DS} = 20V, V_{GS} = 0V$	I_{DSS}			1.0	μA
Gate-source leakage current	$V_{GS} = \pm 10V, V_{DS} = 0V$	I_{GSS}			± 20	μA
Gate threshold voltage (note 1)	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(th)}$	0.35	0.54	1.1	V
Drain-source on-resistance (note 1)	$V_{GS} = 4.5V, I_D = 0.65A$ $V_{GS} = 2.5V, I_D = 0.55A$ $V_{GS} = 1.8V, I_D = 0.45A$	$R_{DS(on)}$		270 320 390	380 450 800	m Ω
Forward tranconductance (note 1)	$V_{DS} = 10V, I_D = 0.8A$	g_{FS}		1.6		S
Diode forward voltage (note 1)	$I_S = 0.15A, V_{GS} = 0V$	V_{SD}			1.2	V
Dynamic characteristics (note 2)						
Input capacitance	$V_{DS} = 16V, V_{GS} = 0V, f = 1MHz$	C_{iss}		79	120	pF
Output capacitance		C_{oss}		13	20	
Reverse transfer capacitance		C_{rss}		9	15	
Switching characteristics (note 2)						
Turn-on delay time	$V_{GS} = 4.5V, V_{DS} = 10V, I_D = 0.5A$ $R_{GEN} = 10\Omega$	$t_{d(on)}$		6.7		ns
Turn-on rise time		t_r		4.8		
Turn-off delay time		$t_{d(off)}$		17.3		
Turn-off fall time		t_f		7.4		
Total gate charge	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 0.25A$	Q_g		750		pC
Gate-source charge		Q_{gs}		75		
Gate-drain charge		Q_{gd}		225		

Notes :

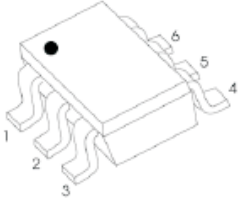
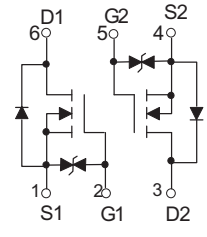
1. Pulse test : pulse width $\leq 300\mu s$, duty cycle $\leq 0.5\%$.
2. Guaranteed by design, not subject to production testing.

Rating and characteristic curves (FMOS3134KDW)



FMOS3134KDW

Pinning information

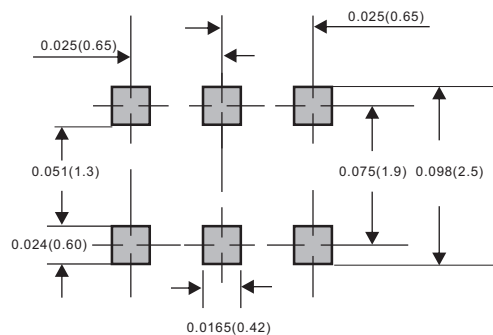
Pin	Simplified outline	Symbol
Pin 1 Source1 Pin 2 Gate1 Pin 3 Drain2 Pin 4 Source2 Pin 5 Gate2 Pin 6 Drain1		

Marking

Type number	Marking code
FMOS3134KDW	34K

Suggested solder pad layout

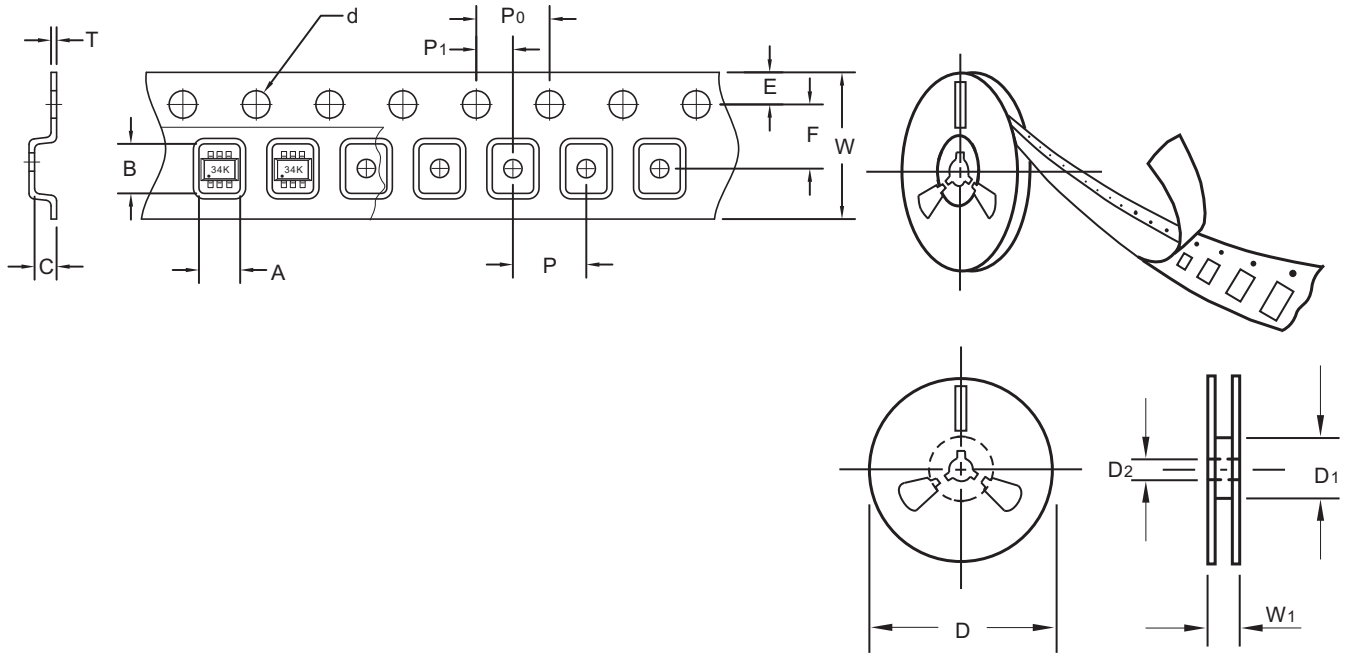
SOT-363



Dimensions in inches and (millimeters)

FMOS3134KDW

Packing information



unit:mm

Item	Symbol	Tolerance	SOT-363
Carrier width	A	0.1	2.25
Carrier length	B	0.1	2.55
Carrier depth	C	0.1	1.20
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D ₁	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D ₁	min	54.40
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W ₁	1.0	12.3

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

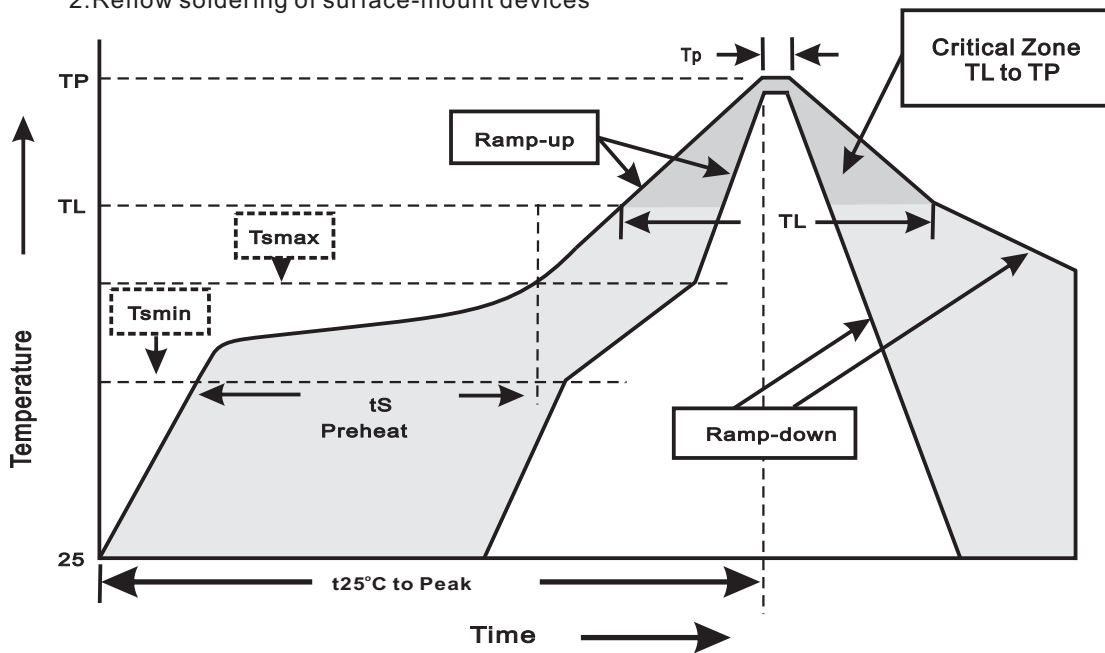
FMOS3134KDW

Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-363	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000	9.5

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{min}) -Temperature Max(T _{max}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{max} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes