FMOS1012K

List

FMOS1012K

20V N-Channel Enhancement Mode MOSFET- ESD Protection

Features

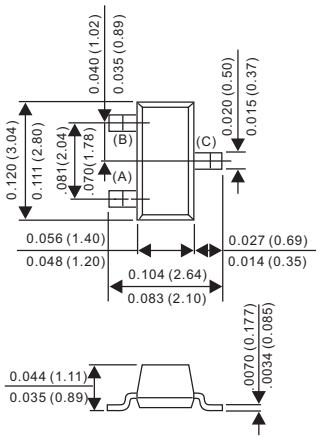
- Power MOSFET:1.8-V Rated
- Gate-Source ESD Protected:2000V
- High-Side Switching
- Low On-Resistance: 0.7Ω
- Low Threshold:0.8V(typ)
- Fast Switching Speed:10 ns
- Suffix "-H" indicates Halogen-free part, ex.FMOS1012K-H.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-23
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.008 gram

Package outline

SOT-23



Dimensions in inches and (millimeters)

Benefits

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

Applications

- Drivers: Relays, Solenoids, Lamps, Hammers,Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

Maximum ratings (AT T_A=25°C unless otherwise noted)

Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	±6		
Continuous Drain Current*b	T_A = 25°C	I_D	600	500	mA
	T_A = 85°C		400	350	
Pulsed Drain Current*a		I_{DM}	1000		
Continuous Source Current (diode conduction)*b		I_S	275	250	
Maximum Power Dissipation		P_D	225		mW
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150		°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000		V

Notes
a. Pulse width limited by maximum junction temperature.
b. Surface Mounted on FR4 Board.

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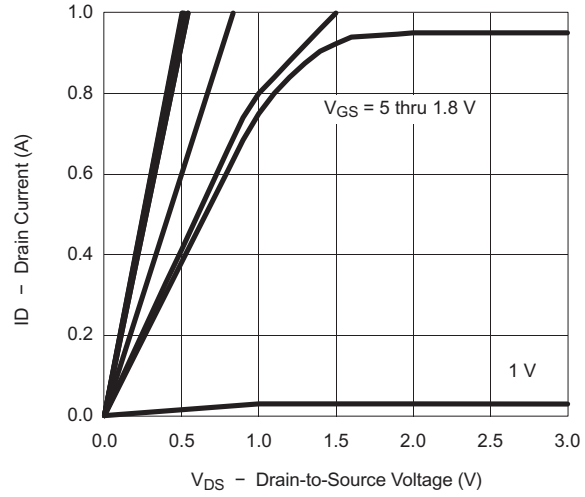
Electrical characteristics (At T_A=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.45		0.9	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5V		±0.5	±1.0	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.3	100	nA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 85°C			5	uA
On-State Drain Current*a	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	700			mA
Drain-Source On-State Resistance*a	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 600 mA		0.41	0.70	Ω
		V_{GS} = 2.5 V, I_D = 500 m A		0.53	0.85	
		V_{GS} = 1.8 V, I_D = 350 m A		0.70	1.25	
Forward Transconductance*a	g_{fs}	V_{DS} = 10 V, I_D = 400 mA		1.0		S
Diode Forward Voltage*a	V_{SD}	I_S = 150 mA, V_{GS} = 0 V		0.8	1.2	V
Dynamic* b						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 250 mA		750		pC
Gate-Source Charge	Q_{gs}			75		
Gate-Drain Charge	Q_{gd}			225		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 47Ω I_D =200 mA, V_{GEN} = 4.5 V, R_G = 10Ω		5		ns
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			25		
Fall Time	t_f			11		

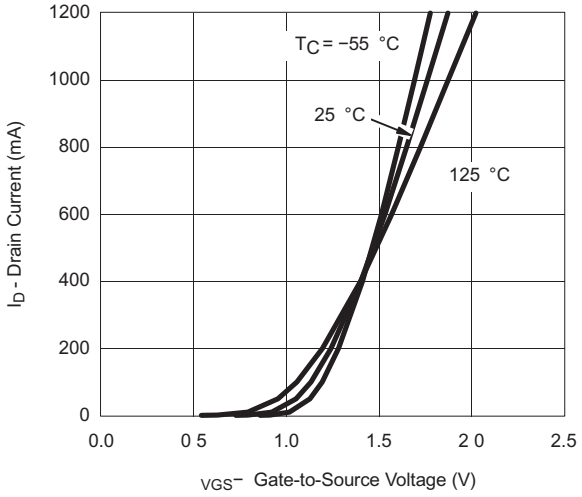
Notes:
a.Pulse test: pulse width≦300us, duty cycle≦2%
b.Guaranteed by design, not subject to production testing.

Rating and characteristic curves (FMOS1012K)

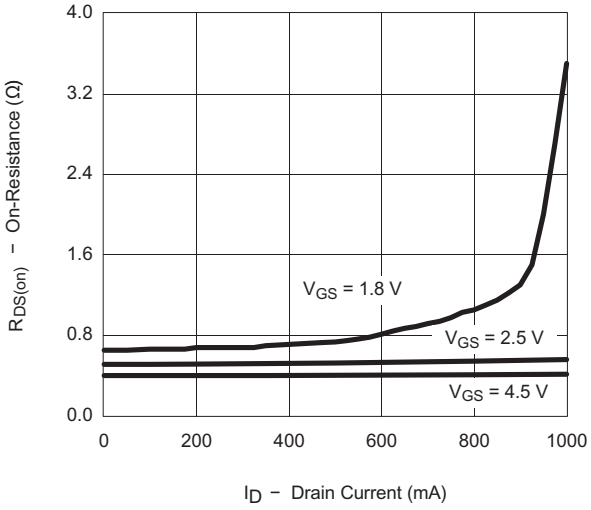
Output Characteristics



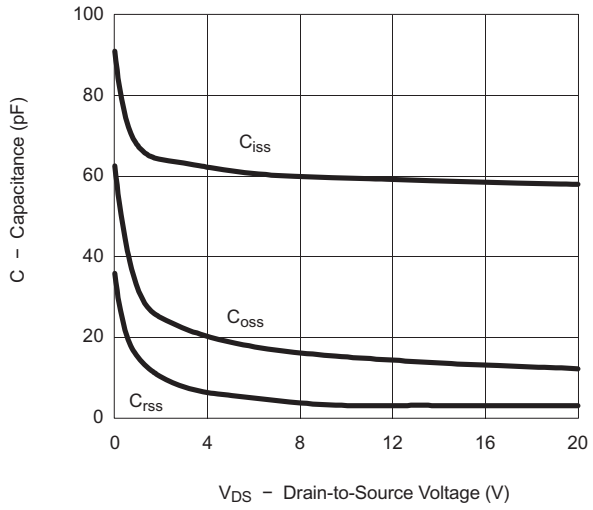
Transfer Characteristics



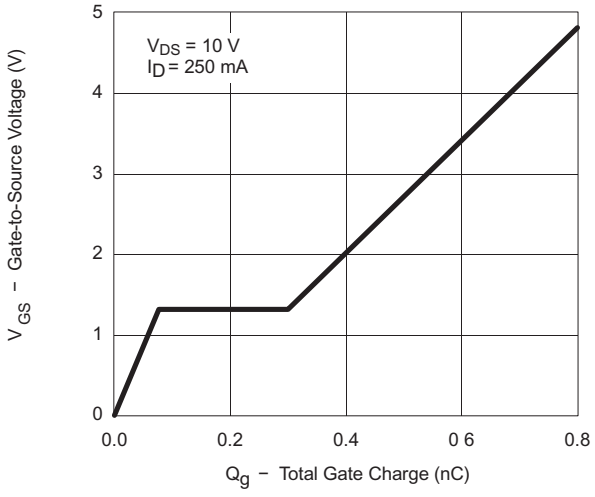
On-Resistance vs. Drain Current



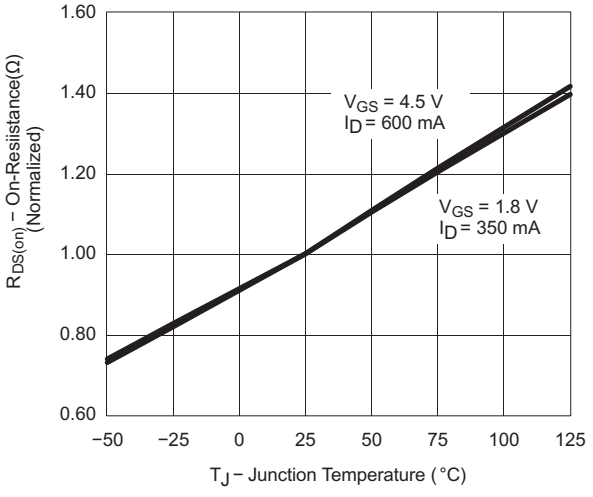
Capacitance



Gate Charge

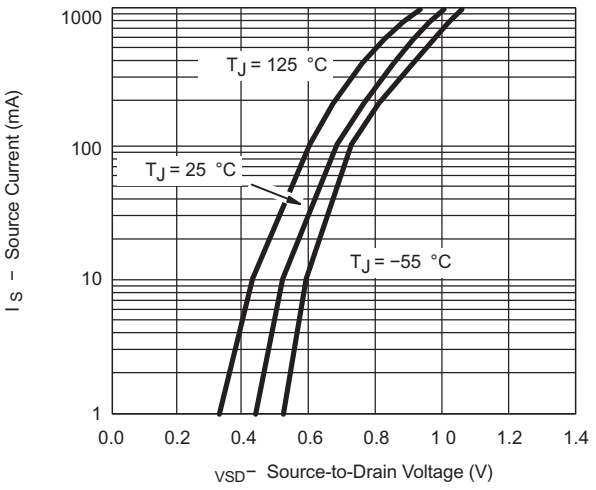


On-Resistance vs. Junction Temperature

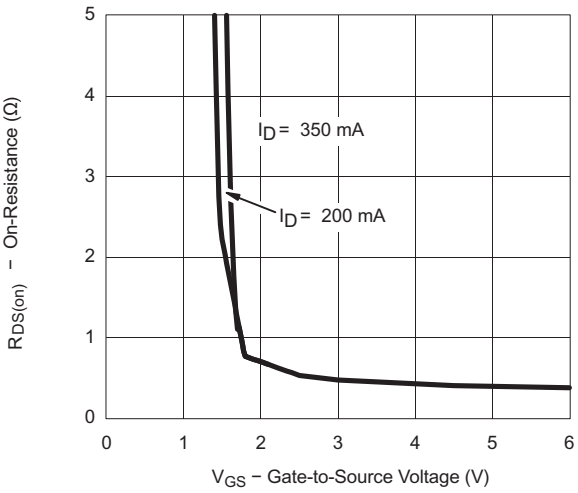


Rating and characteristic curves (FMOS1012K)

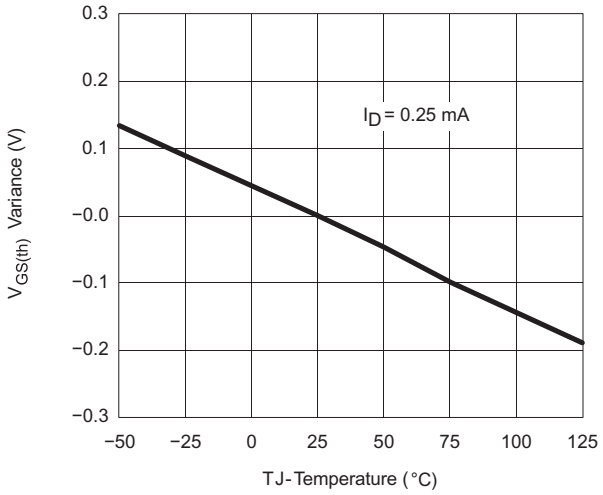
Source-Drain Diode Forward Voltage



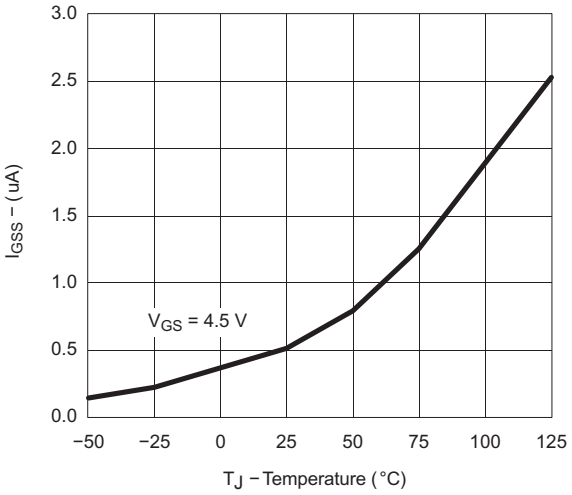
On-Resistance vs. Gate-to-Source Voltage



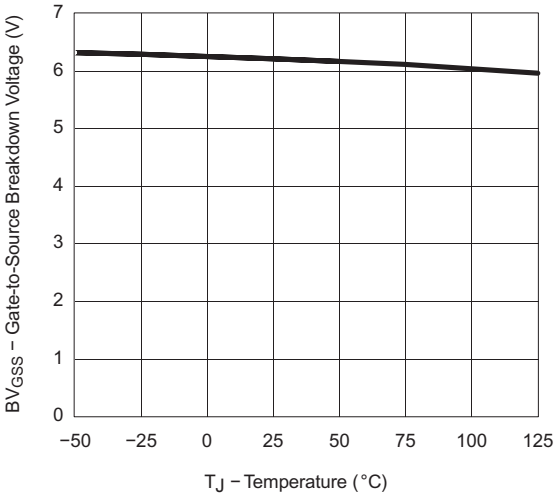
Threshold Voltage Variance vs. Temperature



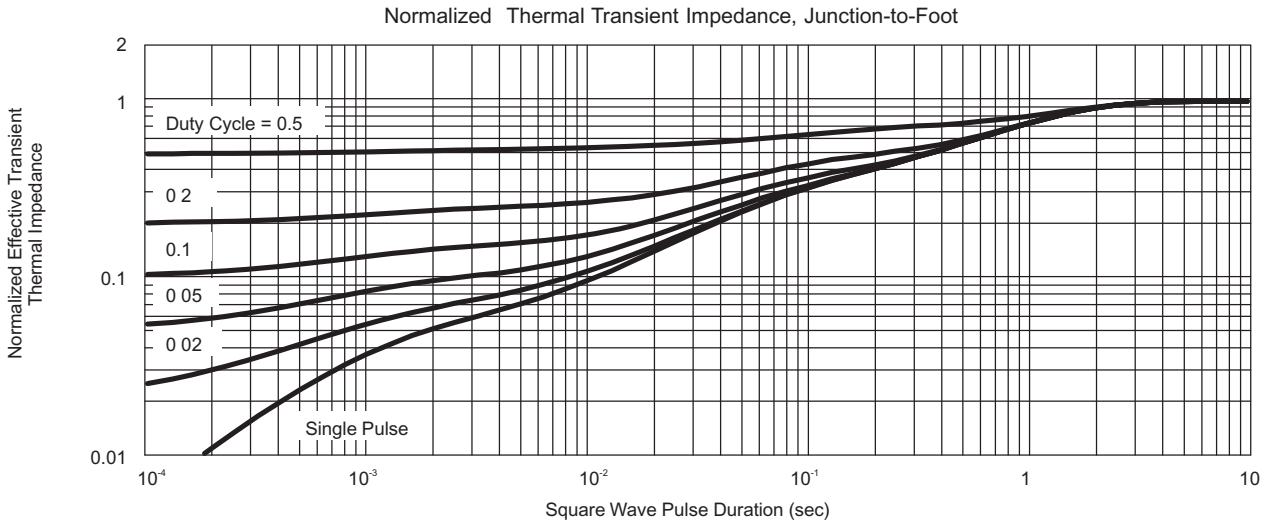
I_{GSS} vs. Temperature



BV_{GSS} vs. Temperature



Rating and characteristic curves (FMOS1012K)



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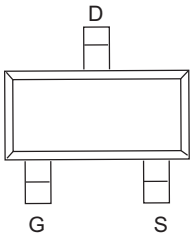
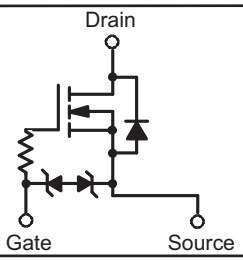
Pinning information

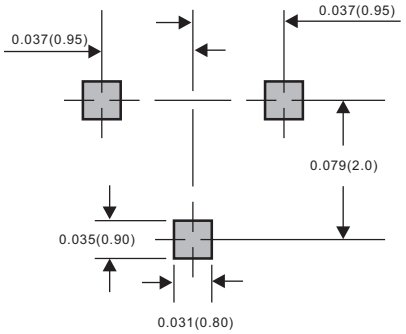
Pin	Simplified outline	Symbol
PinD Drain PinG Gate PinS Source		

Marking

Type number	Marking code
FMOS1012K	A2

Suggested solder pad layout

SOT-23



Dimensions in inches and (millimeters)

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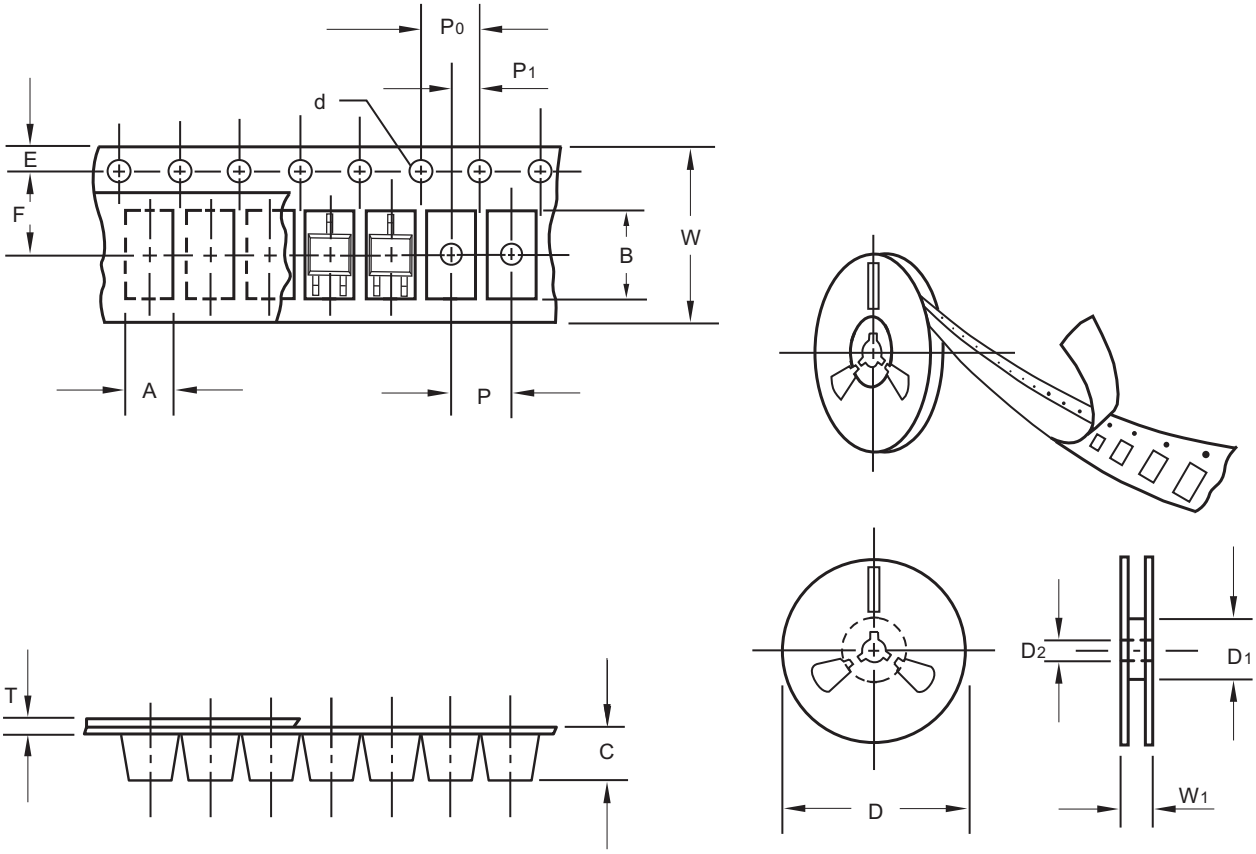
Packing information



unit:mm

Item	Symbol	Tolerance	SOT-23
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D_1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D_1	min	55.00
Feed hole diameter	D_2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P_0	0.1	4.00
Embossment center	P_1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W_1	1.0	12.0

Note:Devices are packed in accor dance with EIA standar RS-481-A and specifications listed above.

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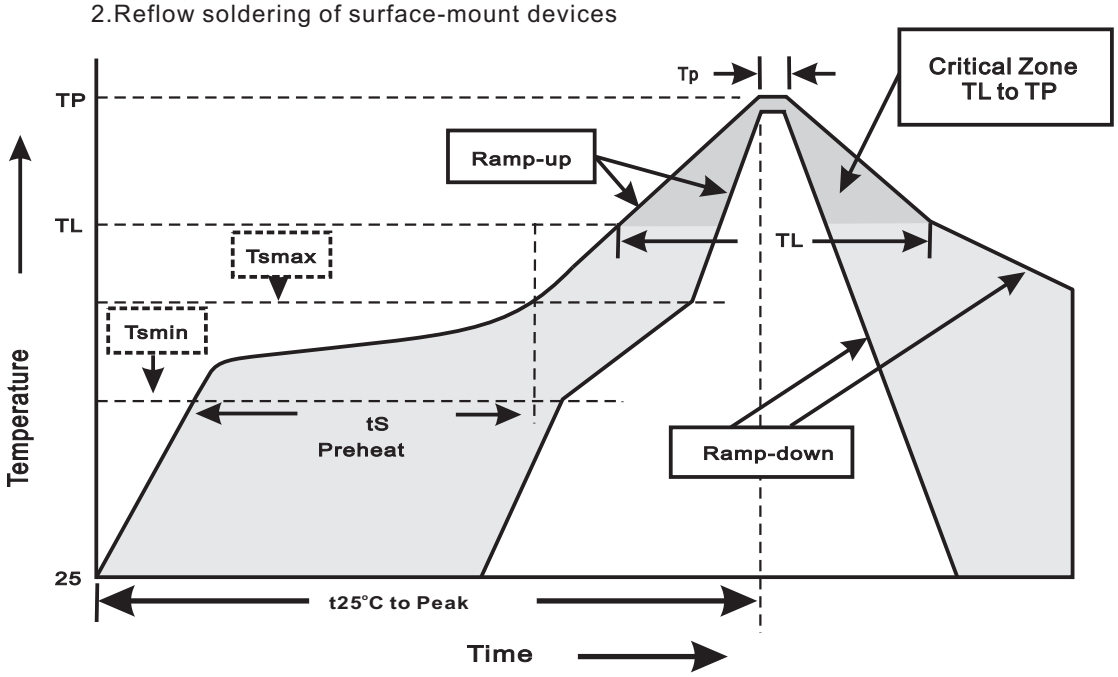
Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-23	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000	11.6

Suggested thermal profiles for soldering processes

1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%

2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	<3°C/sec
Preheat -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time(min to max)(t_s)	 150°C 200°C 60~120sec
Tsmax to T_L -Ramp-upRate	 <3°C/sec
Time maintained above: -Temperature(T_L) -Time(t_L)	 217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes