

2N7002W

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2N7002W

60V N-Channel Enhancement Mode MOSFET

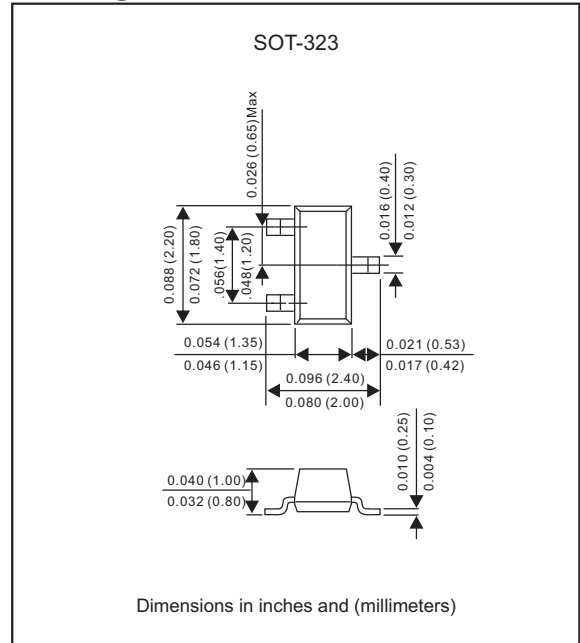
Features

- ESD Protected: 1000V
- $R_{DS(on)}$, $V_{GS}@10V$, $I_{DS}@500mA=7.5 \Omega$
- $R_{DS(on)}$, $V_{GS}@5V$, $I_{DS}@50mA=7.5 \Omega$
- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Specially designed for battery operated system, solid-state relays drivers, relays, displays, lamps, solenoids, memories, etc
- In compliance with EU RoHS 2011/65/EU directives
- Suffix "-H" indicates Halogen-free part, ex. 2N7002W-H

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-323
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.006 gram

Package outline



Maximum ratings (AT $T_A=25^\circ C$ unless otherwise noted)

| Parameter | Conditions | Symbol | MIN. | TYP. | MAX. | Unit |
|--|---|-----------------|------|------|-----------|----------------|
| Drain-source voltage | | V_{DSS} | | | 60 | V |
| Drain-gate voltage($G_{RS} = 1.0M\Omega$) | | V_{DGR} | | | 60 | V |
| Drain to current-continue | | I_D | | | ± 115 | mA |
| | | I_{DM} | | | ± 800 | |
| Gate to source voltage-continue | | V_{GS} | | | ± 20 | V |
| | | V_{GSM} | | | ± 40 | |
| Total power dissipation | Derate above $25^\circ C$ | P_D | | | 200 | mW |
| | | | | | 1.6 | mW/ $^\circ C$ |
| Operation junction and storage temperature range | | T_J, T_{STG} | -55 | | +150 | $^\circ C$ |
| Junction to ambient thermal resistance | | $R_{\theta JA}$ | | | 625 | $^\circ C/W$ |
| Single pulse drain-to-source avalanche energy | $V_{DD} = 50V, V_{GS} = 10V, I_{AS} = 0.8A, L = 30mH, R_G = 25\Omega$ | E_{AS} | | | 9.6 | mJ |
| Maximum lead temperature for soldering purposes | 1/8" from case for 10 seconds | T_L | | | 300 | $^\circ C$ |

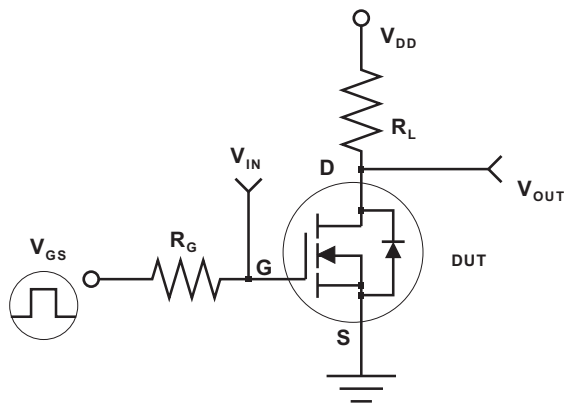
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Electrical characteristics (AT $T_A=25^\circ\text{C}$ unless otherwise noted)

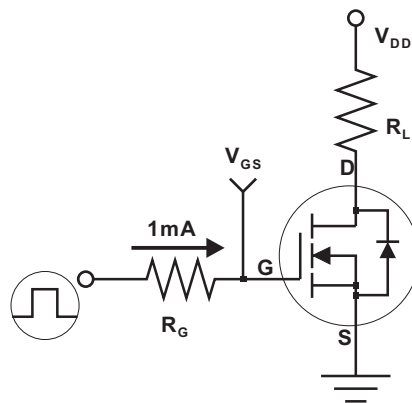
| Parameter | Conditions | Symbol | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|---|---------------|------|------|---------------|----------|
| Drain-source breakdown voltage | $V_{GS} = 0V, I_D = 10\mu A$ | $V_{(BR)DSS}$ | 60 | | | V |
| Drain-source leakage current | $V_{DS} = 60V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ | I_{DSS} | | | 1.0 | μA |
| | | | | | 0.5 | mA |
| Gate-source leakage current-forward | $V_{GSF} = 20V$ | I_{GSS} | | | 100 | nA |
| Gate-source leakage current-reverse | $V_{GSF} = -20V$ | I_{GSS} | | | -100 | nA |
| Gate threshold voltage* | $V_{DS} = V_{GS}, I_D = 250\mu A$ | $V_{GS(th)}$ | 1.0 | | 2.5 | V |
| On-state drain current | $V_{DS} \geq 20V_{DS(on)}, V_{GS} = 10V$ | $I_{D(on)}$ | 500 | | | mA |
| Static drain-source on-resistance* | $V_{GS} = 10V, I_D = 0.5A, T_J = 125^\circ\text{C}$ $V_{GS} = 5.0V, I_D = 50mA, T_J = 125^\circ\text{C}$ | $R_{DS(on)}$ | | | 7.5 | Ω |
| | | | | | 13.5 | |
| | | | | | 7.5 | |
| | | | | | 13.5 | |
| Drain-source on-voltage* | $V_{GS} = 10V, I_D = 0.5A, V_{GS} = 5.0V, I_D = 50mA$ | $V_{DS(on)}$ | | | 3.75 0.375 | V |
| Forward transconductance | $V_{DS} \geq 2V_{DS(on)}, I_D = 200mA^*$ | g_{FS} | 80 | | | ms |
| Input capacitance | $V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz$ | C_{iss} | | | 50 | pF |
| Output capacitance | | C_{oss} | | | 25 | |
| Reverse transfer capacitance | | C_{rss} | | | 5.0 | |
| Turn-on delay time | $V_{DD} = 25V, I_D = 500mA, V_{gen} = 10V, R_G = 25\Omega, R_L = 50\Omega^*$ | $t_{d(on)}$ | | 9 | 15 | ns |
| Turn-off delay time | | $t_{d(off)}$ | | 21 | 26 | |
| Diode forward on-voltage | $I_S = 115mA, V_{GS} = 0V$ | V_{SD} | | 0.93 | 1.2 | V |
| Source current continuous | Body diode | I_S | | | 250 | mA |
| Source current pulsed | | I_{SM} | | | 800 | mA |

*Pules test : Pules width $\leq 300\mu s$, duty cycle $\leq 2\%$

Switching Test Circuit



Gate Charge Test Circuit



Rating and characteristic curves (2N7002W)

FIG.1 TYPICAL FORWARD CHARACTERISTIC

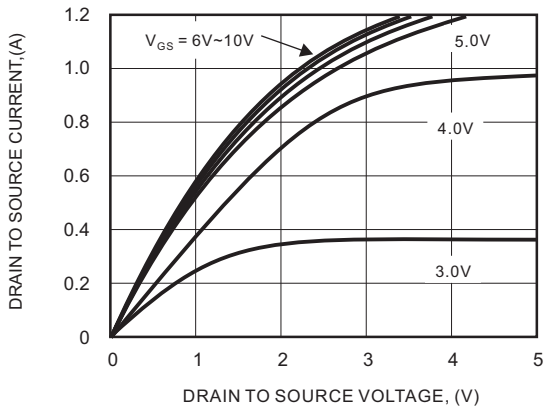


FIG.2 TRANSFER CHARACTERISTIC

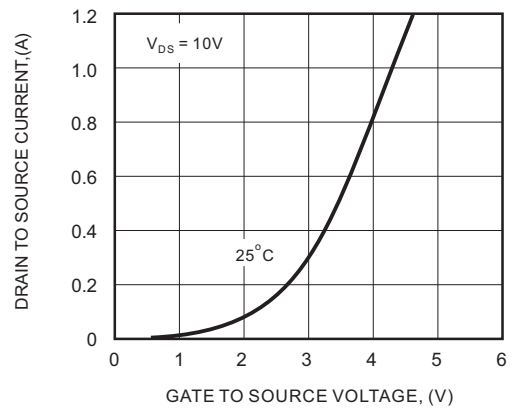


FIG.3 ON RESISTANCE VS DRAIN CURRENT

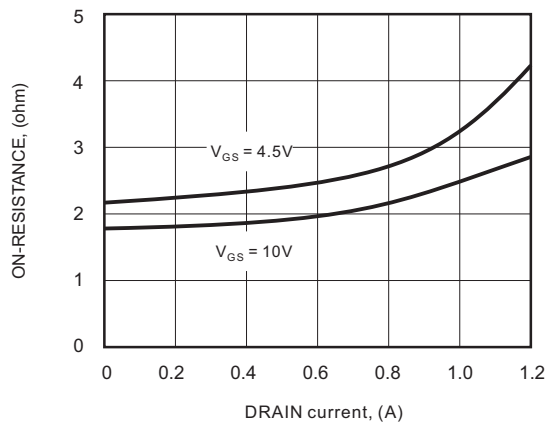


FIG.4 ON RESISTANCE VS GATE TO SOURCE VOLTAGE

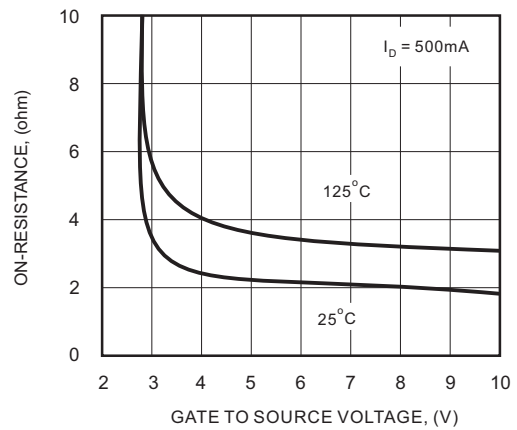
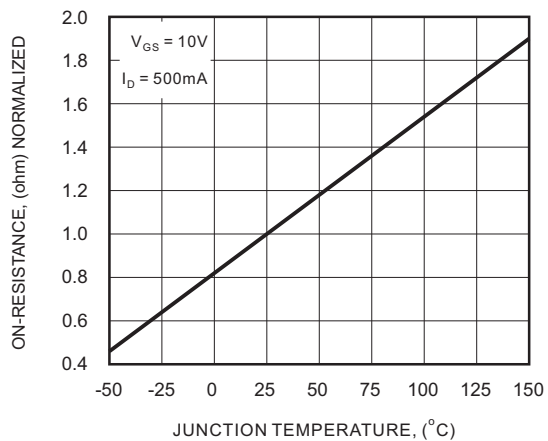


FIG.5 ON RESISTANCE VS JUNCTION TEMPERATURE



Rating and characteristic curves (2N7002W)

FIG.6 GATE CHARGE WAVEFORM

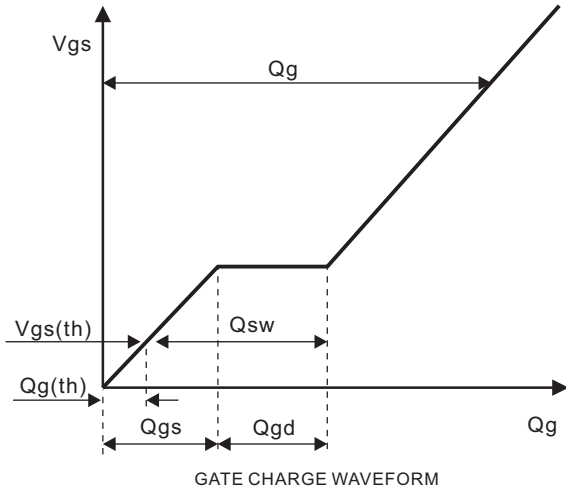


FIG.7 GATE CHARGE

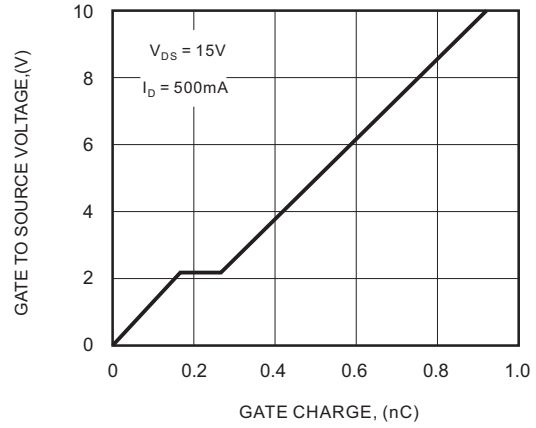


FIG.8 THRESHOLD VOLTAGE VS TEMPERATURE

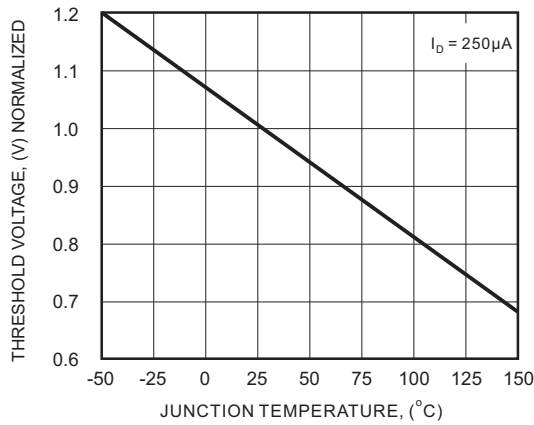


FIG.9 BREAKDOWN VOLTAGE VS JUNCTION TEMPERATURE

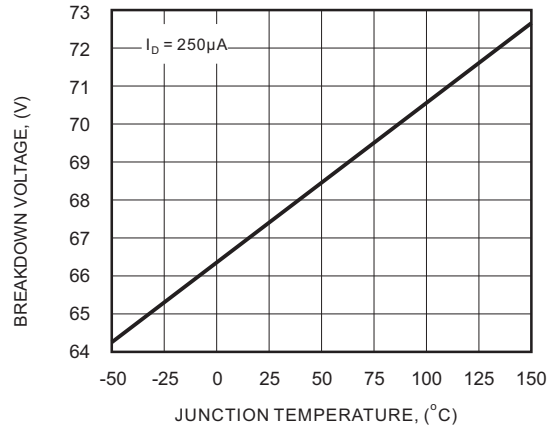
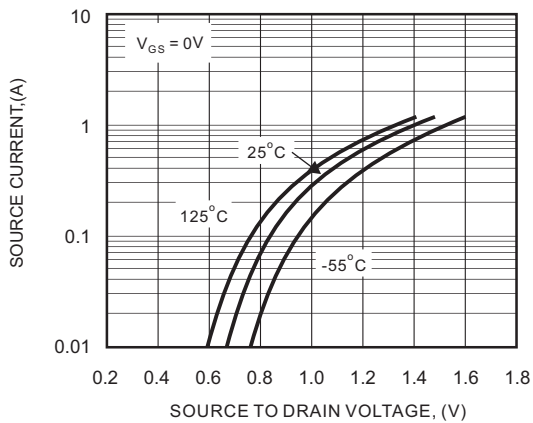
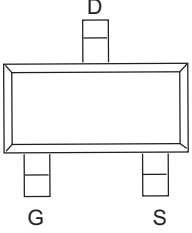
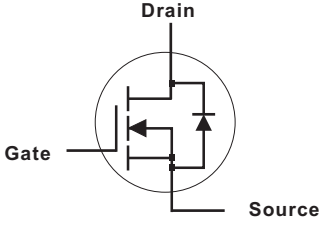


FIG.10 SOURCE-DRAIN DIODE FORWARD VOLTAGE



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Pinning information

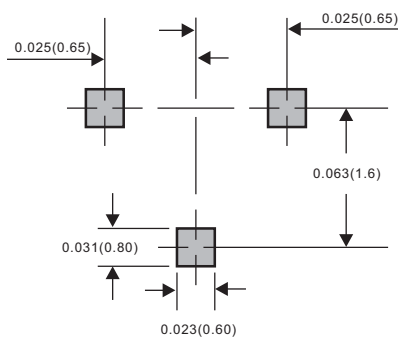
| Pin | Simplified outline | Symbol |
|--|---|---|
| PinD Drain PinG Gate PinS Source |  |  |

Marking

| Type number | Marking code |
|-------------|--------------|
| 2N7002W | 72,E72 |

Suggested solder pad layout

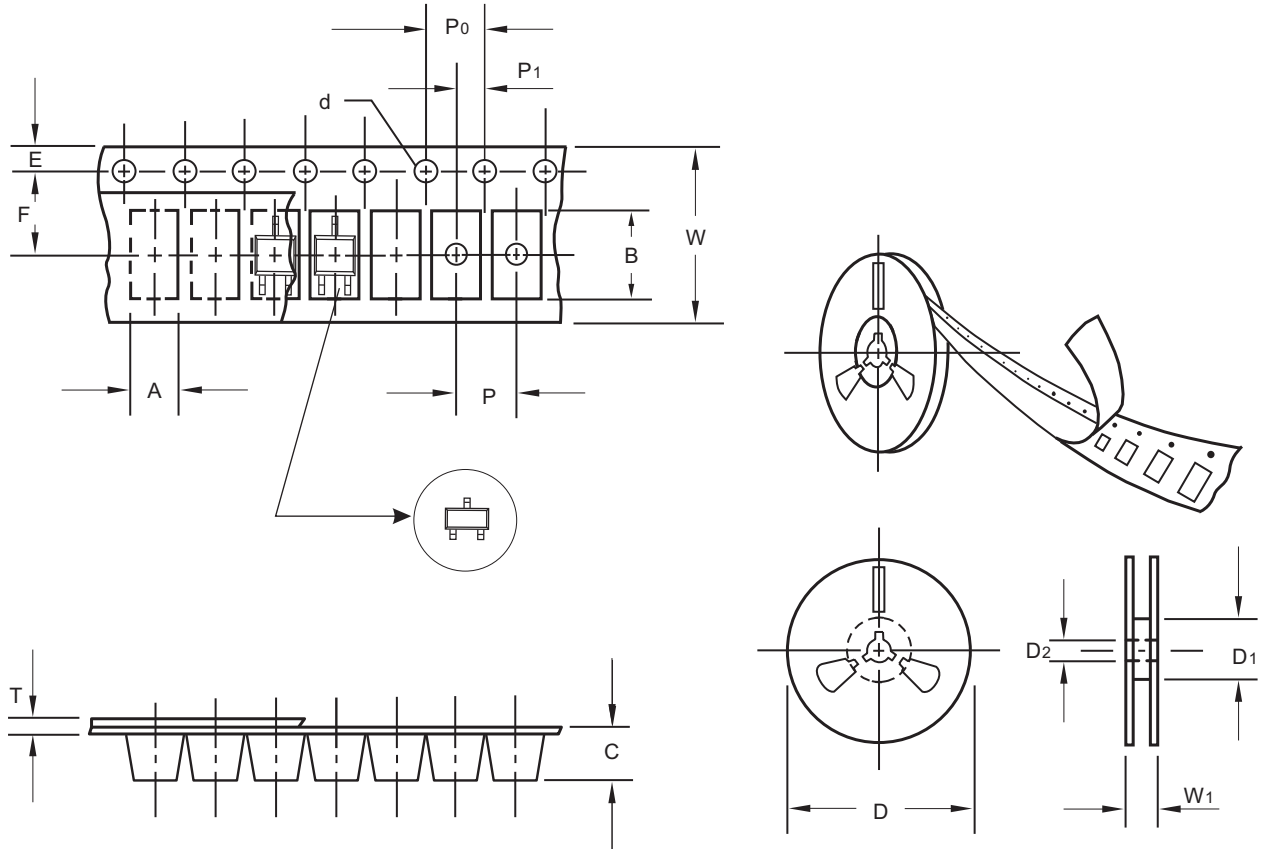
SOT-323



Dimensions in inches and (millimeters)

2N7002W

Packing information



unit:mm

| Item | Symbol | Tolerance | SOT-323 |
|---------------------------|--------|-----------|---------|
| Carrier width | A | 0.1 | 1.47 |
| Carrier length | B | 0.1 | 2.95 |
| Carrier depth | C | 0.1 | 1.15 |
| Sprocket hole | d | 0.1 | 1.50 |
| 13" Reel outside diameter | D | 2.0 | - |
| 13" Reel inner diameter | D1 | min | - |
| 7" Reel outside diameter | D | 2.0 | 178.00 |
| 7" Reel inner diameter | D1 | min | 62.00 |
| Feed hole diameter | D2 | 0.5 | 13.00 |
| Sprocket hole position | E | 0.1 | 1.75 |
| Punch hole position | F | 0.1 | 3.50 |
| Punch hole pitch | P | 0.1 | 4.00 |
| Sprocket hole pitch | P0 | 0.1 | 4.00 |
| Embossment center | P1 | 0.1 | 2.00 |
| Overall tape thickness | T | 0.1 | 0.23 |
| Tape width | W | 0.3 | 8.00 |
| Reel width | W1 | 1.0 | 11.40 |

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

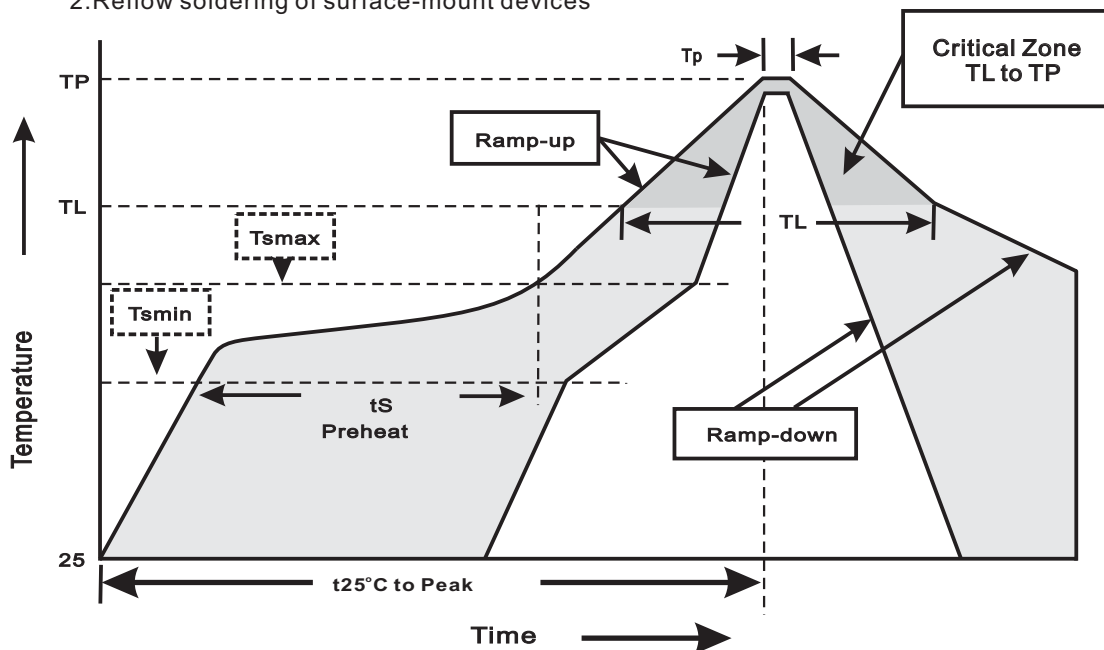
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Reel packing

| PACKAGE | REEL SIZE | REEL (pcs) | COMPONENT SPACING (m/m) | BOX (pcs) | INNER BOX (m/m) | REEL DIA, (m/m) | CARTON SIZE (m/m) | CARTON (pcs) | APPROX. GROSS WEIGHT (kg) |
|---------|-----------|------------|-------------------------|-----------|-----------------|-----------------|-------------------|--------------|---------------------------|
| SOT-323 | 7" | 3,000 | 4.0 | 30,000 | 183*123*183 | 178 | 382*257*387 | 240,000 | 9.5 |

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

| Profile Feature | Soldering Condition |
|--|-----------------------------|
| Average ramp-up rate(T _L to T _P) | <3°C/sec |
| Preheat -Temperature Min(T _{Amin}) -Temperature Max(T _{Smax}) -Time(min to max)(t _S) | 150°C 200°C 60~120sec |
| T _{Smax} to T _L -Ramp-upRate | <3°C/sec |
| Time maintained above: -Temperature(T _L) -Time(t _L) | 217°C 60~260sec |
| Peak Temperature(T _P) | 255°C-0/+5°C |
| Time within 5°C of actual Peak Temperature(t _P) | 10~30sec |
| Ramp-down Rate | <6°C/sec |
| Time 25°C to Peak Temperature | <6minutes |

2N7002W**High reliability test capabilities**

| Item Test | Conditions | Reference |
|----------------------------------|---|-----------------------------|
| 1. Solder Resistance | at $260\pm 5^{\circ}\text{C}$ for 10 sec. | MIL-STD-750D METHOD-2031 |
| 2. Solderability | at $245\pm 5^{\circ}\text{C}$ for 5 sec. | MIL-STD-202F METHOD-208 |
| 3. High Temperature Reverse Bias | $V_{\text{DS}}=0.8 \times BV_{\text{DSS}}$, at $T_{\text{J}}=150^{\circ}\text{C}$ for 168 hrs. | MIL-STD-750D METHOD-1038 |
| 4. Pressure Cooker | $15P_{\text{SIG}}$ at $T_{\text{A}}=121^{\circ}\text{C}$ 100%RH for 4 hrs. | JESD22-A102 |
| 5. Temperature Cycling | -55°C to $+125^{\circ}\text{C}$ dwelled for 30 min total 10 cycles. | MIL-STD-750D METHOD-1051 |
| 6. Humidity | at $T_{\text{A}}=85^{\circ}\text{C}$, 85%RH for 1000 hrs. | MIL-STD-750D METHOD-1021 |
| 7. High Temperature Storage Life | at $T_{\text{A}}=175^{\circ}\text{C}$ for 1000 hrs. | MIL-STD-750D METHOD-1031 |