

2N7002K

List

List..... 1

Package outline..... 2

Features..... 2

Mechanical data..... 2

Maximum ratings 2

Electrical characteristics..... 3

Rating and characteristic curves..... 4~5

Pinning information..... 6

Marking..... 6

Suggested solder pad layout..... 6

Packing information..... 7

Reel packing..... 8

Suggested thermal profiles for soldering processes..... 8

High reliability test capabilities..... 9

2N7002K

60V N-Channel Enhancement Mode MOSFET- ESD Protection

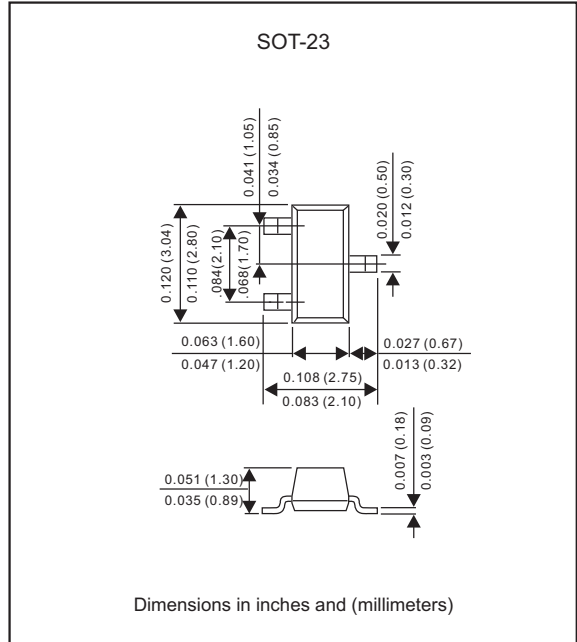
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@500mA=3.0 \Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@200mA=4.0 \Omega$
- ESD protection 2kV (Human body mode)
- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Very low leakage current in off condition
- Specially designed for battery operated system, solid-state relays drivers, relays, displays, lamps, solenoids, memories, etc
- Lead-free parts meet RoHS requirements
- Suffix "-H" indicates Halogen-free part, ex. 2N7002K-H

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-23
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.008 gram

Package outline



Maximum ratings (AT $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-Source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current	I_D	300	mA
Pulsed drain current ¹⁾	I_{DM}	2000	mA

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Total power dissipation	P_D			0.35 0.21	W
Operation junction and storage temperature range	T_J, T_{STG}	-55		+150	$^\circ C$
Thermal resistance(PCB mounted) ²⁾	$R_{\theta JA}$		357		$^\circ C/W$

Notes 1: Maximum DC current limited by package
 2: Surface mounted on FR4 board, $t < 5$ sec

2N7002K

Electrical characteristics (AT $T_A=25^\circ\text{C}$ unless otherwise noted)

STATIC

Parameter	Conditions	Symbol	MIN.	TYP.	MAX.	Unit
Drain-source breakdown voltage	$V_{GS}=0V, I_D=10\mu A$	BV_{DSS}	60			V
Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	$V_{GS(th)}$	1.0		2.5	V
Drain-source on-state resistance	$V_{GS}=10V, I_D=500mA$	$R_{DS(on)}$			3.0	Ω
	$V_{GS}=4.5V, I_D=200mA$				4.0	
Zero gate voltage drain current	$V_{DS}=60V, V_{GS}=0V$	I_{DSS}			1	μA
Gate-body leakage current	$V_{GS}=\pm 20V, V_{DS}=0V$	I_{GSS}			± 10	μA
Forward transconductance	$V_{DS}=15V, I_D=250mA$	g_{fs}	100			ms

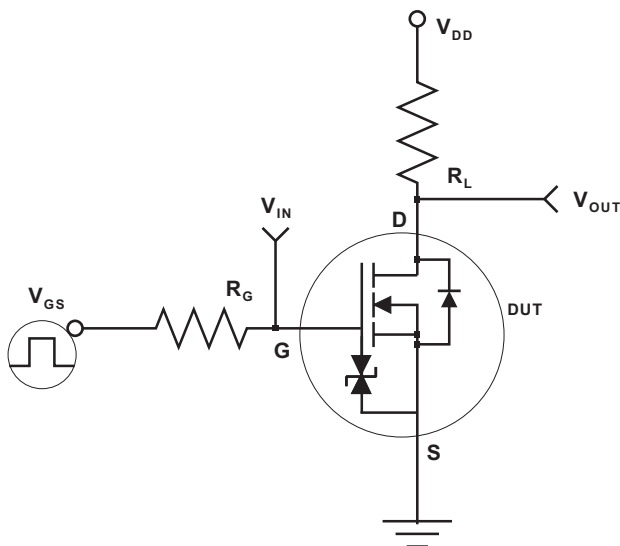
DYNAMIC

Total gate charge	$V_{DS}=15V, I_D=200mA, V_{GS}=4.5V$	Q_g			0.8	nC
Turn-on delay time	$V_{DD}=30V, R_L=150\Omega, I_D=200mA, V_{gen}=10V, R_G=10\Omega$	t_{on}			20	ns
Turn-off delay time		t_{off}			40	
Input capacitance	$V_{DS}=25V, V_{GS}=0V, f=1.0\text{ MHz}$	C_{iss}			35	μF
Output capacitance		C_{oss}			10	
Reverse transfer capacitance		C_{rss}			5	

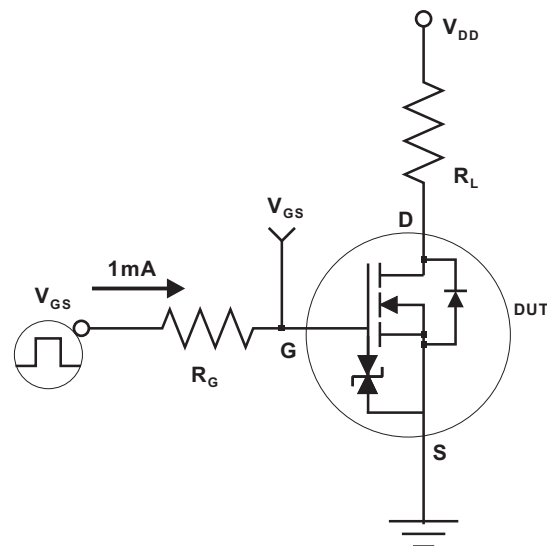
SOURCE-DRAIN DIODE

Diode forward voltage	$I_S=200mA, V_{GS}=0V$	V_{SD}		0.82	1.3	V
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Switching Test Circuit



Gate Charge Test Circuit



Rating and characteristic curves (2N7002K)

Fig.1 Output Characteristic

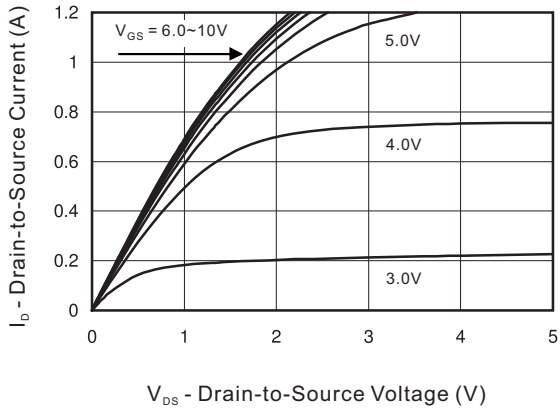


Fig.2 Transfer Characteristic

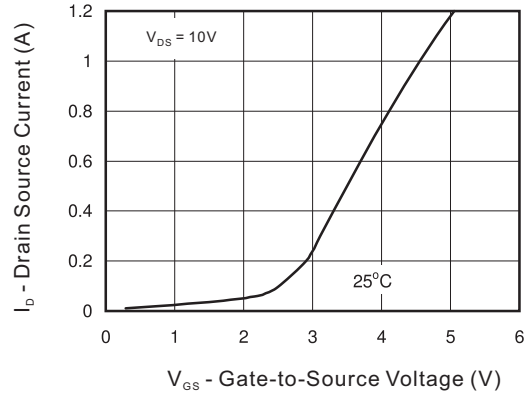


Fig.3 On Resistance vs Drain Current

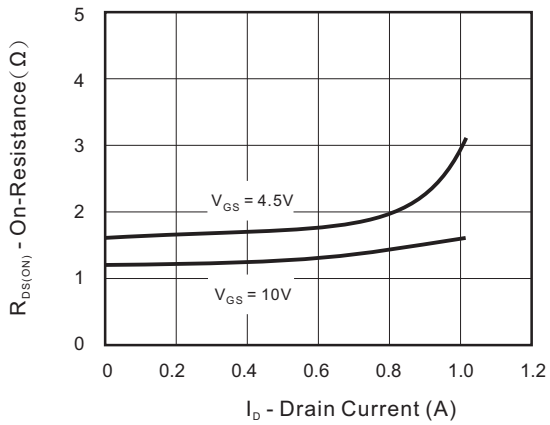


Fig.4 On Resistance vs Gate to Source Voltage

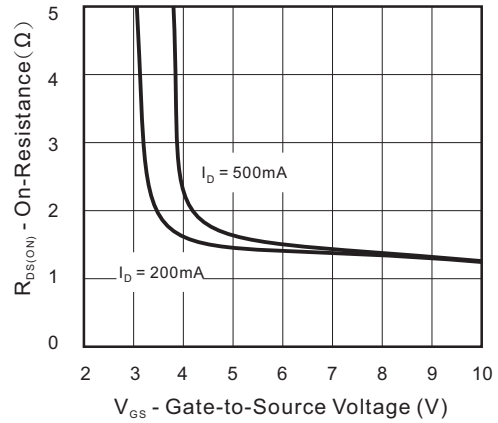
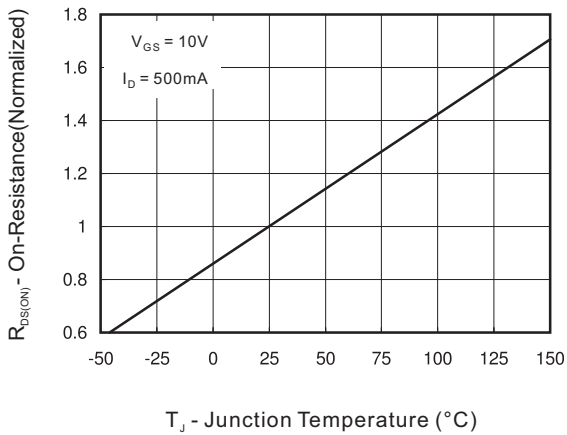


Fig.5 On Resistance vs Junction Temperature



Rating and characteristic curves (2N7002K)

Fig. 6 Gate Charge Waveform

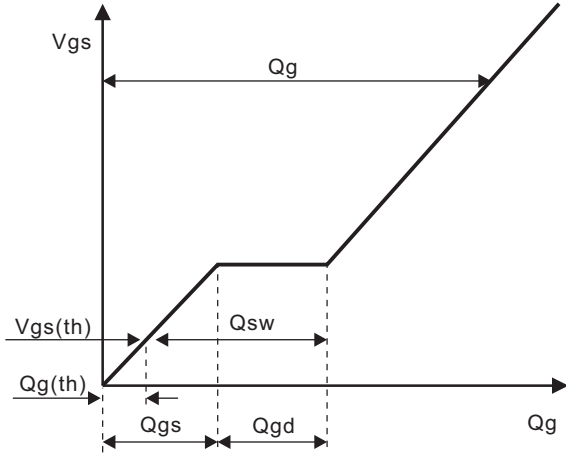


Fig.7 Gate Charge

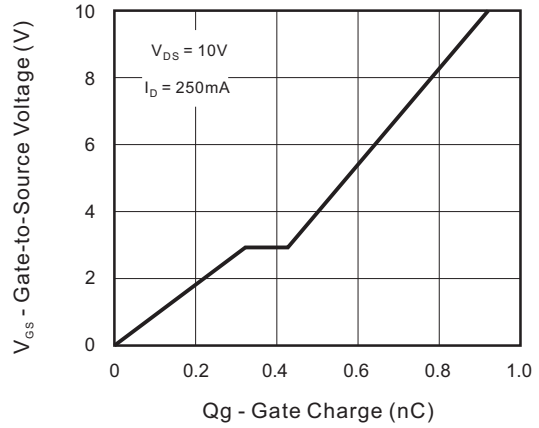


Fig.8 Threshold Voltage vs Temperature

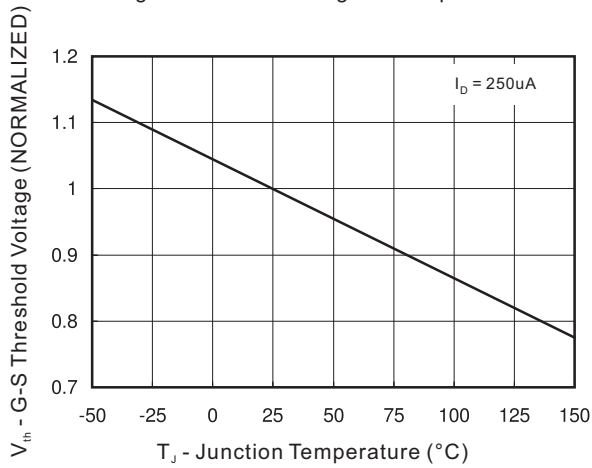


Fig.9 Breakdown Voltage vs Junction Temperature

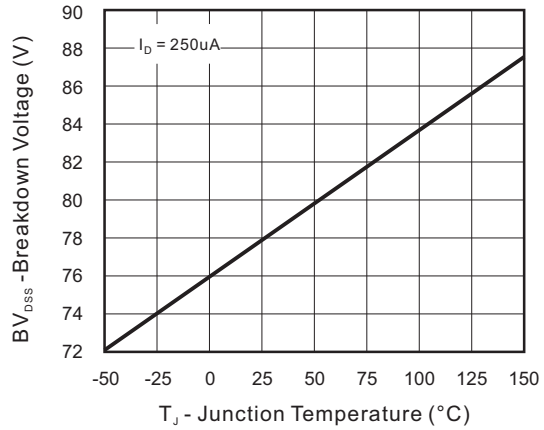
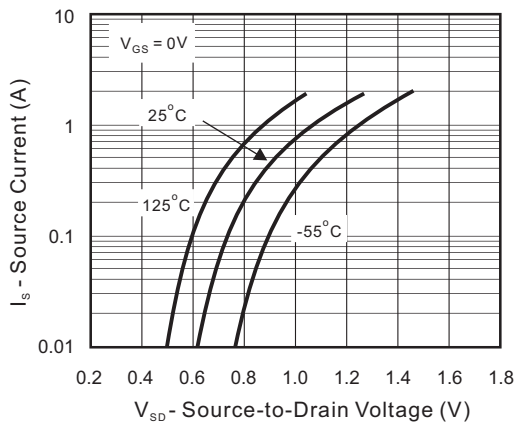
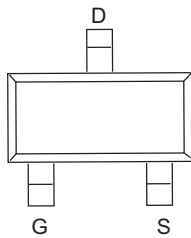
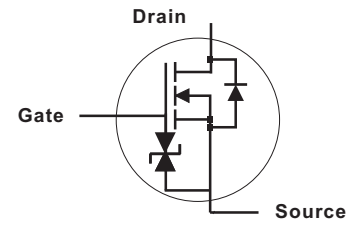


Fig.10 Source-Drain Diode Forward Voltage



2N7002K

Pinning information

Pin	Simplified outline	Symbol
PinD Drain PinG Gate PinS Source		

Marking

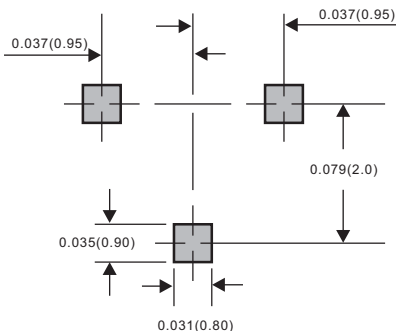
Type number	Marking code
2N7002K	K72Σ (Note 1)
	RKΣ (Note 1)
	D73Σ (Note 1)
	72K

Note 1: M = Month code

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Odd Year	1	2	3	4	5	6	7	8	9	T	V	C
Even Year	E	F	H	J	K	L	N	P	U	X	Y	Z

Suggested solder pad layout

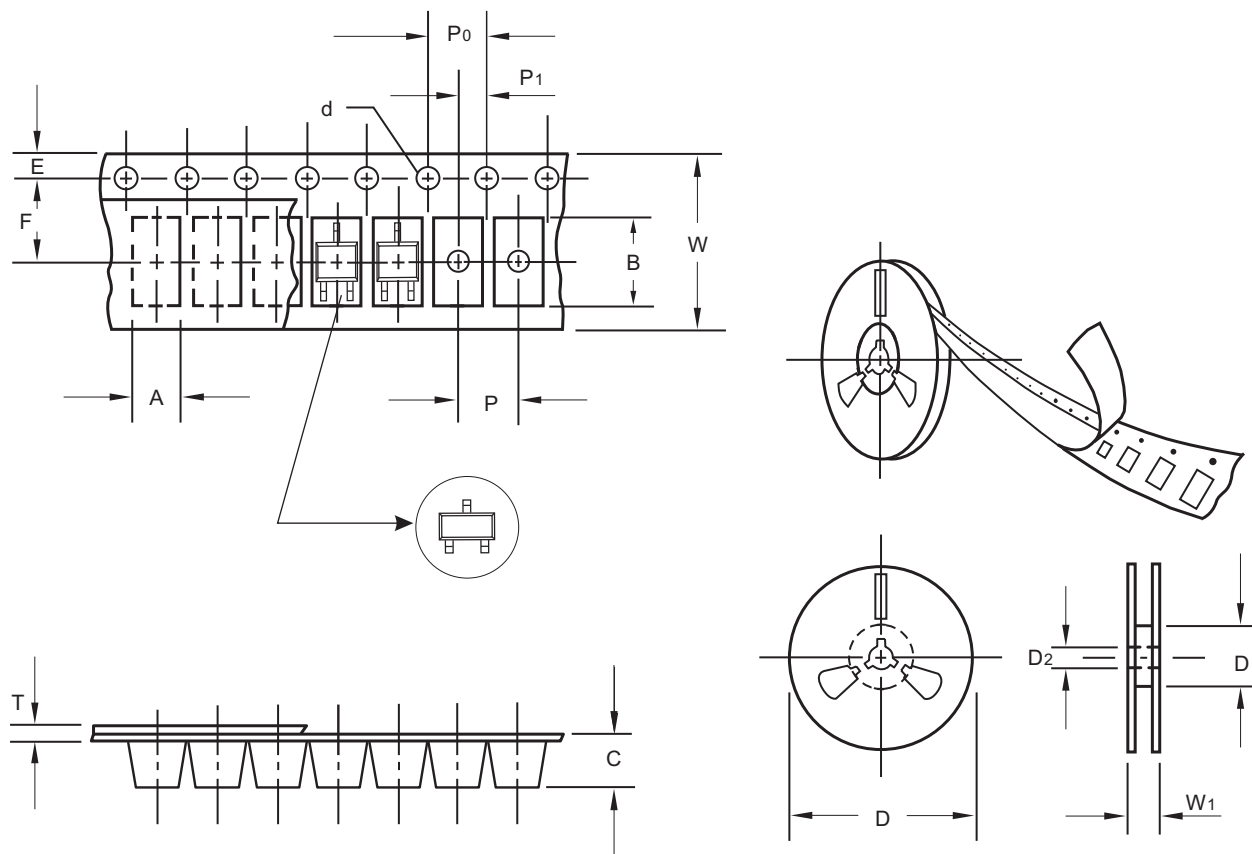
SOT-23



Dimensions in inches and (millimeters)

2N7002K

Packing information



unit:mm

Item	Symbol	Tolerance	SOT-23
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D1	min	55.00
Feed hole diameter	D2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P0	0.1	4.00
Embossment center	P1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W1	1.0	12.0

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

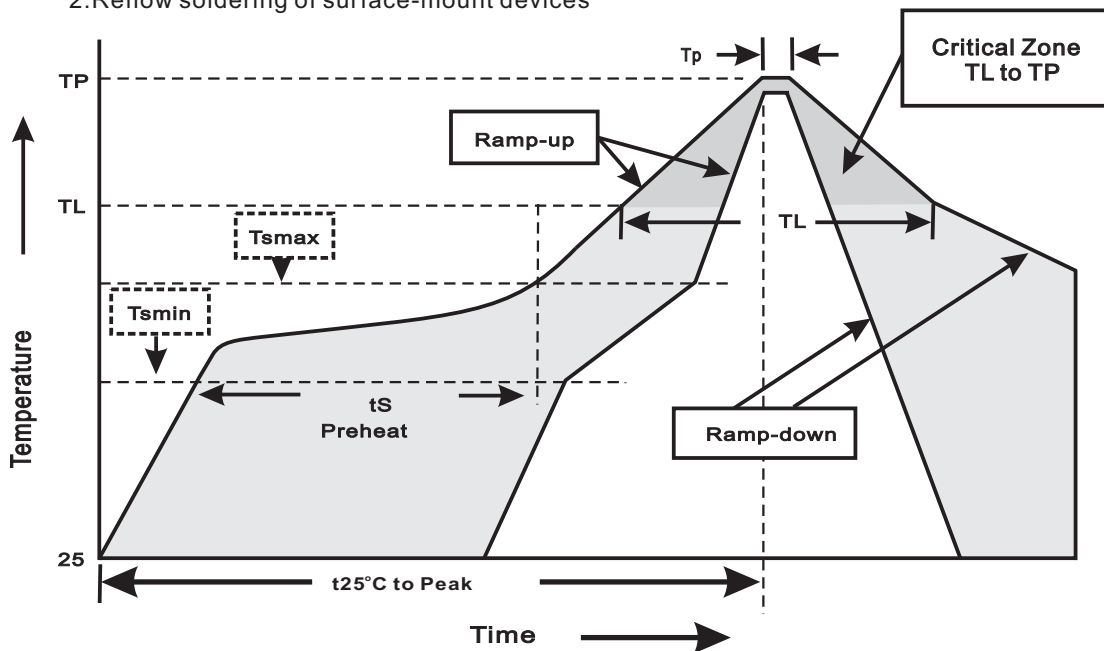
2N7002K

Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-23	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000	11.6

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T _L to T _P)	<3°C/sec
Preheat -Temperature Min(T _{min}) -Temperature Max(T _{max}) -Time(min to max)(t _s)	150°C 200°C 60~120sec
T _{max} to T _L -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(T _L) -Time(t _L)	217°C 60~260sec
Peak Temperature(T _P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t _P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes

2N7002K

High reliability test capabilities

Item Test	Conditions	Reference
1. High Temperature Gate Bias	Ta=150°C Vgs=0, 8 x BVGSS for 1000hours	JESD22-A108-C
2. High Temperature Reverse Bias	Ta=150°C Vds=0, 8 x BVDSS for 1000hours	JESD22-A108-C
3. Solder ability Test	Temp=245°C for 5sec	JESD22-B102-D
4. Pressure Cooker Test	Ta=121°C / 100%RH Pressure=2Atm for 168hours	JESD22-A102-C
5. Temperature Cycle Test	-65°C / 10min~ 150°C / 10min Transfer<5min. total 1000 cycles.	JESD22-A104-B
6. Temperature Humidity Test	Ta=85°C Humidity=85%RH for 1000hours	JESD22-A101-B
7. High Temperature Storage Test	Ta=150°C for 1000hours	JESD22-B103-B