2N7002DW

List

2N7002DW

60V Dual N-Channel Enhancement Mode MOSFET

Features

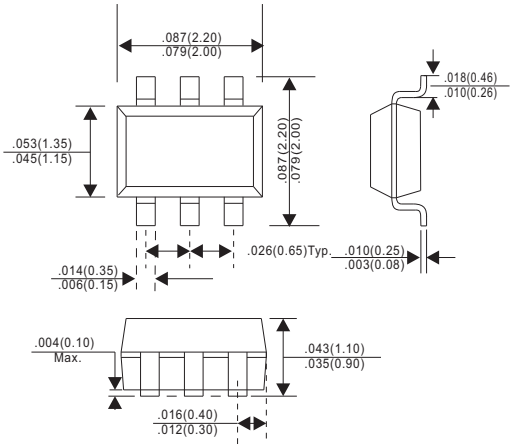
- $R_{DS(ON)}$, V_{GS}@10V, I_{DS}@500mA=3.5Ω(typ.)
- $R_{DS(ON)}$, V_{GS}@4.5V, I_{DS}@300mA=4.0Ω(typ.)
- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Specially designed for battery operated system, solid-state relays drivers, relays, displays, lamps, solenoids, memories, etc
- In compliance with EU RoHS 2011/65/EU directives
- Suffix "-H" indicates Halogen-free part, ex. 2N7002DW-H

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-363
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Polarity : See Diagram
- Mounting Position : Any
- Weight : Approximated 0.006 gram

Package outline

SOT-363



Dimensions in inches and (millimeters)

Maximum ratings (AT T_A=25°C unless otherwise noted)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Drain-source voltage	V_{DSS}			60	V
Drain to current-continue	I_D			±300	mA
-pulsed	I_{DM}			±1000	
Gate to source voltage-continue	V_{GS}			±20	V
-non-repetitive (tp<50μs)	V_{GSS}			±40	
Total power dissipation (Derate above 25°C)	P_D			350	mW
Junction to ambient thermal resistance	$R_{\theta JA}$			375	°C/W
Operation junction temperature range	T_J	-55		+150	°C
Storage temperature range	T_{STG}	-55		+150	°C

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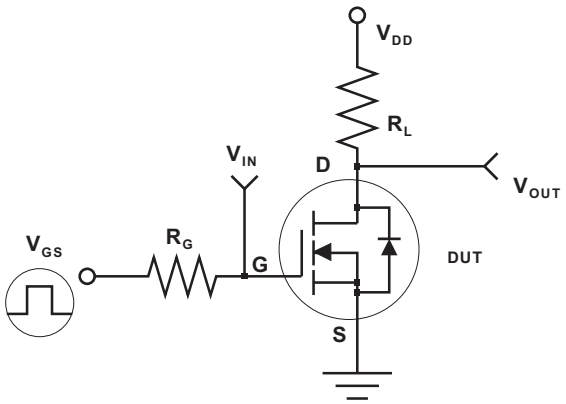
Electrical characteristics (At T_A=25°C unless otherwise noted)

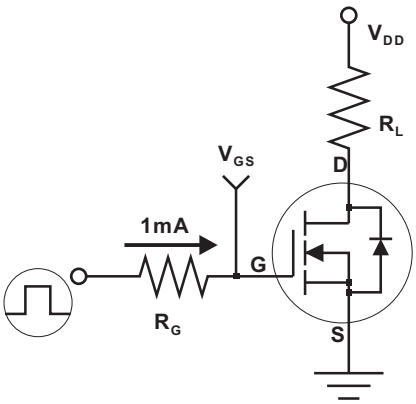
Parameter	Conditions	Symbol	MIN.	TYP.	MAX.	Unit
OFF CHARACTERISTICS						
Drain-source breakdown voltage	V_{GS} = 0V, I_D= 10μA	B_{VDSS}	60			V
Zero gate voltage drain current	V_{DS} = 60V, V_{GS} = 0V	I_{DSS}			1.0	μA
	V_{DS} = 60V, V_{GS} = 0V, T_J = 125°C				10	
Gate-body leakage current-forward	V_{GS} = 20V, V_{DS} = 0	I_{GSSF}			100	nA
Gate-body leakage current-reverse	V_{GS} = -20V, V_{DS} = 0	I_{GSSR}			-100	nA
ON CHARACTERISTICS (Note 1)						
Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(th)}$	1.0	1.7	2.5	V
Static drain-source on-resistance	V_{GS} = 10V, I_D = 0.5A	$R_{DS(ON)}$		3.5	5.0	Ω
	V_{GS} = 4.5V, I_D= 300mA			4.0	6.0	
Source-drain current		I_{SD}			0.35	A
Source-drain current (pulse), Note 2		I_{SDM}			1.40	A
Forward transconductance, Note 1	V_{DS} =10V, I_D = 500mA*	g_{fs}		0.6		sec
Diodes foward voltage, Note 1	V_{DS} =0V, I_S = 0.12mA*			0.85	1.50	V
DYNAMIC CHARACTERISTICS						
Intput capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}		43		pF
Output capacitance		C_{oss}		20		
Reverse transfer capacitance		C_{rss}		6		
Total gate charge	V_{DS} = 30V, I_D = 1.0A, V_{GS} = 5.0V	Q_g		1.4	2.0	nC
Gate-source charge		Q_{gs}		0.8		
Gate-drain charge		Q_{gd}		0.5		
Turn-on delay time	V_{DD} = 30V, R_G = 4.7Ω, I_D = 500mA, V_{GS} = 4.5V	$t_{d(on)}$		6		ns
		t_r		5		
Turn-off delay time		$t_{d(off)}$		15		
		t_r		6		

Notes 1: Pulse duration = 300μs, duty cycle 1.5%
2: Pulse width limited by safe operating area.

Switching Test Circuit



Gate Charge Test Circuit



Rating and characteristic curves (2N7002DW)

FIG.1 TYPICAL FORWARD CHARACTERISTIC

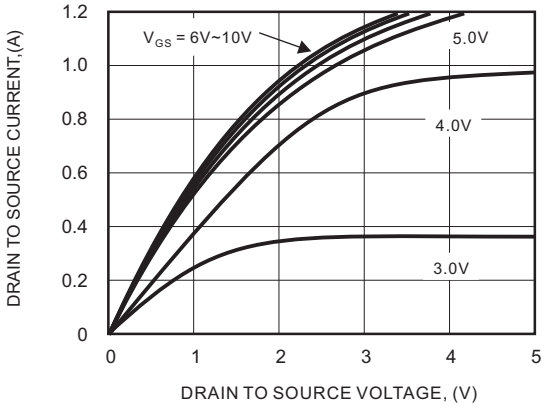


FIG.2 TRANSFER CHARACTERISTIC

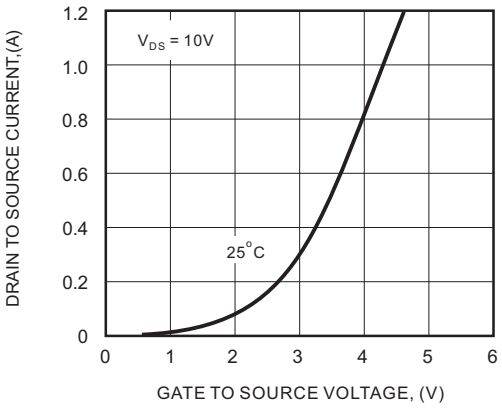


FIG.3 ON RESISTANCE VS DRAIN CURRENT

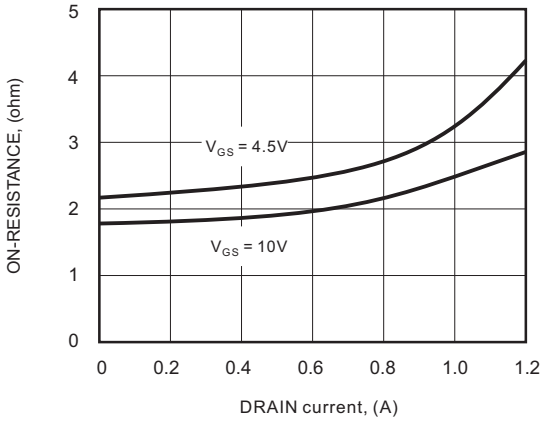


FIG.4 ON RESISTANCE VS GATE TO SOURCE VOLTAGE

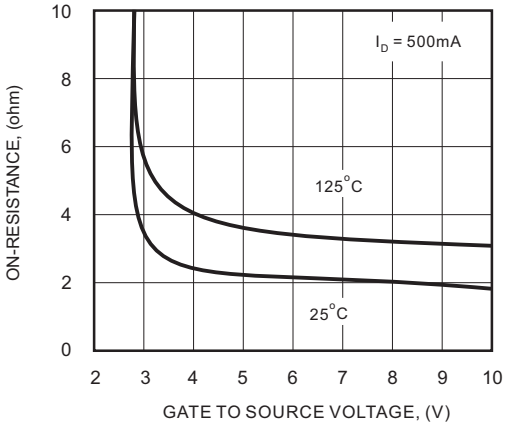
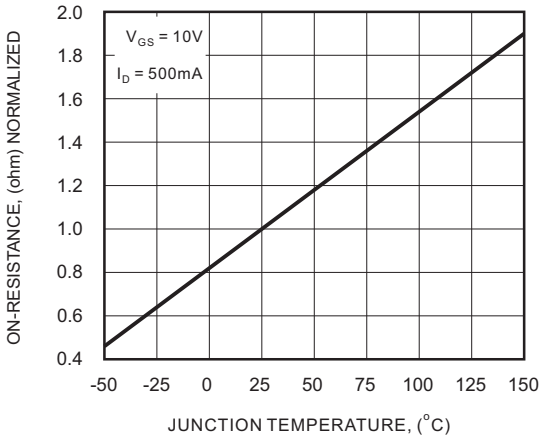


FIG.5 ON RESISTANCE VS JUNCTION TEMPERATURE



Rating and characteristic curves (2N7002DW)

FIG.6 GATE CHARGE WAVEFORM

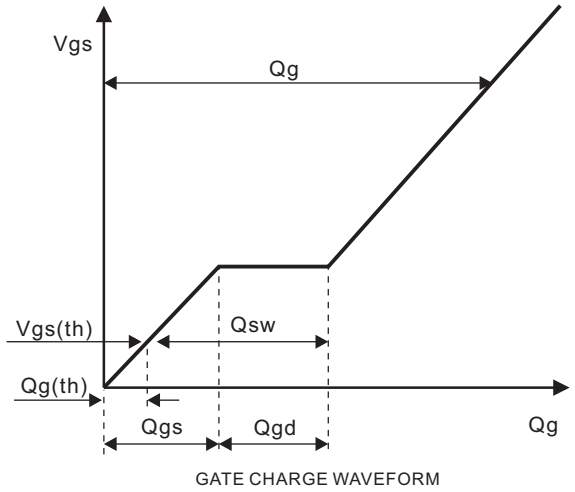


FIG.7 GATE CHARGE

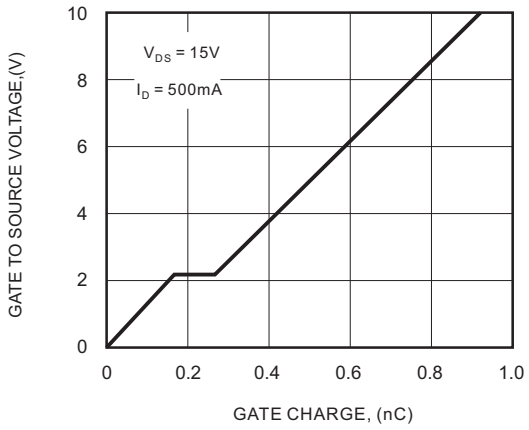


FIG.8 THRESHOLD VOLTAGE VS TEMPERATURE

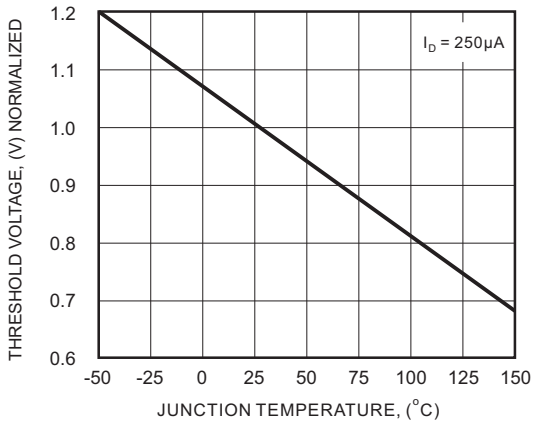


FIG.9 BREAKDOWN VOLTAGE VS JUNCTION TEMPERATURE

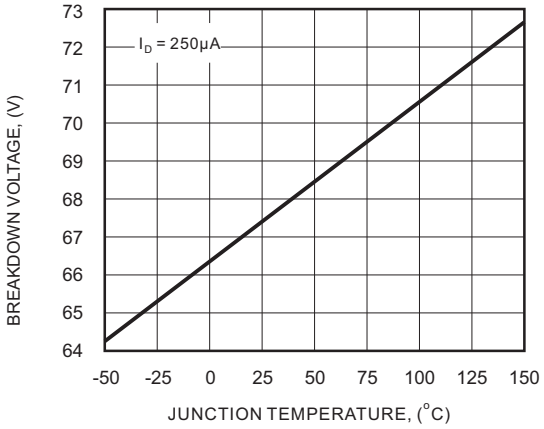
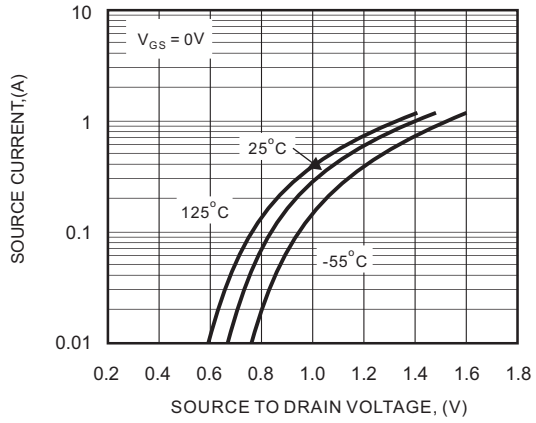


FIG.10 SOURCE-DRAIN DIODE FORWARD VOLTAGE



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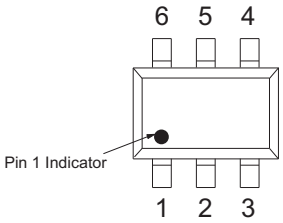
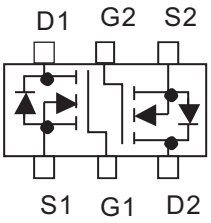
Pinning information

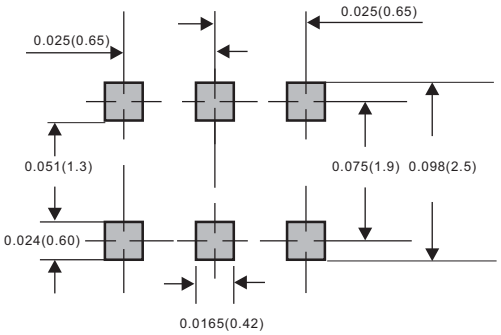
Pin	Simplified outline	Symbol
Pin 1 Source1 Pin 2 Gate1 Pin 3 Drain2 Pin 4 Source2 Pin 5 Gate2 Pin 6 Drain1		

Marking

Type number	Marking code
2N7002DW	702,E76

Suggested solder pad layout

SOT-363



Dimensions in inches and (millimeters)

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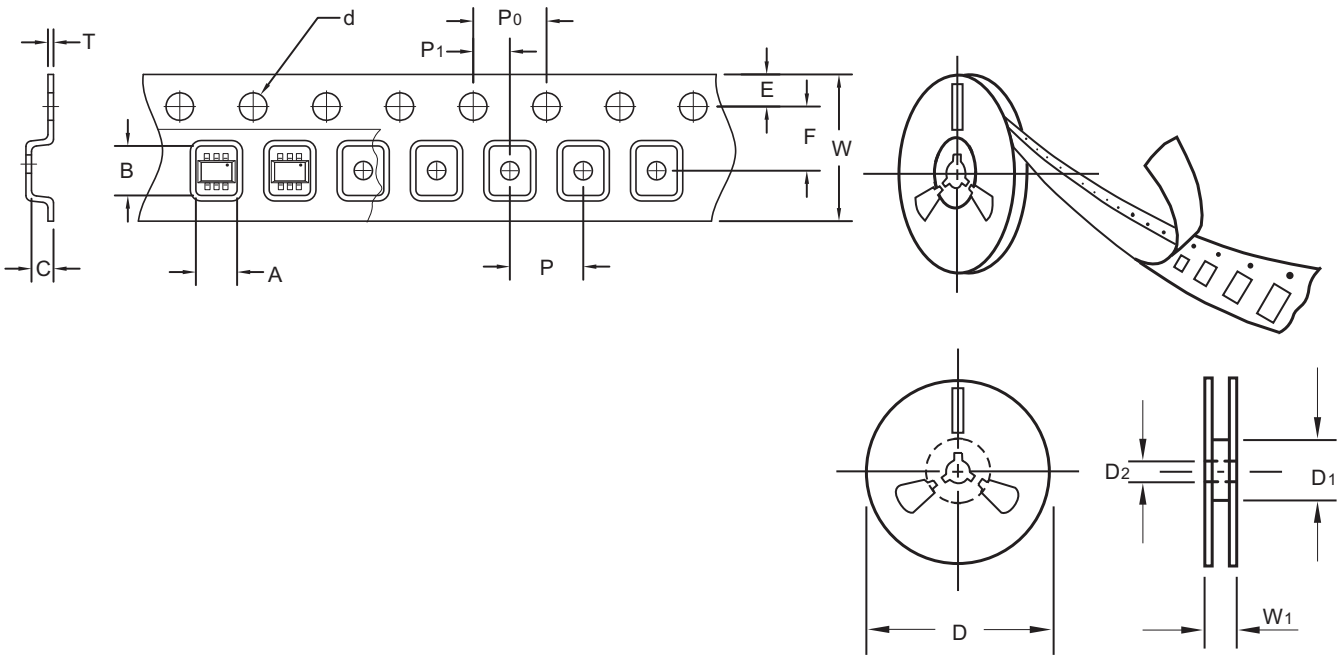
Packing information



unit:mm

Item	Symbol	Tolerance	SOT-363
Carrier width	A	0.1	2.25
Carrier length	B	0.1	2.55
Carrier depth	C	0.1	1.20
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D_1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D_1	min	54.40
Feed hole diameter	D_2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P_0	0.1	4.00
Embossment center	P_1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W_1	1.0	12.3

Note:Devices are packed in accor dance with EIA standar RS-481-A and specifications listed above.

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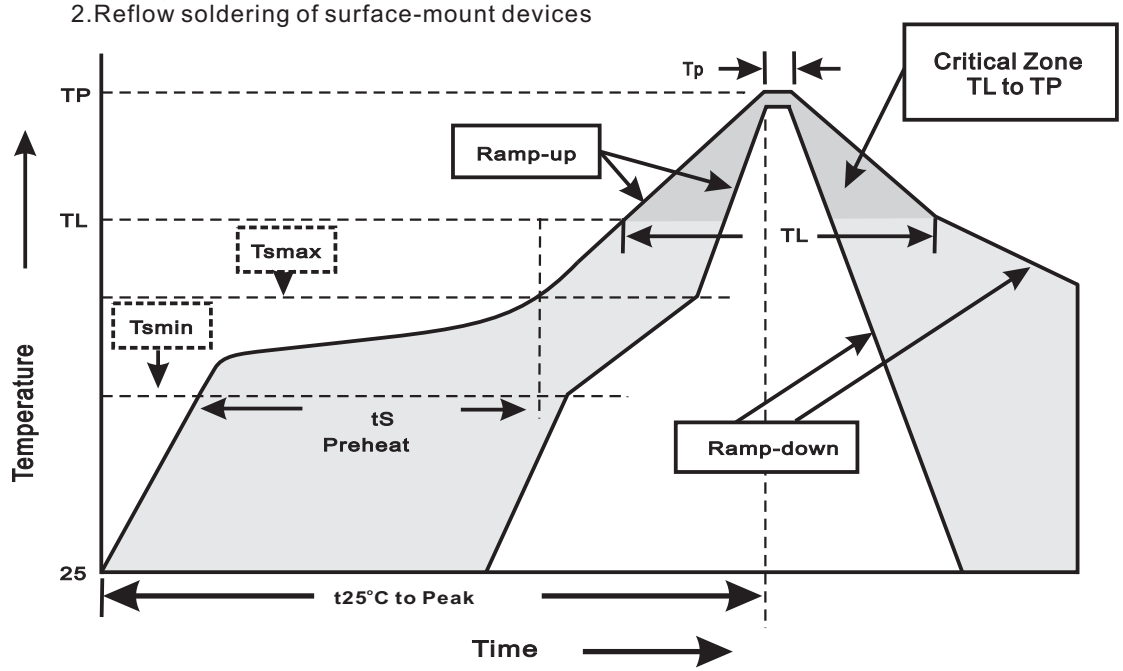
Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-363	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000	9.50

Suggested thermal profiles for soldering processes

1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%

2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	<3°C/sec
Preheat -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time(min to max)(t_s)	 150°C 200°C 60~120sec
Tsmax to T_L -Ramp-upRate	 <3°C/sec
Time maintained above: -Temperature(T_L) -Time(t_L)	 217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes

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High reliability test capabilities

Item Test	Conditions	Reference
1. Solder Resistance	at 260±5°C for 10 sec.	MIL-STD-750D METHOD-2031
2. Solderability	at 245±5°C for 5 sec.	MIL-STD-202F METHOD-208
3. High Temperature Reverse Bias	V_{DS}=0.8 X BV_{DSS}, at T_J=150°C for 168 hrs.	MIL-STD-750D METHOD-1038
4. Pressure Cooker	15P_{SIG} at T_A=121°C 100%RH for 4 hrs.	JESD22-A102
5. Temperature Cycling	-55°C to +125°C dwelled for 30 min total 10 cycles.	MIL-STD-750D METHOD-1051
6. Humidity	at T_A=85°C, 85%RH for 1000 hrs.	MIL-STD-750D METHOD-1021
7. High Temperature Storage Life	at T_A=175°C for 1000 hrs.	MIL-STD-750D METHOD-1031