

LL054BT6

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LL054BT6

4-Channel Low Capacitance ESD Protection Diodes Array- 5.0V

Features

- 4 channels of ESD protection
- Provide transient protection:
IEC 61000-4-2 (ESD) level 4
IEC 61000-4-4 (EFT) 80A (5/50ns)
IEC 61000-4-5 (Surge) (8/20us)
- Channel I/O to GND capacitance: 0.9pF(Max)
- Channel I/O to I/O capacitance: 0.45pF(Max)
- Low clamping voltage
- Low operating voltage
- Improved zener structure
- Optimized package for easy high speed data lines PCB layout
- RoHS compliant
- Suffix "-H" indicates Halogen-free parts, ex. LL054BT6-H.

Mechanical data

- Epoxy : UL94-V0 rated flame retardant
- Case : Molded plastic, TSOP-6
- Terminals :Plated terminals, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.013 gram

Applications

- HDMI / DVI ports
- Display Port interface
- 10M / 100M / 1G Ethernet
- USB 2.0 interface
- VGA interface
- Set-top box
- Flat panel Monitors / TVs
- PC / Note book

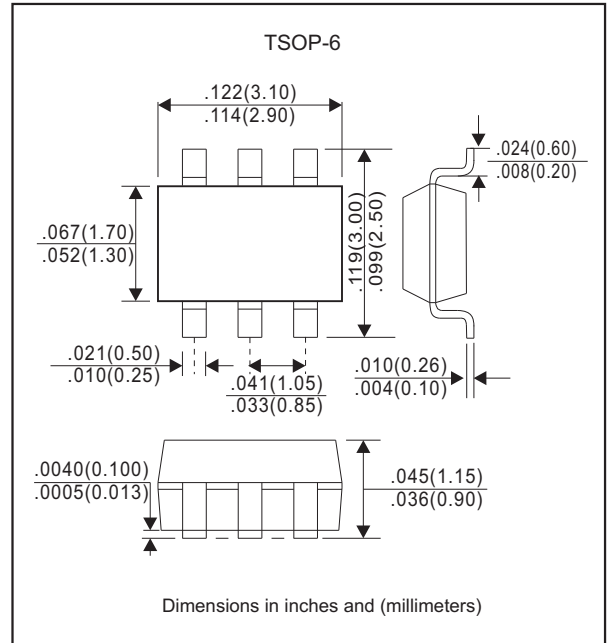
Maximum ratings (at $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Peak pulse power(8/20us)	P_{PP}	150	W
Peak pulse current IEC 61000-4-5(8/20us)	I_{PP}	5	A
ESD per IEC 61000-4-2(air) ESD per IEC 61000-4-2(contact)	V_{ESD}	± 15 ± 8	kV
Operating junction temperature range	T_{opr}	-55 to +125	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 to +150	$^\circ\text{C}$

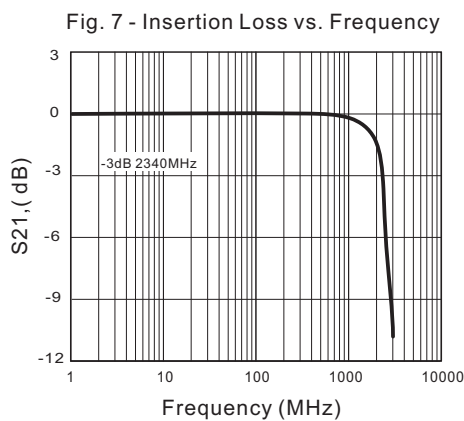
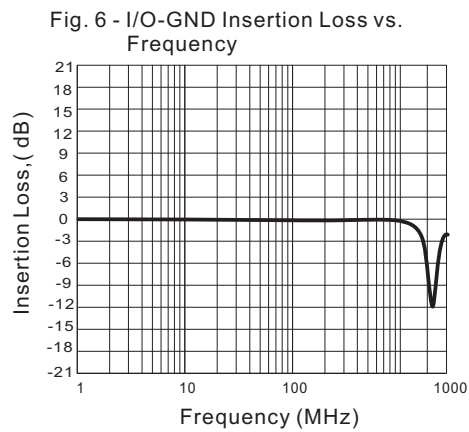
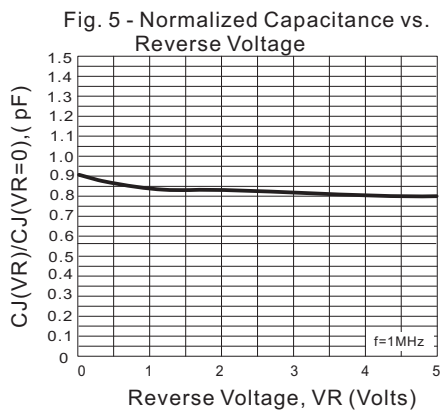
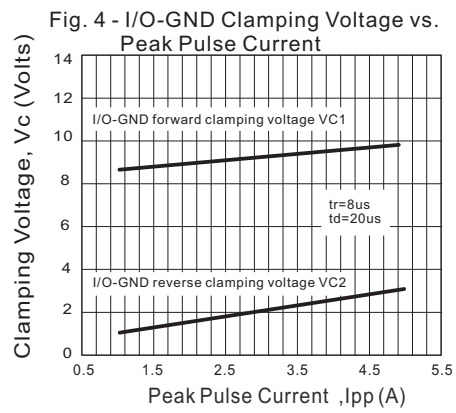
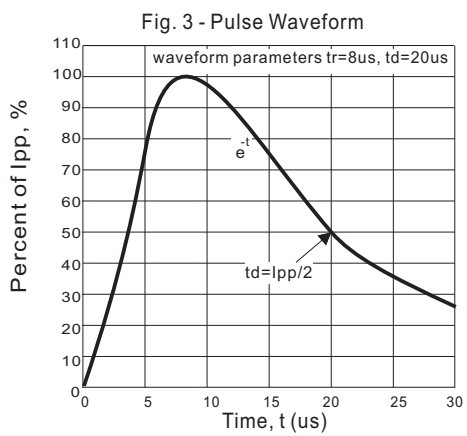
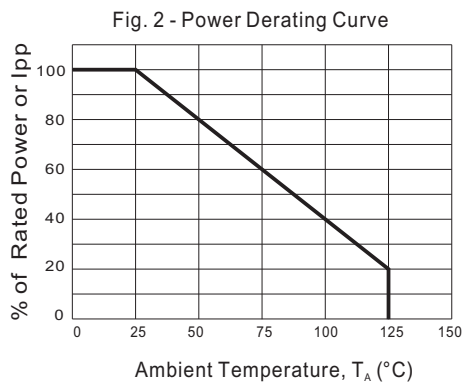
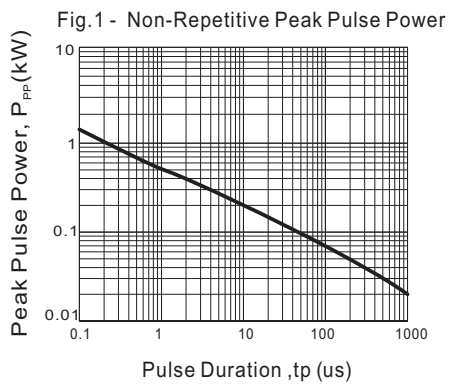
Electrical characteristics (at $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Reverse working voltage	any I/O pin to GND	V_{RWM}			5.0	V
Reverse breakdown voltage	$I_T = 1\text{mA}$, any I/O pin to GND	V_{BR}	6.0			V
Reverse leakage current	$V_{RWM}=5\text{V}$, any I/O pin to GND	I_R			1.0	μA
Positive clamping voltage	$I_{PP}=1\text{A}$, $t_p=8/20\mu\text{s}$, positive pulse; any I/O pin to GND	V_{C1}		8.5	12.0	V
Negative clamping voltage	$I_{PP}=1\text{A}$, $t_p=8/20\mu\text{s}$, negative pulse; any I/O pin to GND	V_{C2}		1.8		V
Junction capacitance Between channel	$V_R=0\text{V}$, $f=1\text{MHz}$, between I/O pins	C_{J1}		0.35	0.45	pF
Junction capacitance Between I/O and GND	$V_R=0\text{V}$, $f=1\text{MHz}$, any I/O pin to GND	C_{J2}			0.9	pF

Package outline



Rating and characteristic curves (LL054BT6)



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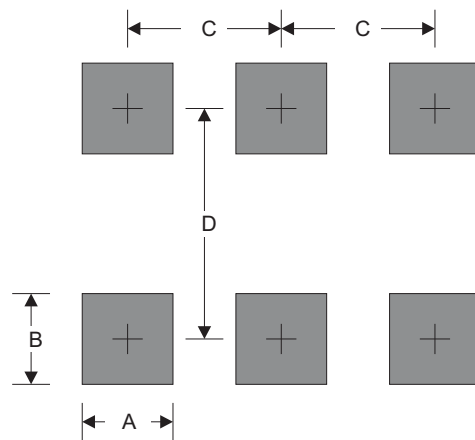
Pinning information

Pin Configuration	Simplified outline	Circuit Diagram
<p>Pin Configuration diagram showing a 6-pin package with pins 1-6 and their functions: I/O1, GND, I/O2, I/O3, VREF, I/O4.</p>	<p>Simplified outline of the LL054BT6 package showing pin locations 1, 2, 3, 4, 5, 6.</p>	<p>Circuit diagram showing the internal ESD protection structure with diodes connected to pins 1, 3, 4, 6 and ground.</p>

Marking

Type number	Marking code
LL054BT6	C96

Suggested solder pad layout

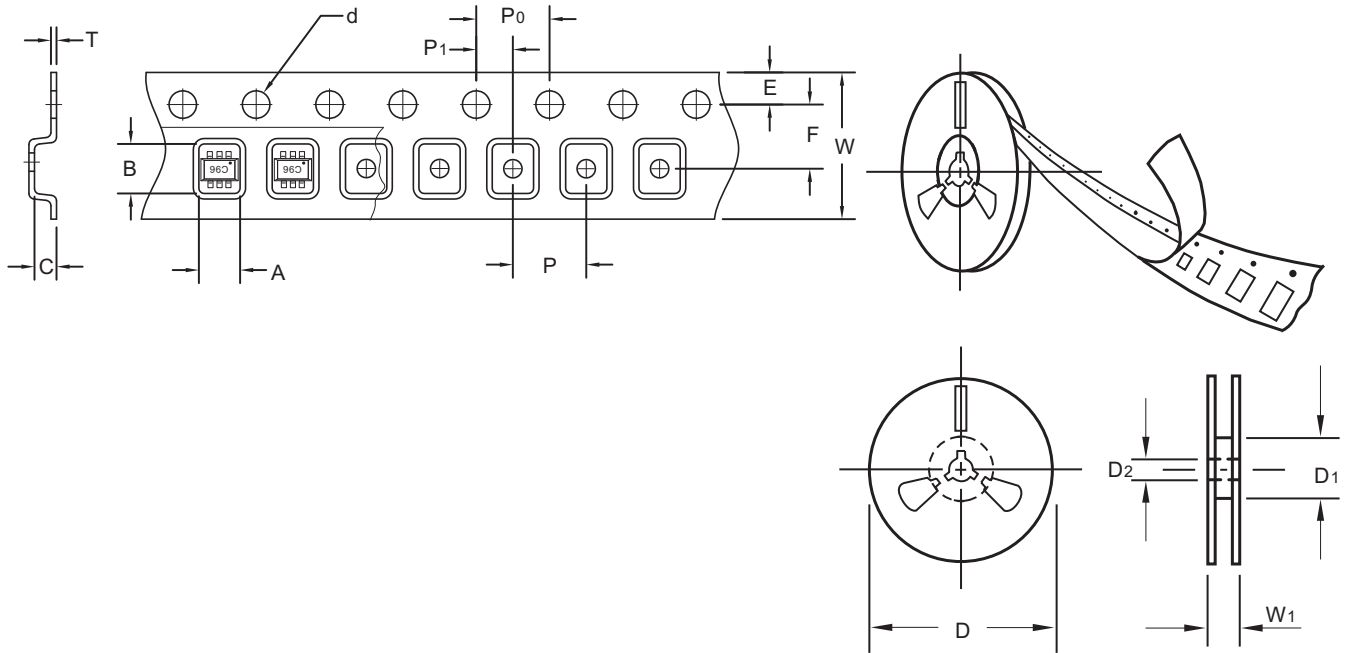


Dimensions in inches and (millimeters)

PACKAGE	A	B	C	D
TSOP-6	0.028 (0.70)	0.039 (1.00)	0.037(0.95)	0.094(2.40)

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Packing information



unit:mm

Item	Symbol	Tolerance	TSOP-6
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D ₁	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D ₁	min	54.4.00
Feed hole diameter	D ₂	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.05	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P ₀	0.1	4.00
Embossment center	P ₁	0.05	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W ₁	max	14.40

Note: Devices are packed in accordance with EIA standard RS-481-A and specifications listed above.

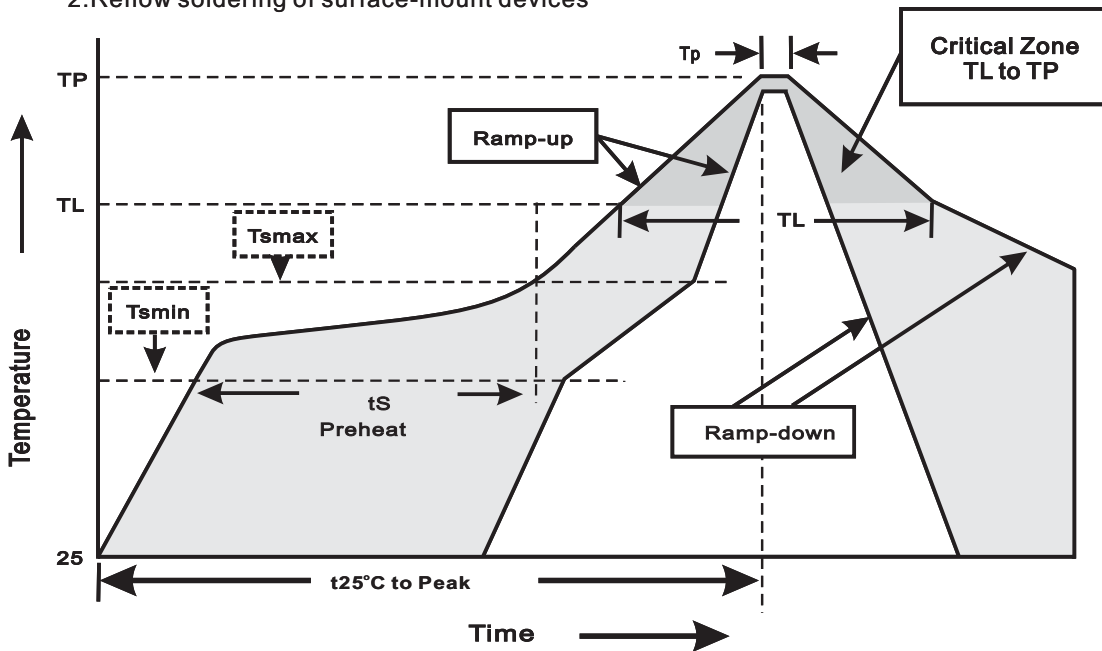
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Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
TSOP-6	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000	9.50

Suggested thermal profiles for soldering processes

- 1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
- 2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(TL to TP)	<3°C/sec
Preheat -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time(min to max)(ts)	150°C 200°C 60~120sec
Tsmax to TL -Ramp-upRate	<3°C/sec
Time maintained above: -Temperature(TL) -Time(tL)	217°C 60~260sec
Peak Temperature(TP)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(tp)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes

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High reliability test capabilities

Item Test	Conditions	Reference
1. Solder Resistance	at 260±5°C for 10±2sec.	MIL-STD-750D METHOD-2031
2. Solderability	at 245±5°C for 5 sec.	MIL-STD-202F METHOD-208
3. High Temperature Reverse Bias	$V_{BR} = V_{BR\ Min} * 80\%$ at $T_J = 125^\circ\text{C}$ for 168 hrs.	MIL-STD-750D METHOD-1038
4. Pressure Cooker	15P _{SIG} at $T_A = 121^\circ\text{C}$ for 4 hrs.	JESD22-A102
5. Temperature Cycling	-55°C to +125°C dwelled for 30 min. and transferred for 5min. total 10 cycles.	MIL-STD-750D METHOD-1051
6. Humidity	at $T_A = 85^\circ\text{C}$, RH=85% for 1000hrs.	MIL-STD-750D METHOD-1021
7. High Temperature Storage Life	at 175°C for 1000 hrs.	MIL-STD-750D METHOD-1031